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Modified PID Implementation On FPGA Using Distributed Arithmetic Algorithm

Comparison with traditional implementation

Wasim Ghder Soliman[1]and Prof. Vinod P.Patel[2]

[1]Final year student in Instrumentation and control Engineering Department
[2]Associate professor in Instrumentation and control Engineering Department

[1,2]L.D Engineering College of Engineering, Ahmedabad-380015

Abstract- *As we know that the application of PID controller span from small industry to high industry. In order to implement the PID controller on microprocessors or on FPGA, we need a digital form of that controller. Indeed, several digital forms of PID controller were developed. The key consideration of any design on FPGA is the resources consumption. In this paper two different schemes of PID implementation on FPGA are presented. The first one is distributed arithmetic algorithm lookup table (DALUT) based PID controller, and the second one is multipliers based PID controller. The resources consumption of both schemes is compared using XILINX tool boxes on MATLAB. The DALUT based PID controller is more efficient and consumes less FPGA resources.*

Keywords- *distributed arithmetic, PID controller, Xilinx sysgen, FPGA design, multiplierless.*

I. INTRODUCTION

An important feature of PID controller is that it does not need a precise analytical model of the system that is being controlled. For this reason, PID controllers have been widely used in process control, manufacturing, robotics, automation, transportation, and interestingly in real-time scheduling of concurrent tasks in multi-tasking applications [1].

Field Programmable Gate Arrays (FPGA) have become an alternative solution for the realization of digital control systems, previously dominated by the general-purpose microprocessor and application specific integrated circuits (ASIC) [1]. The FPGA-based controllers offer advantages such as high-speed computation, complex functionality, real- time processing capabilities, and low power consumption.

Conventional implementation of FPGA based controllers have not focused on optimal use of hardware resources. These designs usually require a large number of multipliers and adders and do not efficiently utilize the memory-rich characteristics of FPGAs [5]. An FPGA chip consists of a lot of memory blocks, referred to as Look-Up Tables (LUT), which can be utilized to implement efficient designs.

In this work, we utilize the Distributed Arithmetic (DA) scheme [6], which is an efficient LUT design method, and is very promising in the FPGA implementation of PID controller.

Distributed Arithmetic (DA) architecture, which was first purposed by Peled and Liu in 1974, can be used to implement multiplierless FPGA based PID controller [3].

In this paper we obtain one of the PID controller digital forms by using the Distributed Arithmetic (DA) algorithm and then we use Xilinx tool boxes on MATLAB SIMULINK in order to get the estimated resources from FPGA, after that we use same tools to simulate the multiplier based PID controller, then we get also the estimated resources consumption, finally we compare the two results.

II. THE PID CONTROLLER

The application of a PID controller in a feedback control system is shown in Fig. 1.2, where u_c is the command signal, y is the feedback signal, e is the error signal, and u is the control input. The simplest form of the PID control algorithm is given by:

$$u(t) = k\left(e(t) + \frac{1}{T_i}\int_0^t e(t)dt + T_d\frac{de(t)}{dt}\right) \qquad (2.1)$$

Where:

e(t) = error signal.

u(t) = Command signal.

K = Gain or Proportional gain.

T_i = Integration time or rise time.

T_d = Derivative time.

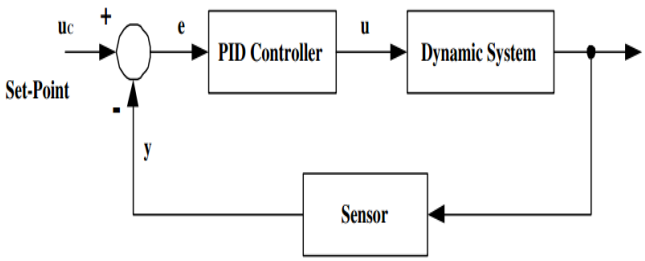

Fig.1.2. A PID-based feedback control system.

PID controller provides proportional, integral, and derivative compensation to an existing system, where:

P Control: Increases gain margin & stabilizes the unstable system.

I Control: Minimizes Steady State error.

D Control: Increases System Speed by increasing system Bandwidth.

It does not need a precise analytical model of the system that is being controlled. It is used in many different areas, such as aerospace, process control, manufacturing, robotics, automation, and transportation system.

III. DISTRIBUTED ARITHMETIC (DA) ALGORITHEM

Distributed Arithmetic (DA) is a bit-serial algorithm which performs efficient multiplication by using LUT's [3].

Consider sum of product (SOP) calculation as:

$$Y = \sum_{k=0}^{N-1} A_k x_k \qquad (3.1)$$

Where:

A_k = constant coefficient.

x_k = input data of size N.

Y = output.

Now assuming that it is a 2's complement fractional number and representing x_k bit-wise format so we get:

$$x_k = -x_{k,0} + \sum_{j=1}^{M-1} x_{k,j} 2^j \qquad (3.2)$$

Where:

$x_{k,0}$= jth bit of x_k

$x_{k,j}$= Sign Bit.

M = Word Size.

Substituting we get:

$$Y = \sum_{k=0}^{N-1} A_k \left[$$

$$Y = -\sum_{k=0}^{N-1} A_k$$

Defining:

$$Z_j = \sum_{k=0}^{N-1} A_k x$$

And

$$Z_0 = -\sum_{k=0}^{N-1} A$$

So the output will be written as:

$$Y = \sum_{j=0}^{M-1} Z_j 2^j \qquad (3.7)$$

These values can be pre-calculated and stored in Look Up Tables (LUT's) or ROM. The output can be calculated by shifting and addition operations for all Z_j's from jth bit.

3.1 PID Implementation using DA Algorithm

DA based PID ontroller is area efficient as it can fit on very small FPGA chips.

In the equation (2.1), we cannot implement derivative control purely because it will amplify noise. So its gain must be limited, and in this way noise can be reduced.

Taking Laplace transform of PID equation:

$$U(s) = k\left(E(s) + \frac{1}{sT_s}E(s) + sT_D E(s)\right) \qquad (3.1-1)$$

Approximating the sT_D as follows:

$$T_D = \frac{sT_D}{1 + {sT_D}/{N}} \qquad (3.1-2)$$

This approximation is correct for the low frequencies while at high frequencies the gain is limited by N ranges from 3 to 20. It was found that only a fraction 'f' of the command signal act on the proportional gain.

Now improved PID algorithm is given by:

$$U(s) = k\left(fU_d(s) - Y(s) + \frac{1}{sT_s}\left(U_d(s) - Y(s)\right) - \frac{sT_D}{1 + {sT_D}/{N}}Y(s)\right) \qquad (3.1-3)$$

Discretizing the above equation we get:

$$U(K) = PR(K) + IN(K) + DE(K) \qquad (3.1-4)$$

Where:

$$PR(K) = K\left(f U_d(K) - Y(K)\right) \qquad (3.1-4)$$

$$IN(K) = IN(K-1) + \frac{K}{T_i}\left(U_d(K-1) - Y(K-1)\right) \qquad (3.1-5)$$

$$DE(K) = \frac{T_d}{T_d + NT} DE(K-1) - \frac{KT_d N}{T_d + NT}\left(Y(K) - Y(K-1)\right) \qquad (3.1-6)$$

Now by using the DA algorithm the above equations are the form of:

$$PR(K) = \sum_{j=0}^{M-1} (kf * U_d(K)[j] - K * Y(K)[j]) * 2^j \qquad (3.1-7)$$

$$IN(K) = IN(K-1) + \sum_{j=0}^{M-1} \frac{KT}{T_i} (U_d(K-1)[j] - Y(K-1)[j]) * 2^j \qquad (3.1-8)$$

$$DE(K) = \sum_{j=0}^{M-1} (\frac{T_d}{T_d + NT} DE(K-1)[j] - \frac{KT_d N}{T_d + NT} (Y(K)[j] - Y(K-1)[j])) * 2^j \qquad (3.1-9)$$

Where T is the sampling time.

The results of $kf * U_d(K)[j] - K * Y(K)[j]$,

$\frac{KT}{T_i}(U_d(K-1)[j] - Y(K-1)[j])$, $\frac{T_d}{T_d+NT} DE(K-1)[j]$ and $\frac{KT_dN}{T_d+NT}(Y(K)[j] - Y(K-1)[j])$.

Can be pre-calculated and stored in respective LUT's denoted as LUT_{Pr}, LUT_{In}, LUT_{De1} and LUT_{De2}.

The contents of these LUT's are:

Table 3.1-1: CONTENTS OF LUT_{Pr}

$U_d(K)[j]$	$Y(K)[j]$	LUT_{Pr}
0	0	0
0	1	-k
1	0	kf
1	1	$kf - k$

Table 3.1-2: CONTENTS OF LUT_{In}

$U_d(K-1)[j]$	$Y(K-1)[j]$	LUT_{In}
0	0	0
0	1	$-\frac{KT}{T_i}$
1	0	$\frac{KT}{T_i}$
1	1	0

Table 3.1-3: CONTENTS OF LUT_{De1}

$Y(K)[j]$	$Y(K-1)[j]$	LUT_{De1}
0	0	0
0	1	$\frac{KT_d N}{T_d + NT}$
1	0	$-\frac{KT_d N}{T_d + NT}$
1	1	0

Table 3.1-4: CONTENTS OF LUT_{De2}

$DE(K-1)$	LUT_{De2}
0	0
1	$\frac{T_d}{T_d + NT}$

Based on the above equations, the direct DA implementation of the PID controller is shown in Figure Fig.3.1-1.

The architecture of the DA based PID controller had been implemented using Xilinx tool boxes on MATLAB SIMULINK as shown on Fig.3.1-2.

The estimated resources consumption is given on Fig.3.1-3. , which is obtained using the block named Resource Estimator (Xilinx Resource Estimator).

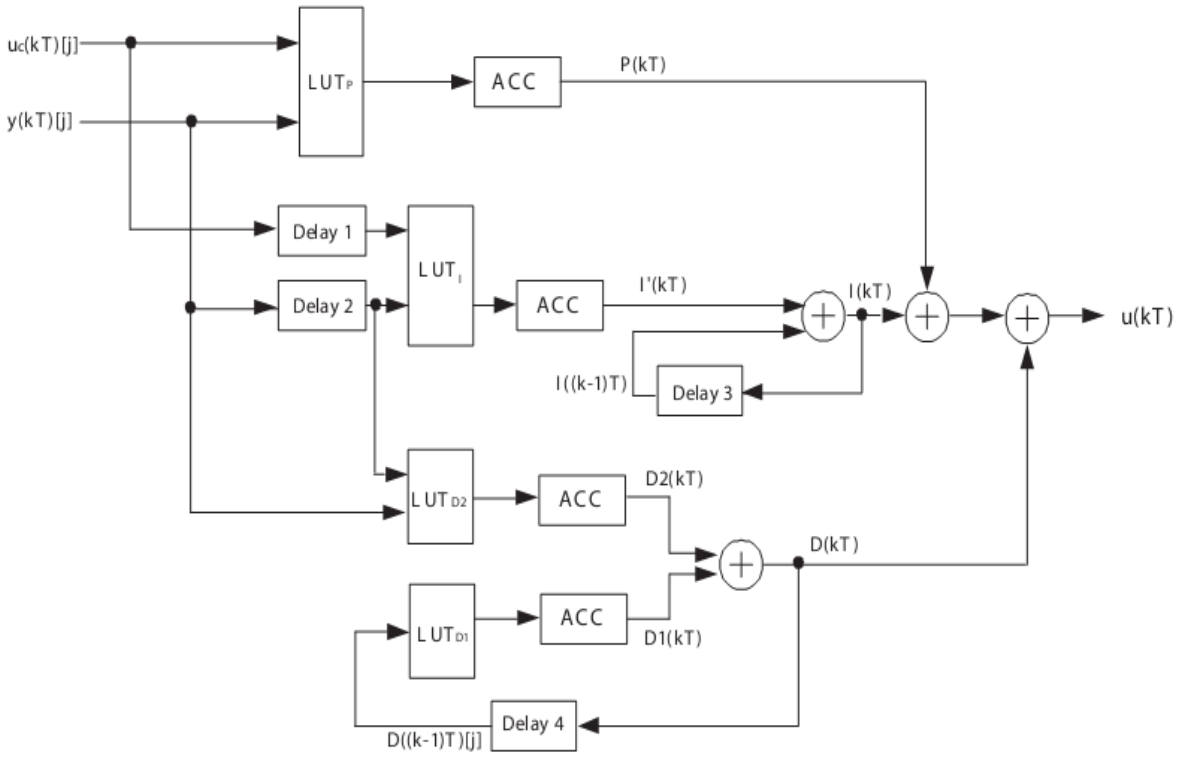

Fig.3.1-1. Architecture of the DA based PID controller

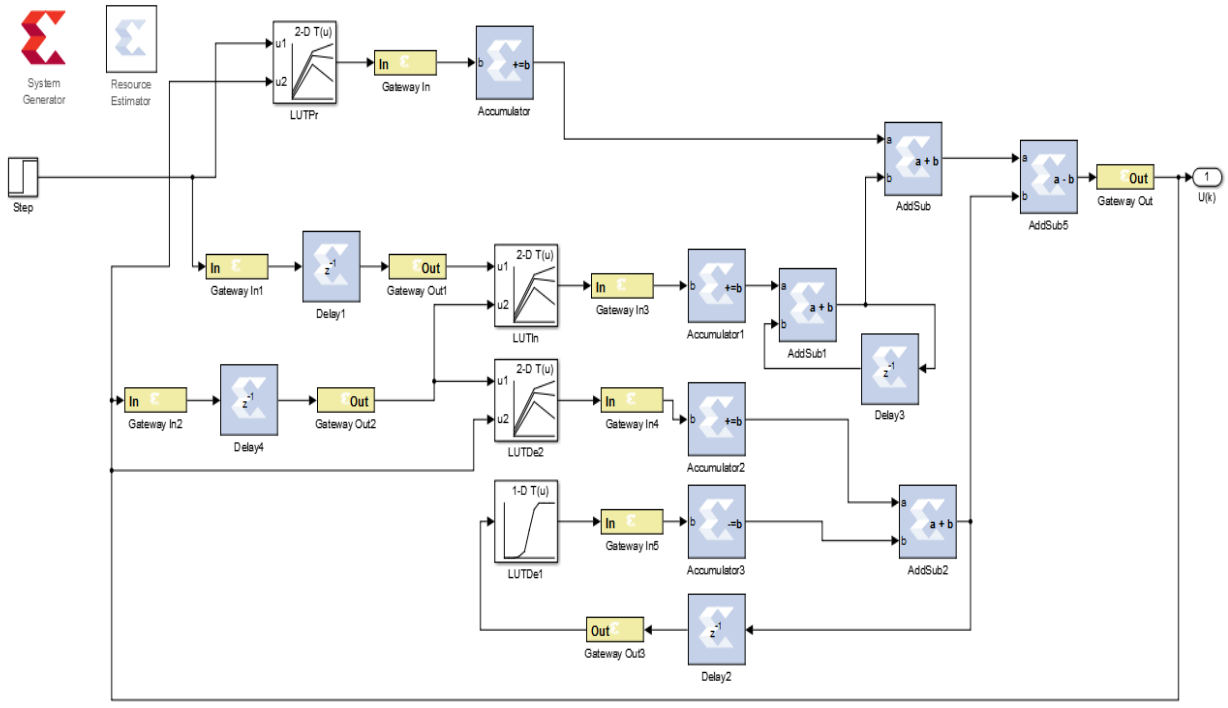

Fig.3.1-2. DA based PID controller using Xilinx tool boxes on MATLAB SIMULINK

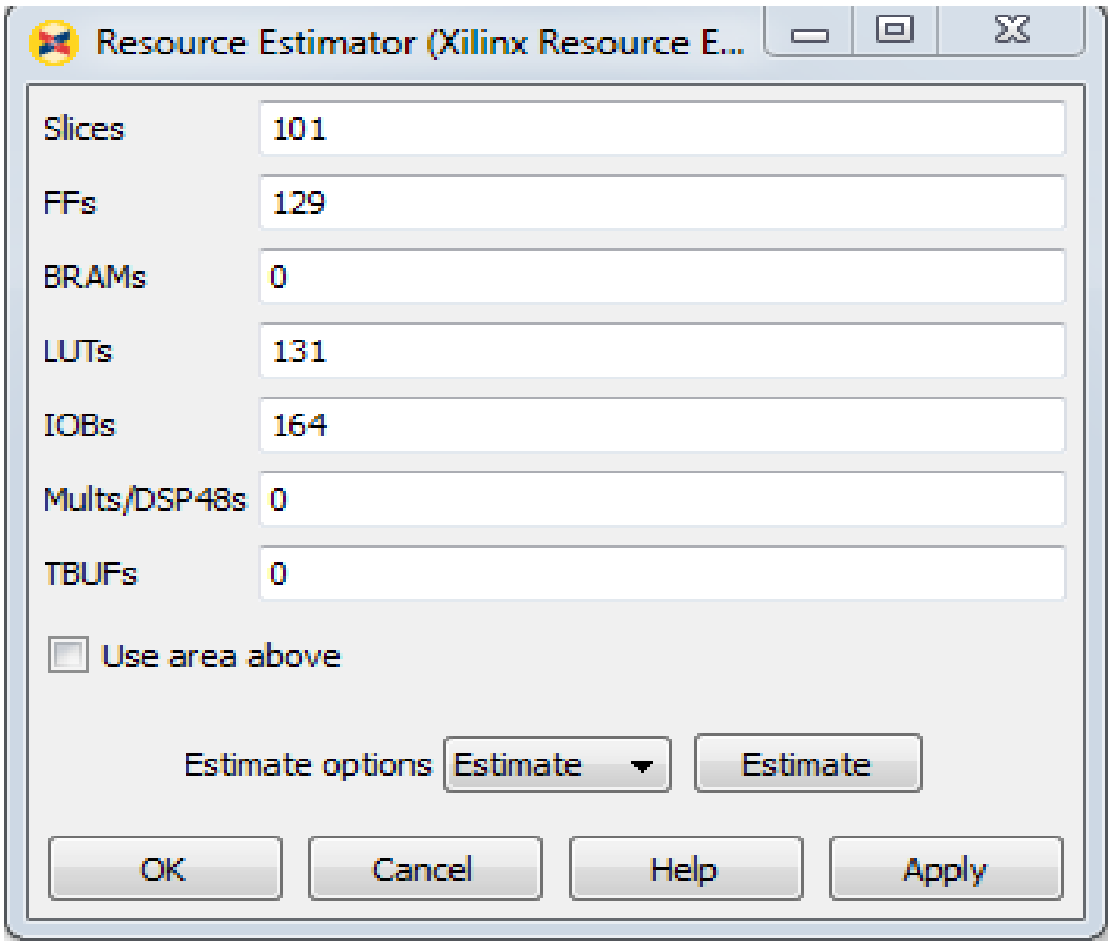

Fig.3.1-3. The estimated resources consumption

3.2.MULTIPLIER Based PID Controller

For digital implementation, we are more interested in a Z-transform of (1) in this case the after simplifying the transform we arrive to the following equation [2]:

$$u[k] = u[k-1] + k_1 e[k] + k_2 e[k-1] + k_3 e[k-2] \qquad (3.2-1)$$

Based on the above equation, the direct multiplier implementation of the PID controller is shown in Figure Fig.3.2-1.

The architecture of the MULTIPLIER Based PID controller had been implemented using Xilinx tool boxes on MATLAB SIMULINK as shown on Fig3.2-2.

The estimated resources consumption is given on Fig.3.2-3. , which is obtained using the block named Resource Estimator (Xilinx Resource Estimator).

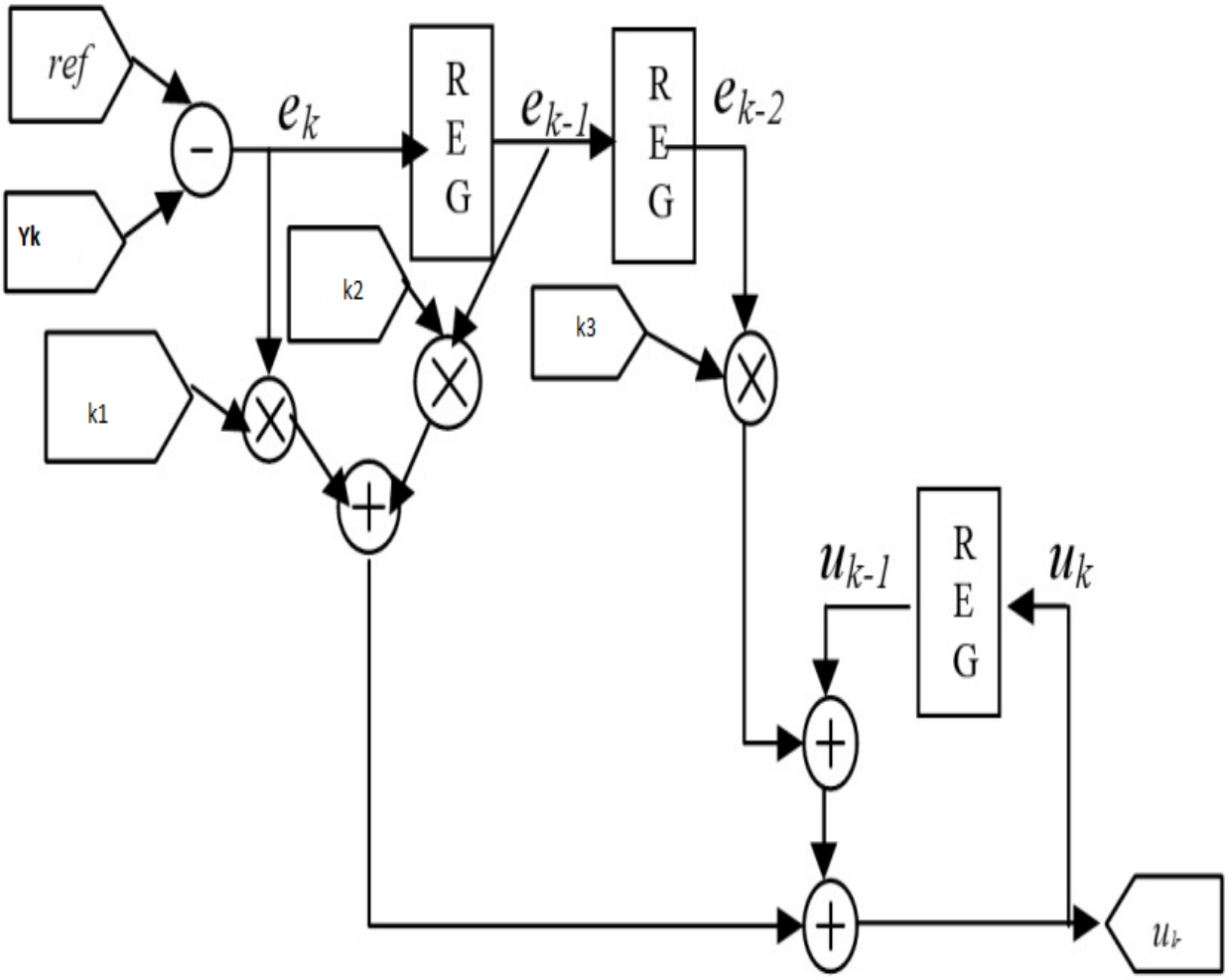

Fig.3.2-1.Architecture of the MULTIPLIER based PID controller

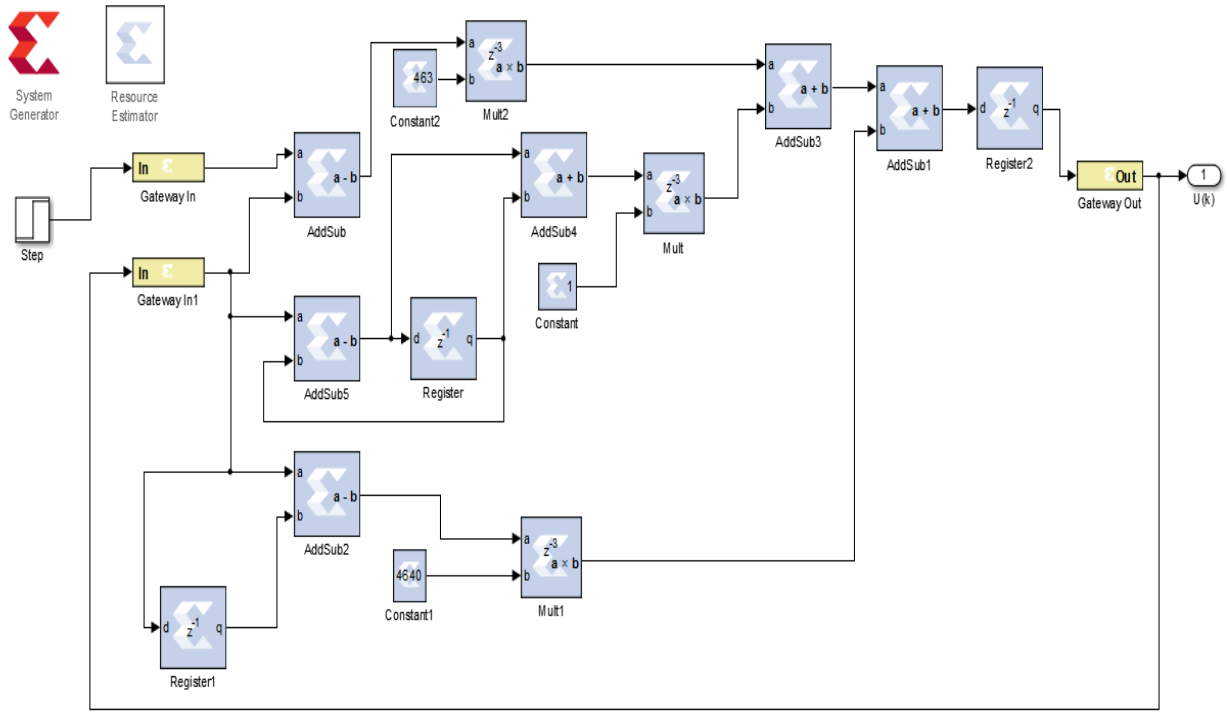

Fig3.2-2. MULTIPLIER based PID controller using Xilinx tool boxes on MATLAB SIMULINK

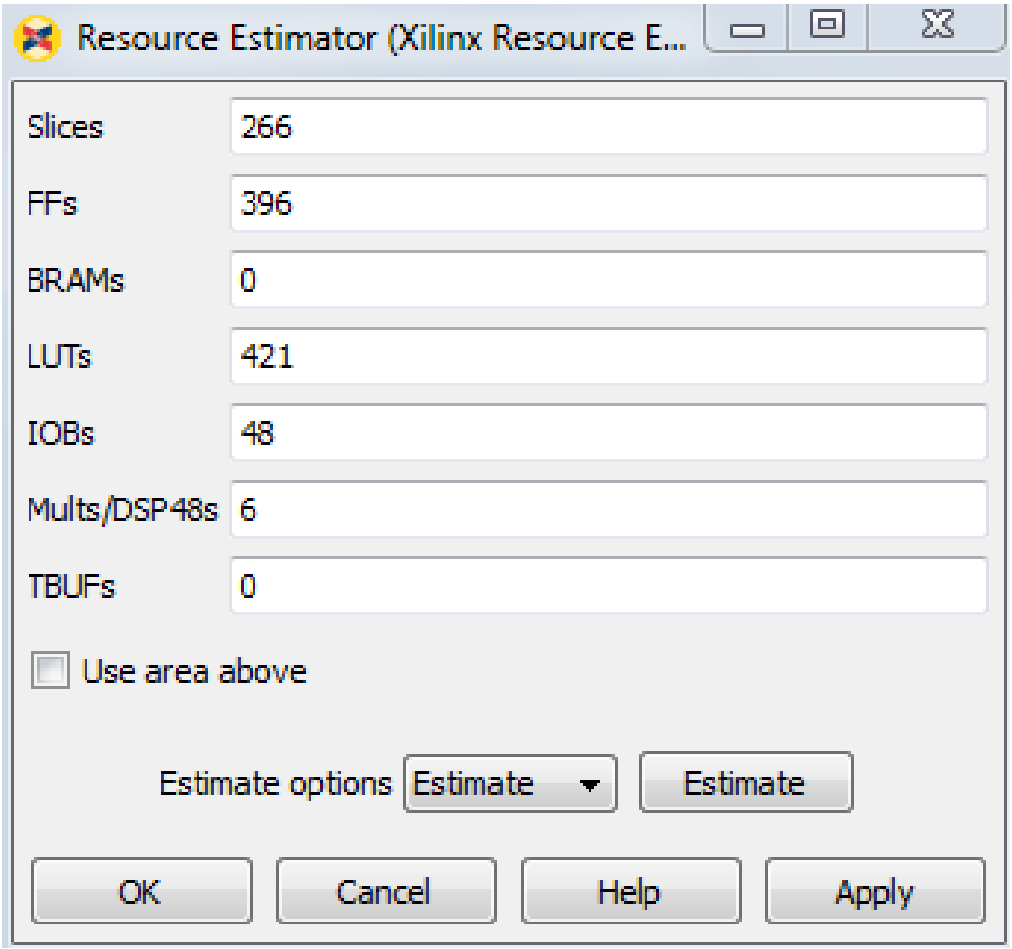

Fig.3.2-3. The estimated resources consumption

IV. CONCLUSTION

The synthesis report provides the information about slices, Flip-Flops, Input Output blocks, LUT's and Multipliers.

We can see that Multiplier based PID controller requires large number of hardware resources as compared to DALUT based PID controller.

The DA based PID controller reduces the cost of the FPGA design.

Due to the flexibility of the LUT in the FPGA, this FPGA-based PID controller can be easily extended to incorporate other algorithms.

This design approach would specifically be suitable for the next generation of FPGA chips, in which ADC and D/A converter are built inside the chip.

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