International Journal of Advance Engineering and Research Development (IJAERD)
Volume 1,Issue 5,May 2014, e-ISSN: 2348 - 4470 , print-ISSN:2348-6406

High performance dual output CMOS Realization of the Third Generation Current Conveyor (CCIII)

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Abstract— In this paper a new CMOS high performance dual-output realization of the third generation current conveyor (CCIII) is presented. The presented CCIIl provides good linearity, high output impedance at port Z and excellent input/output current gain. SPICE simulation results using TSMC 0.18µm and Generic 0.09µm CMOS process parameters in Mentor Graphics are given.

Keywords— CMOS Circuits, CCIII, SPICE

I. INTRODUCTION

Current conveyors and unity-gain amplifiers are widely used by analog designers especially in applications of signal processing and active network synthesis**.** In 1995, third generation current conveyor (CCIII) was introduced as a new active element for conveniently taking out the current flowing through a branch of a circuit [8].

The main features of the CCIII are low gain errors (high accuracy), high linearity and wide frequency response. In addition high output resistance at terminal Z of the CCIII is required to enable easy cascadability without need for additional active elements in applications. Unfortunately, because of the limited linearity and low output resistance of the basic current mirrors used in the structure of the conventional CCIII [8], its DC and AC performances are low.

In this paper, we introduced a new implementation of dual-output CCIII based on three unity gain cells. The circuit exhibits excellent output-input gain accuracy and frequency responses. Simulation results, which confirm the high performance of the new CCIII, are given.

II. CIRCUIT DISCRIPTION

The port relations of an ideal dual-output CCIII, which is shown in Figure 1, can he given by.

$$\begin{bmatrix} I_Y \\ V_X \\ I_{Z+} \\ I_{Z-} \end{bmatrix} = \begin{bmatrix} 0 & -1 & 0 & 0 \\ 1 & 0 & 0 & 0 \\ 0 & 1 & 0 & 0 \\ 0 & -1 & 0 & 0 \end{bmatrix} \begin{bmatrix} V_Y \\ I_X \\ V_{Z+} \\ V_{Z-} \end{bmatrix} \quad (1)$$

where the positive and negative signs define a positive and negative current-controlled conveyor, respectively.

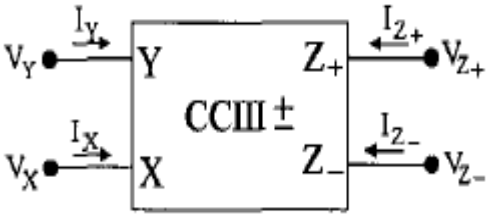


Figure1 Symbol of the CCIII.

The conventional third generation current conveyor is shown in Figure 2**.** It is based on basic current mirrors (M_6, M8), (M_5.M_7), (M_{14}, M16) and (M_{13}, M15). The currents in ports X and Y is transferred to the ports Z+ and Z by the output stage transistors M_{21}-M_{22} and M_{23}-M_{24} respectively. A major advantage of this CCIII is its simple structure. The Z+ output resistance of this current conveyor is calculated as

$$\mathbf{R_{oz+} = (r_{ds21})// (r_{ds22})} \qquad (2)$$

Where r_{dsi} denotes the output resistance of the i'th transistor respectively. The Z- output resistance of the conveyor can be calculated similarly. An important drawback of the conventional CCIII is the finite output resistance (R_{oz}).

Figure 3 is shown a DOCCIII by combining the VF-C with simple CMs, where PMOS and NMOS Current mirrors are formed by M9/M11 and M10/M12.First PMOS and NMOS current followers are formed by M9/M13/M15/M17 and M10/M14/M16 M18. Finally second PMOS and NMOS Current followers are formed by M9/M13/M15/M17 and M10/M14/M16 M18.

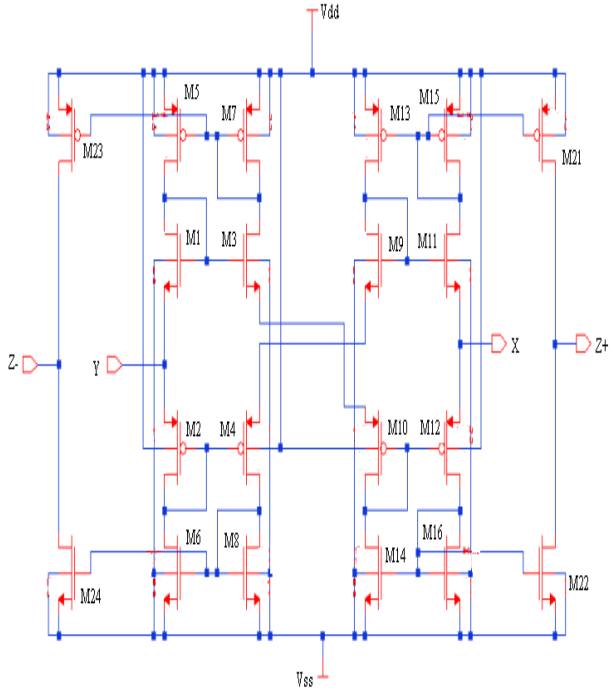


Figure 2 Schematic of Conventional third generation current conveyor (CCIII)

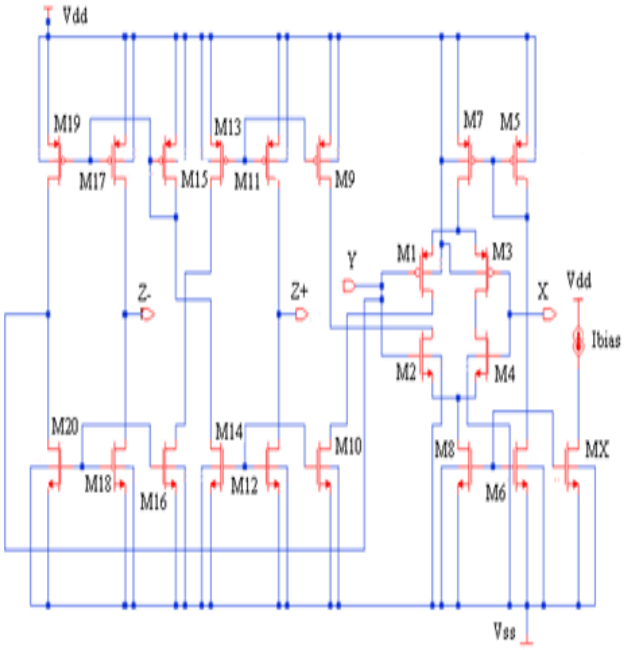


Figure 3 Schematic of DOCCIII by combining VF-C with simple CMs

III. SIMULATION RESULTS AND COMPARISON

Simulation Results for TSMC 0.18µm CMOS Technology

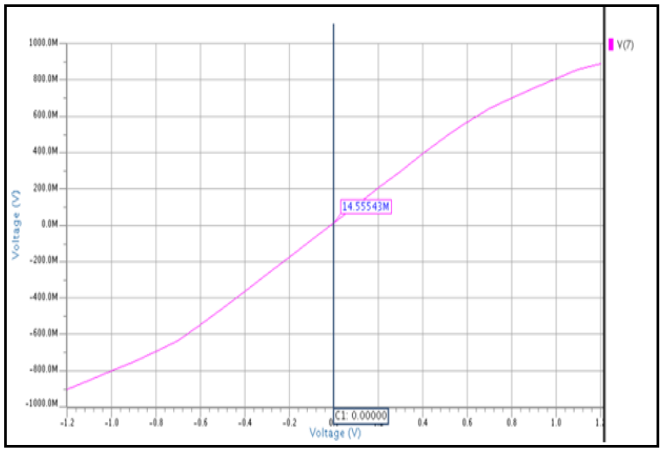


Figure 4 DC voltage characteristics at port X.

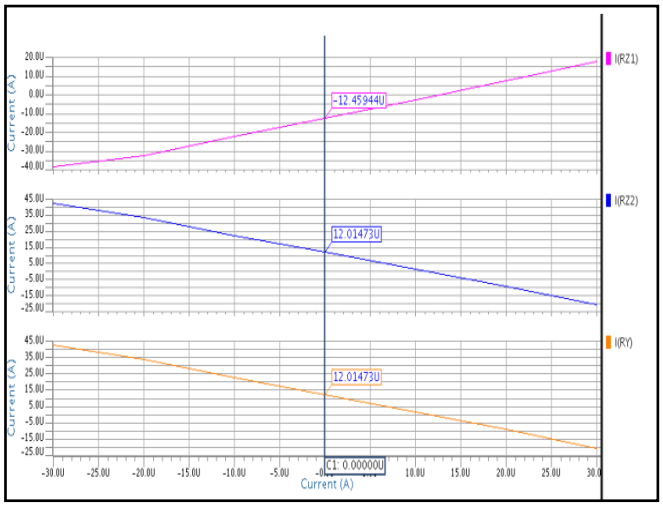


Figure 5 DC current characteristics at port Z+.

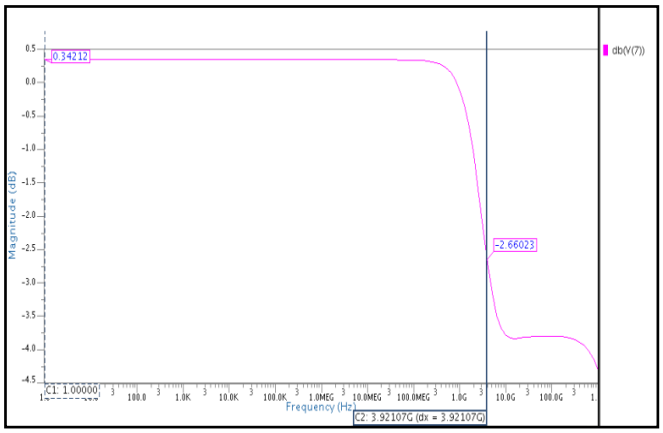
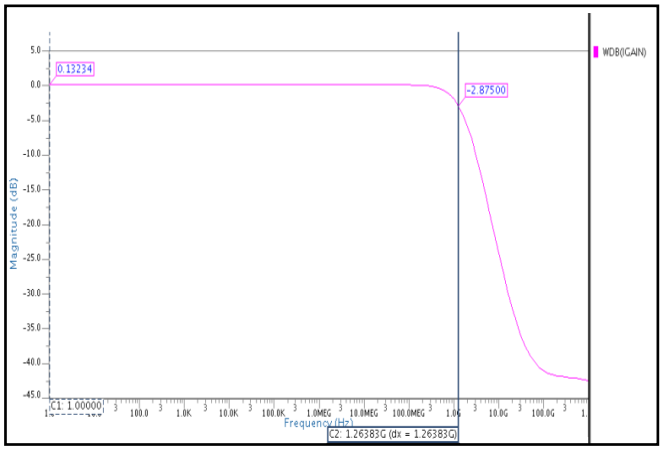


Figure 6 Frequency response of voltage gain at port X



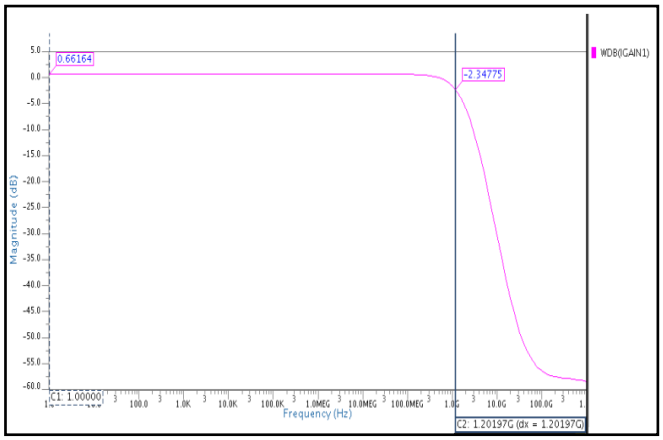


Figure 7 Frequency response of current gain and Bandwidth at ports Z+ and Z-.

Simulation Results for Generic 0.09µm CMOS Technology

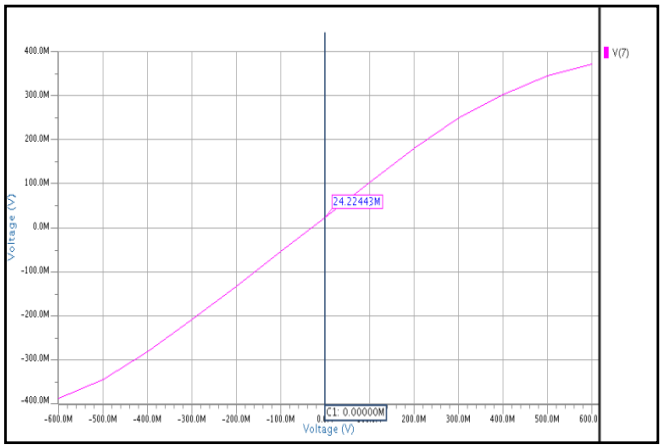


Figure 8 DC voltage characteristics at port X.

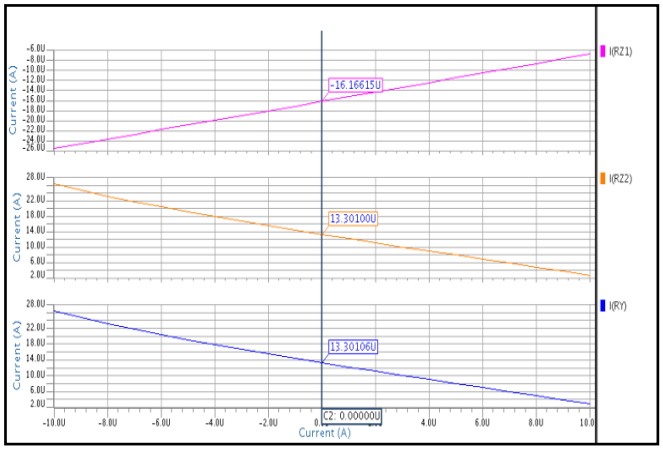


Figure 9 DC current characteristics at port Z+.

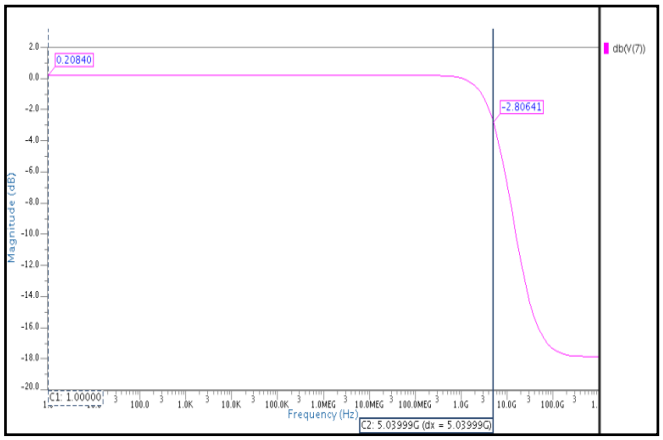


Figure 10 Frequency response of voltage gain at port X

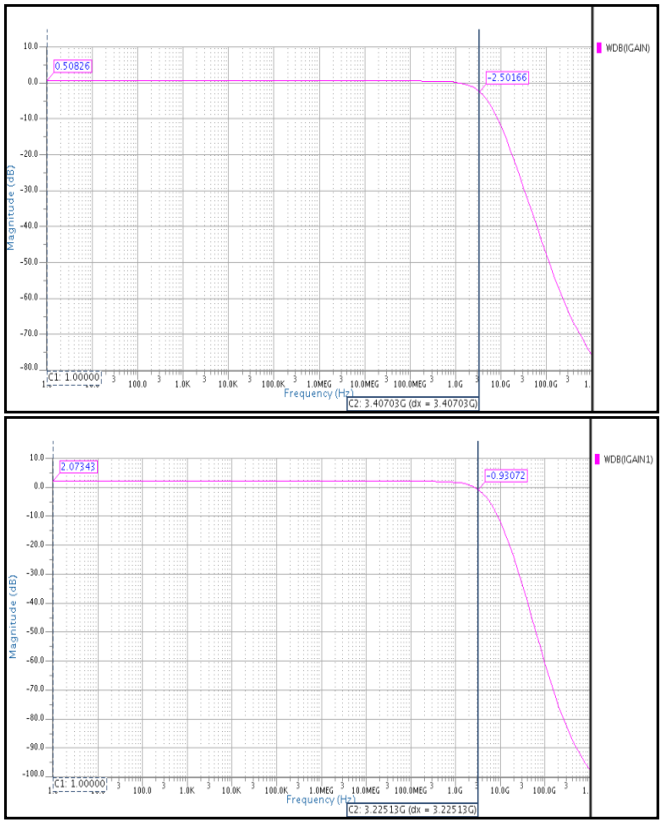


Figure 11 Frequency response of current gain and Bandwidth at ports Z+ and Z-.

IV: COMPARATIVE RESULTS

Table 1 Comparison of Characteristics for all CCIIIs described above in 180nm and 90nm CMOS technology

Current Conveyor Characteristics Simulated Value				
Characteristics	**Third Generation Current Conveyors**			
	Conventional CCIII	**DOCCIII**	**Conventional CCIII**	**DOCCIII**
	0.18µm		**0.09µm**	
Supply Voltage	±1.2V	±1.2V	±0.6V	±0.6V

Power Dissipation	0.09mW	0.49mW	0.065mW	0.22mW
3dB Current Bandwidth	158MH$_z$	1.26GH$_z$	1.6GH$_z$	3.40GH$_z$
3dB Voltage Bandwidth	169MH$_z$	3.92GH$_z$	1.34GH$_z$	5.04GH$_z$
Biasing Current I_{bias}	-	30µA	-	10µA
Offset	4mV	14.55mV	2.94mV	24mV
Current Gain(β)	1.07	1.07	1.2	1.14
Voltage Gain(α)	1.06	1.04	1.2	1.02
Node x Parasitic Impedance	360	4.16KΩ	674Ω	5.6KΩ
Node Y Parasitic Impedance	1.38KΩ	3.60KΩ	1.52KΩ	3.08KΩ
Node z Parasitic Impedance	1.01MΩ	94KΩ	18.16 KΩ	16.92KΩ

From the table 1, it can be seen that DOCCIII has higher value of output offset voltage and power dissipation but it can gives us higher speed than the conventional CCIII.

V: CONCLUSION

New high Speed CMOS third-generation current conveyor is presented. The presented circuit uses three unity gain cells namely Current mirror, Current follower and Voltage follower which increases the voltage and current bandwidths. The simulation results confirm high speed and performance of the circuits in terms of linearity, voltage and current gain accuracy.

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