

POWER OPTIMIZATION AND AREA-EFFICIENT SHIFT REGISTER USING PULSED LATCHES

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Abstract—The area and power consumption are reduced by replacing flip-flops with pulsed latches. The flip-flop performance is a significant element to regulate the efficiency of the entire synchronous circuit. The replacing method solves timing problem between pulsed latches through the use of multiple non-overlap delayed pulsed clock signals in conventional single pulsed clock signal. The pulsed clock signals uses a small number of shift registers by grouping many sub shifter registers and using additional temporary storage latches. In addition, we further proposed a modified sub-shift register using pulsed latches and 512-bit shift register to reduce the power.

Index Terms— Area-Efficient, Flip-Flop, Pulsed Clock, Pulsed Latch, Shift Register.

I. INTRODUCTION

In digital design latches and flip-flops are basic storage element. The performance of flip-flop is an significant element to regulate the efficiency of the entire synchronous circuit. Flip-flops are uncertain timing elements in digital circuits which have a great impact on speed and power consumption[1]. In VLSI chip design reducing power has become a most consideration of an performance and area. Mainly shift register is a type of sequential circuit it is used for storage or transfer digital data. In several applications flip-flops are replaced by pulsed latch. Pulsed latches are smaller than flipflops. The use of multiple non-overlap delay pulsed clock signals substituted by the traditional single pulsed clock signals by solves the timing problem in pulsed latches[2]. The shift register uses a less number of the pulsed clock signals and combine the latches to many sub shift registers and over work further temporary storage latches. Shift registers are mainly used in digital filters[3], communication receivers [4], and image processing ICs[5]. Because of high quality image data, the size of the image data is increases. A4k-bit shift register uses a VLSI chip because of an image-extraction and vector generation. A2k-bit shift register in 10-bit 208 channel output LCD column driver IC[6]. The word length of the shift register increases, the area and power consumption of the shift register become important design consideration.

II. ARCHITECTURE

The flip-flops are combined to form shift register which shares the same clock, each flip-flop output of data is given to input of next flip-flop. The master-slave flip-flops are using two latches to share the same clock pulse. The pulsed latch we taken as pulsed clock signal to replace the two pulsed latches. Master-slave flip-flop using normal clock signal. The pulsed latch using the pulsed clock signal. Compare to master-slave flip-flop the pulsed latch size is almost half so that the area and power reduces. All pulsed latches share the pulse generation circuit because of the pulsed clock signal. The pulsed latch is an good solution for small area and low power consumption.

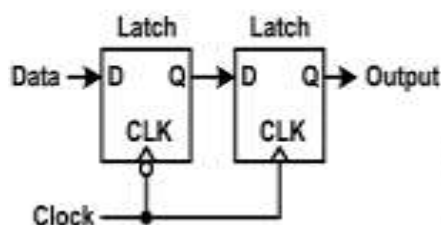
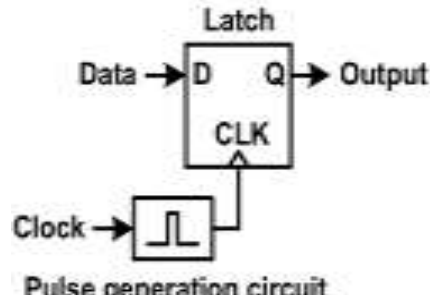


Figure 1(a) Master-slave flip-flop



1(b) Pulsed latch.

Because of the timing problem pulsed latch cannot be used in shift register. The shift register consists of the some latches and pulsed clock signal. Figure(2a) The clock pulse is given to the first latch. The output signal of the first latch(Q1) changes correctly because of the input signal of the first latch(IN) and constant during the clock pulse width.

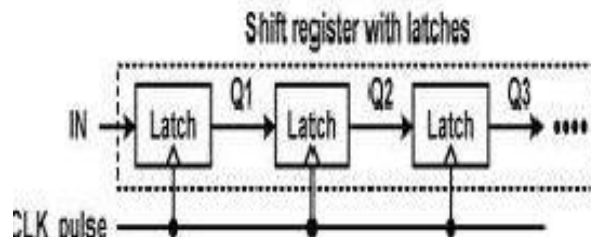


Figure 2 Shift register with latches and a pulsed clock signal. (a) schematic

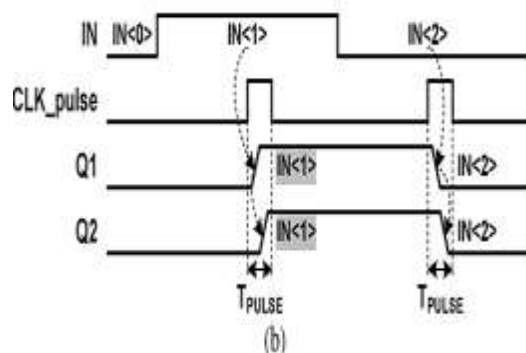


Figure (b) Wave forms

In this Figure Q1 changes correctly. But Q2 is not changes correctly. Because of timing problem. Compare to Q1 the Q2 is having some delay. Because of when the input is active then only output come to next state of input on that time it is in off state. So here some delay produces.

Here two solutions for to overcome the timing problems. One solution for the timing problem is to add delay circuits. The input clock signal is giving first latch and here adding the delay circuits.here output signal of the latch is delayed and reaches the next latch after the clock pulse. During the clock pulse width the output signal of the first and second latches change. The second and third latches of the input signal becomes same as the first and second latches after the clock pulse width. So here all latches is having the constant input and no timing problem occurs between the latches.

Another solution for overcome the timing problem is to use multiple non-overlap delayed pulsed clock signals. when the pulsed clock signals goes through delay circuits then the delayed pulsed clock signals are generated. Each latch uses a pulsed clock signal which is delayed from pulsed clock signal. So each latch update the data after its next latch update the data. So that each latch has a constant input during its clock pulse and no timing problem occurs between the latches.

III. EXISTING ARCHITECTURE

A. PULSED CLOCK GENERATOR

In clock generator the clock pulse circuit consists clock, delay, buffers and AND gate. In this all inverts are having the rising and falling times in delay circuits. so that the AND gate generated with inverters to get the sharp pulsed clock signals. Each pulse clock signal arrives at the sub shift register because of the pulse skew. All pulse clock signals have almost same pulse skew when they arrive at the sub shift register. The clock pulse intervals larger than the pulse skew differences cancel out of the effects of the pulse skew differences.

To insert the clock buffers and clock trees to send the short clock pulse width with a small wire delay. The rising and falling times of the clock pulse width is small because each sharp pulsed clock signal is generated from an AND gate and two delayed signals. so that the delayed pulsed clock generator matches for short pulsed clock signals. In this clock pulse circuit the delay and AND gate performs as a when clock pulse is giving to the delay and input of the AND gate and the output of the delay signal is given to the inverter and also goes to AND gate input. Here the delayed pulse clock signal changes in inverter, and it goes through the AND gate, and the final value is gives to the clock buffer, it will produce the output. And here second inverter changes the value and it gives to the another clock pulse circuit.

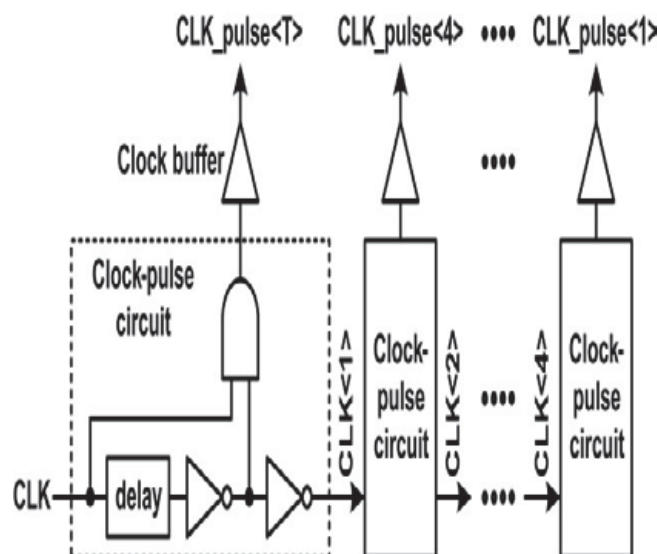


Figure 3. Delayed pulsed clock generator

Each pulsed clock signal is generated in a clock-pulse circuit consisting a delay circuit and AND gate.

B. SSASPL (Static Differential Sense Amplifier Shared Pulse Latch):

A latch can capture data only when the clock is enabled. If the pulse clock triggers a latch, then latch is synchronized similar to the edge triggered flip flop. The pulsed generators generate the pulsed clock waveforms with a source clock. SSASPL– latch is Static differential Sense Amplifier Shared Pulse Latch. This latch is the smallest latch. This latch has 9[7] transistors. In the proposed Shift Register this latch has been modified with 7 transistors by removing an inverter in the circuit.

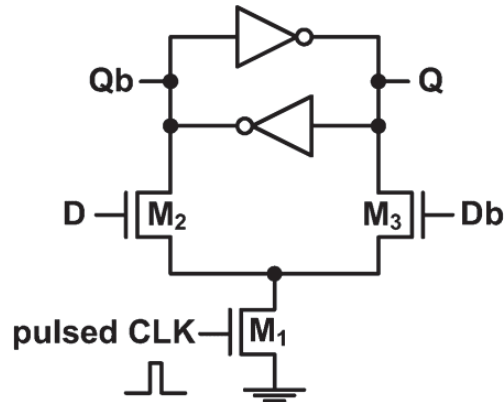


Figure4.Circuit diagram of SSASPL

The SSASPL updates the data with three NMOS transistors(M1-M3) and it grasps the data with four transistors in two cross-coupled inverters. SSASPL requires two differential data inputs (D and DB) and a pulsed clock signal. When a pulsed clock signal goes to high , data is updated. The node Qor QB is pulled down to ground according to the input data (D and DB). The pull-up current of the PMOS transistors must be smaller than the pull-down current of the NMOS transistors in the inverters.

C. PPCFF (Power-Pc-Style Flip-Flop):

The PPCFF is a master-slave flip-flop composed of two latches. The PPCFF consists of 16 transistors. In these 16 transistors , 8 transistors driven by clock signals.It uses the minimum size of transistors. The PPCFF uses 16 transistors, which is the smallest number of transistors among the flip-flops. The proposed PPCFF is area-efficient shift register which shows effectiveness in design of 256-bit.

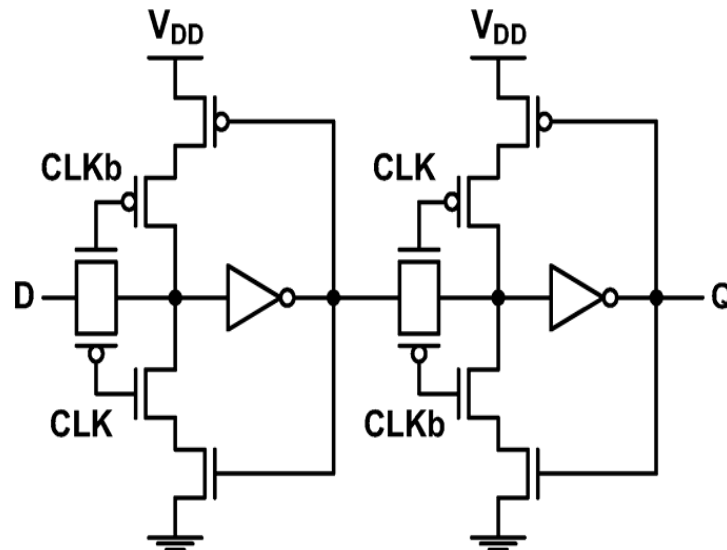


Figure5. circuit diagram of PPCFF

IV. PROPOSED SHIFT REGISTER

The proposed shift register(512 bits) is divided into M sub shift registers. Because of to reduce the number of delayed pulsed clock signals. A 4-bit sub shift register consists of five latches and also one temporary data element and also a pulsed clock generator.

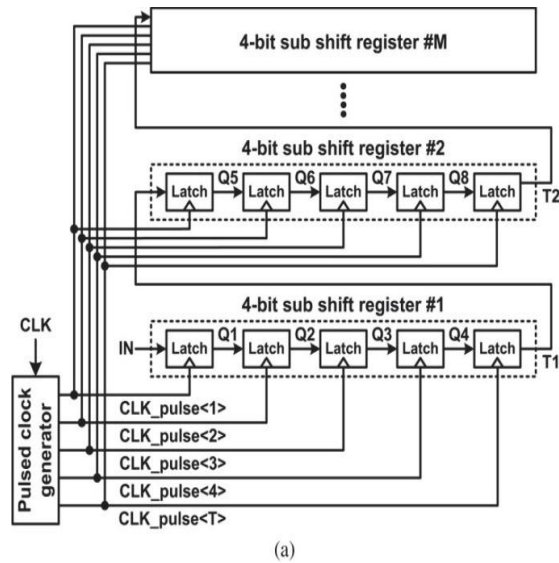


Figure 6. Proposed shift register

The five latches are performs a shift operations with five non-overlap delayed pulsed clock signals (CLK_pulse[1:4] and CLK_pulse[T]). In 4-bit sub shift register , four latches store 4-bit data(Q1-Q4) and the last latch stores 1-bit temporary data(T1) will stored in the first latch (Q5) of the 4-bit sub shift register #2. The input pulsed clock signal is giving to the latch IN and the output is given to the Q1. Until it performs to Q4 and then the output of Q4 is given to the next latch that is the input of the second sub shift register (Q5) here the data is stored. The pulsed latch update the latch data T1 from Q4. The pulsed clock signals clk pulse update the four latch data from Q4 to Q1 sequentially. The latches receive the data from their previous input. Like Q2-Q4 receive data from their previous latches Q1-Q3. But Q1 receives data from input of the shift register (IN).

Latches store the data as Q5 to Q8 and last latch as the data of T2. Until this process continuous to the 4-bit sub shift register #M. The proposed shift register reduces the number of delayed pulsed clock signals, but it increases the number of latches because of the additional temporary storage latches. In shift register every latch exist clock pulses in this the clock pulses are generated from the delayed pulsed clock generator in Figure 6.

V. SIMULATION RESULTS

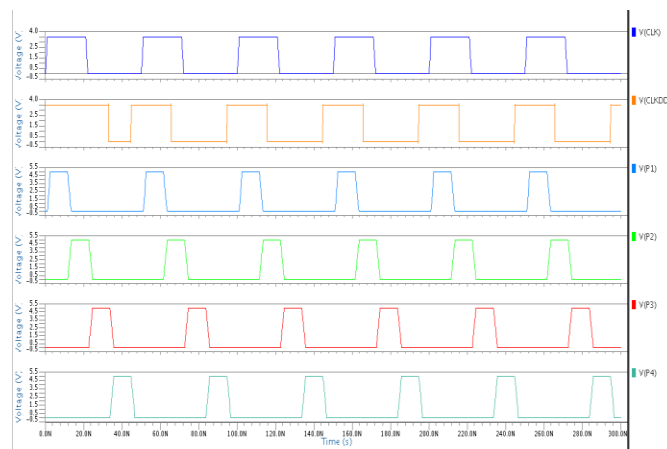


Figure 7.Pulse Clock generator

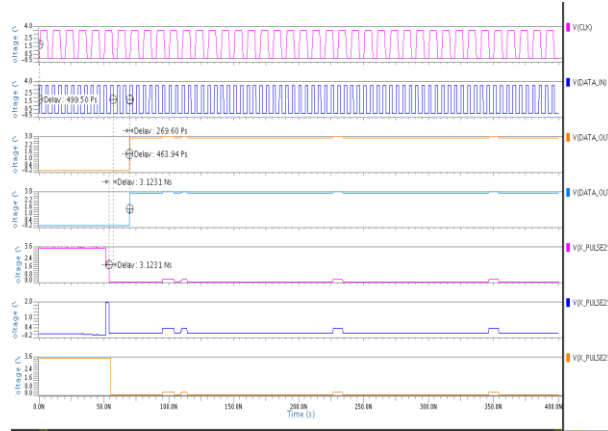


Figure 8. 256 bit shift register

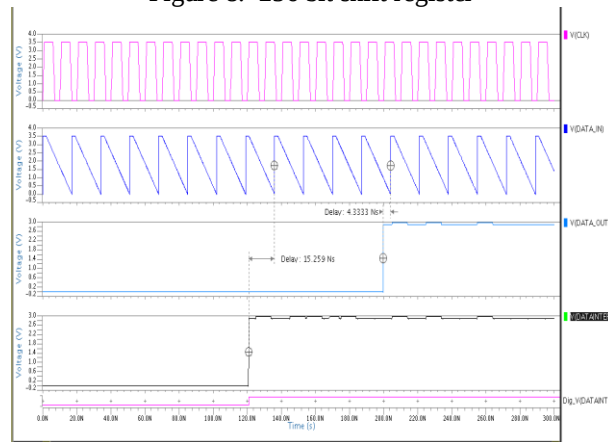


Figure 9. 512 bit shift register

VI. POWER CONSUMPTION

Number of bits	POWER
256 bit	431.25mW
512 bit	21.83mW

Table 1. Comparison of 256 bit and 512 bit

VII. CONCLUSION

This paper presents a low-power and area efficient shift register using pulsed latches. Compared to the existing system i.e, 256 bit shift register, the proposed system reduces power. The proposed shift register saves 70% power compared to conventional shift register with flip-flops.

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