

**Push-pull Front End Converter Based Bi-directional Inverter For Photovoltaic  
Rooftop System**Saurabh.B.Patel<sup>1</sup>, Prof. Vikash Verma<sup>2</sup><sup>1</sup>PG student at dept. of electrical engineering, Parul Institute of Engineering & Technology<sup>2</sup>Assistant Professor Dept. of Electrical Engineering, Parul Institute of Engineering & Technology

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**Abstract-** Photovoltaic (PV) residential power system is an important application of renewable energy. In this manuscript a soft-switching current fed push-pull front end converter based inverter is offered. push-pull converter has only two primary device with common ground to supply and result in straight forward and summary the gating requirement. The device voltage is clamped naturally by secondary modulation without active clamping circuit or passive snubber. zero current switching (ZCS) of primary device and zero voltage switching (ZVS) of secondary device is achieved. Soft switching is inherent remaining to anticipated secondary modulation load independent, and is maintained during wide variation of input voltage and power transfer capacity and suitable for PV application.

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**Keywords:-** Photovoltaic (PV) Residential Power System, Current-fed converter, Push-Pull DC-DC converter, soft-switching, ZCS/ZVS, Active-clamped, Matlab-Software.

**INTRODUCTION**

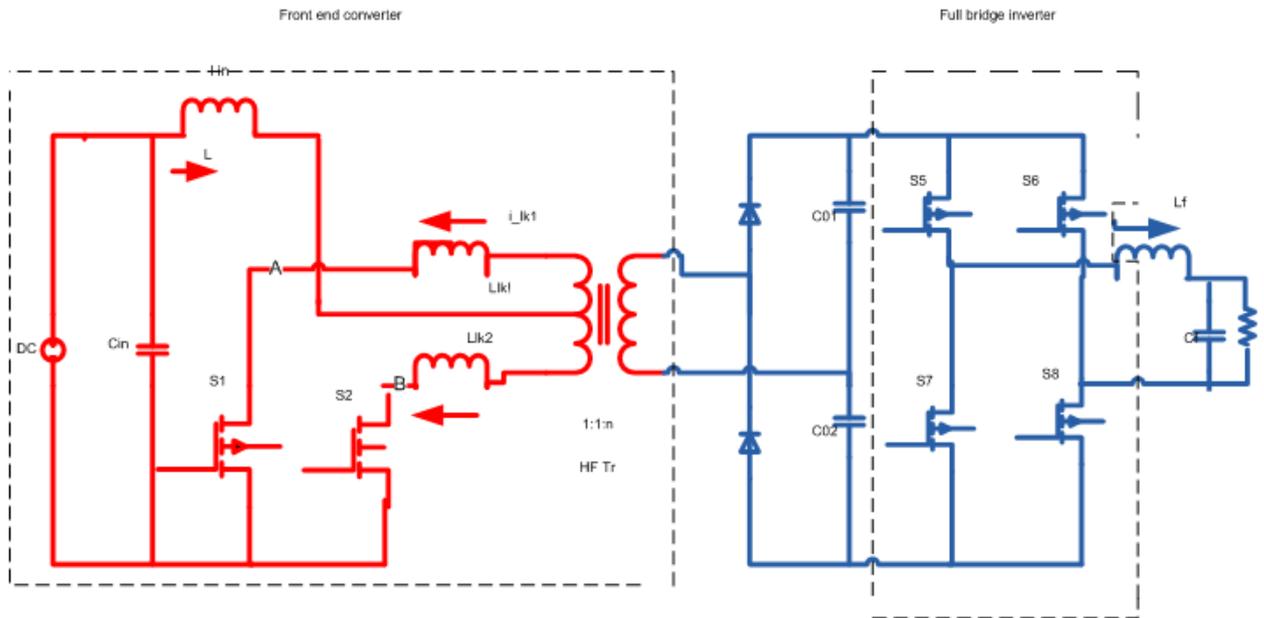
In the near future, the demand for electric energy is expected to increase rapidly due to the global population growth and industrialization. This rise in the energy demand requires electric utilities to increase their generation. Recent studies predict that the world's net electricity generation is expected to rise from 17.3 trillion kilowatt-hours in 2005 to 24.4 trillion kilowatt-hours (an increase of 41%) in 2015 and 33.3 trillion kilowatt-hours (an increase of 92.5%) in 2030. Currently, a large share of electricity is generated from fossil fuels, especially coal due to its low prices. However, the increasing use of fossil fuels accounts for a significant portion of environmental pollution and greenhouse gas emissions, which are considered the main reason behind the global warming. For example, the emissions of carbon dioxide and mercury are expected to increase by 35% and 8%, correspondingly, by the year 2020 due to the expected increase in electricity generation. Moreover, possible depletion of relic fuel reserves and unstable price of oil are two main concerns for industrialized countries. To overcome the problems associated with generation of electricity from fossil fuels, renewable energy sources can be participated in the energy mix.

There are many sources available for electricity generation, among all these sources solar has been very promising. The PV system will use the solar energy as the power source and transfer the power into the grid through conditioning by power electronics. So power electronics is an essential part of a PV system, and it is necessary to understand how to apply and control this part for optimization of the power generation.

The residential PV power system plays an increasing important role in solar renewable energy. However, PV modules have highly non-linear voltage-current characteristics and the maximum power point (MPP) varies dramatically with the ambient environmental factors such as solar irradiance and temperature. For residential applications, the performance of PV inverter system is easily to be affected by partial shadows and mismatch of electrical parameters. The configuration of PV modules and corresponding power electronics design are crucial to draw maximum power from PV modules. Generally, PV modules configurations are categorized into three classifications:

- 1) Centralized configuration
- 2) String/multi-string configurations,
- 3) Module integrated converter (MIC) configuration.

In conventional, centralized and string configuration of PV modules, a number of PV modules are connected in series to obtain sufficient dc-link voltage for inversion operation. However, the performance of entire series connected string of PV modules could be significantly impeded due to the module mismatch or partial shading. Building integrated PV systems with several different power configurations have been evaluated considering



**Fig.1 push-pull front endconverter based bi-directional inverter**

energy efficiency in AC module technology and PV dc-building-module (PVDCBM) based Technology are very much suitable for residential building integrated application for its outstanding anti-shading and anti-mismatch performances. In this paper, a dual stage dc/ac inverter as shown in Fig.1 is proposed that is composed of high step-up snubberless current-fed push-pull front-end converter and full-bridge inverter. Voltage doubler is used to reduce number of the switches and the transformer turns ratio. A novel secondary modulation technique is proposed to clamp the voltage across the primary side devices and therefore eliminates the necessity for snubbers. Switching losses are reduced significantly owing to ZCS of primary switches and ZVS of secondary switches. Soft-switching is inherent, load independent, and is continued with wide variation of input voltage and power, and thus is suitable for PV applications.

## II. DESIGN AND OPERATION OF CONVERTER

### 2.1 Design of the Converter

In this Section, converter design process is illustrated by a design example for the following specifications: input voltage  $V_{in}=12$  V, output voltage  $V_o = 150$  to  $300$  V, output power  $P_o=250$  W and switching frequency  $f_s = 100$  kHz. The design equations are presented to determine the components' ratings. It helps selection of the components as well as to predict the converter performance theoretically.

(1) Maximum voltage across the primary switches is,

$$V_{p, sw} = \frac{2 v_0}{n} \quad (1)$$

(2) Voltage conversion ratio or input and output voltages are related as,

$$V_0 = \frac{nV_{in}}{2(1-d)} \quad (2)$$

Where  $d$  is the duty cycle of primary switches. This equation is derived on the condition that anti-parallel diode conduction time (e.g. interval 6) is quite short and negligible with the intention to ensure ZCS of primary switches without significantly increasing the peak current. However, at light load condition of converter, and the anti-parallel diode conduction time is comparatively large, (1) is not valid any more. Due to the existence of longer anti-parallel diode conduction period, the output voltage is boosted to higher value than that of nominal boost converter

(3) Average input current is  $I_{in} = P_o / (\eta V_{in})$ . Assuming an ideal efficiency  $\eta$  of 95%,  $I_{in} = 21.9$  A.

(4) The selection of transformer turns-ratio is selected to maintain duty cycle  $d > 0.5$ . By using (1),

Therefore, maximum value of  $n = 12.5$  for  $V_{o,min} = 150V$ . Fig. 3 shows variation of total value of series inductances  $L_{lk\_T}(H)$  with respect to power transferring ability  $P(W)$  for four values of turnsratio. With the rise of turns-ratio, the value of  $L_{lk\_T}$  decreases. It is difficult to realize low leakage inductance with high turns-ratio. In addition, higher turns-ratio may lead to more transformer loss because of higher copper loss, higher eddy current from proximity effect and higher core loss due to larger size. However, increasing the turns-ratio can reduce the maximum voltage across the primary switches, which permits use of low voltage devices with low on-state resistance. Thus conduction losses in the primary side semiconductor devices can be suggestively reduced. An optimum turns ratio  $n = 10$ , duty ratio  $d = 0.8$  are selected to achieve an acceptable trade-off. Output voltage can be regulated from 150 V to 300 V by modulating the duty ratio from 0.6 to 0.8.

(5) Leakage inductance  $L_{lk\_T} = 22.2 \mu H$  for the given values. Here, series inductors  $L_{lk1}$  and  $L_{lk2}$  are chosen to be equal to  $L_{lk1} = L_{lk2} = 3.4 \mu H$ . Unable design of series inductors  $L_{lk1}$  and  $L_{lk2}$  is also allowable. Where  $V_{in} = 12V$ ,  $V_o = 300V$ ,  $n = 10$ ,  $P_o = 250W$ ,  $f_s = 100kHz$ ,  $I_{in} = 21.93A$ ,  $TDR/T_s = (n \cdot V_{in})/V_o = 0.2$  duty cycle = 0.85 for ZVS and 0.8 for proposed ZCS topology. The efficiency of the proposed converter is higher due to compact losses associated with clamp circuit and main primary switches.

## 2.2 Operation of Converter

For the sake of simplicity, the following assumptions are made to study the operation and explain the analysis of the converter:

- a) Boost inductor  $L$  is large enough to maintain constant current through it.
- b) All the components are ideal.
- c) Series inductors  $L_{lk1}$  and  $L_{lk2}$  include the leakage inductances of the transformer. The total value of  $L_{lk1}$  and  $L_{lk2}$  is represented as  $L_{lk\_T}$ .  $L_{lk}$  represents the equivalent series inductor reflected to the high voltage side.
- d) Magnetizing inductance of the transformer is infinitely large.

**Interval 1 ( $t_0 < t < t_1$ ):** In this mode of operation, primary side switch  $S_2$  and anti-parallel body diode  $D_3$  and  $D_6$  of the secondary side H bridge switch are conducting. Power is delivered to the load through HF transformer. The non-conducting secondary device  $S_4$  and  $S_5$  are blocking output voltage  $V_{DC}$  and the non-conducting primary device  $S_1$  is blocking reflected output voltage  $2V_o/n$ . The values of current through various components are:  $i_{S1} = 0$ ,  $i_{S2} = I_{in}$ ,  $i_{L_{lk1}} = 0$ ,  $i_{L_{lk2}} = I_{in}$ ,  $i_{D3,6} = I_{in}/n$ . Voltage across the switch  $S_1$ :  $V_{S1} = 2V_o/n$ . Voltage across the switch  $S_{4,5}$ :  $V_{S4,5} = V_{dc}$ .

**Interval 2 ( $t_1 < t < t_2$ ):** At  $t = t_1$ , primary switch  $S_1$  is turned-on. The corresponding snubber capacitor  $C_1$  discharges in a very short period of time. At the end of this interval,  $S_1$  is fully conducting and  $C_1$  is completely discharged.

**Interval 3 ( $t_2 < t < t_3$ ):** Now all two primary switches are conducting. Reflected output voltage appears across series inductors  $L_{lk1}$  and  $L_{lk2}$ , diverting/transferring the current through switch  $S_2$  to  $S_1$ . It causes current through previously conducting device  $S_2$  to reduce linearly. It also results in conduction of switch  $S_1$  with zero current which helps reducing associated turn-on loss. The currents through various components are given by.

$$i_{L_{lk1}} = i_{S1} = \frac{V_{DC}}{n L_{lk\_T}} (t - t_2) \quad (3)$$

$$i_{L_{lk2}} = i_{S2} = I_{in} - \frac{V_{DC}}{n L_{lk\_T}} (t - t_2) \quad (4)$$

$$i_{D3} = \frac{I_{in}}{n} - \frac{2V_{DC}}{n^2 L_{lk\_T}} (t - t_2) \quad (5)$$

Where  $L_{lk\_T} = L_{lk1} + L_{lk2}$ . Before the end of this interval  $t = t_3$ , the body diode  $D_3$  is conducting. Therefore  $S_3$  can be gated on for ZVS turn-on. At the end of this interval,  $D_3$  commutates naturally. Current through all primary devices reaches  $I_{in}/2$ . Final values are:  $i_{L_{lk1}} = i_{L_{lk2}} = I_{in}/2$ ,  $i_{S1} = i_{S2} = I_{in}/2$ ,  $i_{D3} = 0$ .

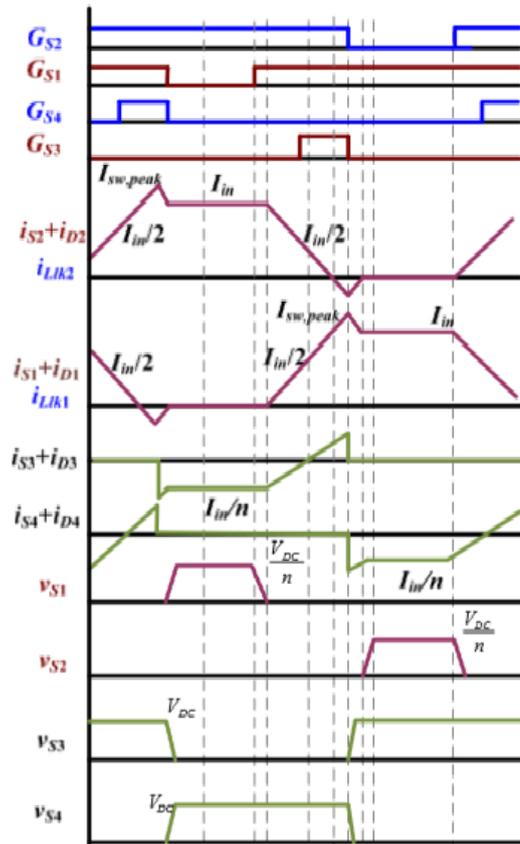


Fig.2 operating interval of high step-up current fed push-pull isolated dc/dc converter

**Interval 4 ( $t_3 < t < t_4$ ):** In this interval, secondary device  $S_3$  is turned-on with ZVS. Currents through all the switching devices continue increasing or decreasing with the same slope as interval 3. At the end of this interval, the primary device  $S_2$  commutates naturally with ZCS and the respective current  $i_{S2}$  reaches zero obtaining ZCS. The full current, i.e. input current is taken over by other device  $S_1$ . Final values are:  $i_{LLk1} = i_{S1} = I_{in}$ ,  $i_{LLk2} = i_{S2} = 0$ ,  $i_{S3,6} = I_{in/n}$ .

**Interval 5 ( $t_4 < t < t_5$ ):** In this interval, the leakage inductance current  $i_{LLk1}$  increases further with the same slope and anti-parallel body diode  $D_2$  starts conducting causing extended zero voltage appear across commutated switch  $S_2$  to ensure ZCS turn-off. Now, the secondary device  $S_{3,6}$  are turned-off. At the end of this interval, current through switch  $S_1$  reaches its peak value. This interval should be very short to limit the peak current though the transformer and switch reducing the current stress and kVA ratings. The currents through operating components are given by

**Interval 6 ( $t_5 < t < t_6$ ):** During this interval, secondary switch  $S_3$  is turned-off. Anti-parallel body diode of switch  $S_4$  takes over the current immediately. Therefore, the voltage across the transformer primary reverses polarity. The current through the switch  $S_1$  and body diodes  $D_2$  also start decreasing. The currents through operating components are given by

At the end of this interval, current through  $D_2$  reduce to zero and is commutated naturally. Current through  $S_1$  reaches  $I_{in}$ . Final values:  $i_{LLk1} = i_{S1} = I_{in}$ ,  $i_{LLk2} = i_{D2} = 0$ ,  $i_{D4} = I_{in/n}$ .

**Interval 7 ( $t_6 < t < t_7$ ):** In this interval, snubber capacitor  $C_2$  charges to  $V_{DC}/n$  in a short period of time. Switch  $S_2$  is in forward blocking mode now.

**Interval 8 ( $t_7 < t < t_8$ ):** In this interval, currents through  $S_1$  and transformer are constant at input current  $I_{in}$ . Current through anti-parallel body diode of the secondary switch  $D_4$  is  $I_{in}/n$ . The final values are:  $i_{LLk1} = i_{S1} = I_{in}$ ,  $i_{LLk2} = i_{S2} = 0$ ,  $i_{D4} = I_{in/n}$ . Voltage across the switch  $S_2$   $V_{S2} = V_o/n$ . In this half HF cycle, current has transferred from switch  $S_2$  to  $S_1$ , and the transformer current has reversed its polarity.

### 2.3 simulation result

Proposed converter has been simulated using software MATLAB. Simulation results for input voltage  $V_{in} = 12$  V, output voltage  $V_{out} = 200$ V, output power  $P_o = 250$ W, device switching frequency  $f_s = 100$  kHz are illustrated in Fig. 4. Simulation results coincide closely with theoretically predicted waveforms. It verifies the steady-state operation and analysis of the converter presented in Section 2.1. Waveforms of current through the input inductor  $L$  and voltage  $V_{sec}$  are shown in Fig. 4.

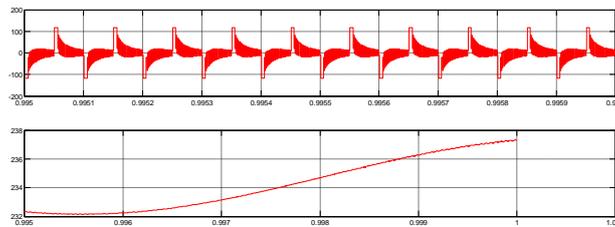


Fig. 3(a) o/p voltage of secondary transformer and o/p of voltage doubler

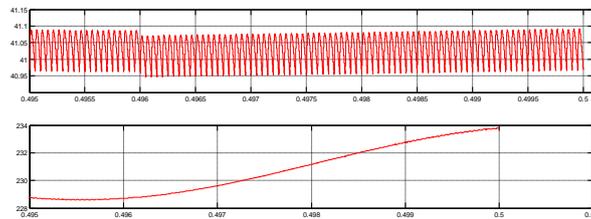


Fig.3(b)input voltage of PV panel and I/P voltage of inverter

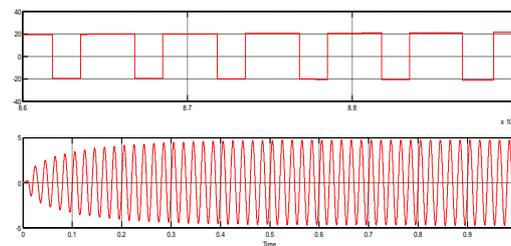


fig.3(c) output voltage and current without filters

### CONCLUSION

This paper proposes a two-stage single-phase inverter consisting of novel high step-up current-fed push-pull front-end converter followed by full-bridge inverter for the PV residential application. Push-pull topology with voltage doubler configuration reduces the number of the switches. The conventional current fed push-pull converter circuit has the major problem of voltage overshoot across the semiconductor devices at turn-off. Therefore, voltage clamping or snubber circuits are employed to limit the device voltage. The proposed innovative secondary modulation achieves the soft-switching of all semiconductor devices (ZCS of primary side and ZVS of secondary devices) without modifying the topology. It solves the basic problem of device turn-off in current-fed converter and is absolutely new and innovative. Proposed modulation achieves zero current commutation and natural voltage clamping of the devices without snubber or any auxiliary circuit.

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