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IMPLEMENTATION OF 24 BIT HIGH SPEED FLOATING POINT VEDIC MULTIPLIER

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Abstract-*The computational complexity of various data processing applications is vastly reduced when signals are represented in the frequency domain. In launch vehicle systems, FFT is required for telemetry data processing applications. Since the systems work in real time, a fast and efficient computation of the FFT is called for. FFT multiplication deals with Floating point numbers. Vedic mathematics is an ancient multiplication procedure which is widely used in every field that requires computations. The Urdhva Tiryakbhyam sutra is used because it will reduce computation time than conventional multipliers. Digital Signal Processing applications essentially require the multiplication of binary floating point numbers. For IEEE754 floating point multiplier implementation, Vedic Multiplication Method is used. The ease of multiplication of Mantissa part is done by Urdhva Tiryakbhyam method. This paper deals with the 24 bit floating point implementation using IEEE754 multiplication based on vedic mathematics and compare the result with conventional multi plier. Design and HDL coding was carried out using Verilog using the Libero IdeV9.1 project environment, natively used for the Actel Pro-Asic devices. The code synthesis was done using Synplify and simulation stage was done using Modelsim.*

Keywords- *Fast Fourier Transform, Urdhava-Tiryakbhyam, Vedic Mathematics, Libero Ide V9.1, Modelsim.*

I INTRODUCTION

Nowadays the computational complexity of various data processing applications is vastly reduced when signals are represented in the frequency domain. Fourier Transform analysis transforms a signal from its original domain to a representation in frequency domain and vice versa. Fast Fourier Transform [FFT] algorithm efficiently computes the DFT by factorizing the DFT matrix into a product of zero factors, and thereby reducing the computational complexity to 0[n logn]. Fast Fourier transforms are globally used for various application fields in engineering, communication, and mathematics. Nowadays, every process should be rapid and efficient. Fast Fourier transform is an effective algorithm to calculate the 'n' point DFT. Even though this algorithm has large range of applications in communication, signal and image processing, its Implementation needs great number of complex multiplication steps. So for our convenience and make the whole method simple and delay free, we need an efficient multiplier. To overcome this problem Urdhva Tirvagbhyam sutra (UT Sutra) is considered as an efficient method of multiplication [1].The most widely used standard for Binary floating point computation is the Binary Floating Point IEEE754 Standard. Floating-point fixes a number of representation problems. Fixed point is restricted to a fixed limit which restricts it from representing very large or small numbers. Also when two large numbers are divided, a fixed point is exposed to loss of precision. Vedic mathematics mentioned on ancestral Indian Vedas gives a different multiplication algorithm to carry out fast multiplication. The Sutras Urdhava-Tiryakbhyam and Nikilam Sutras give easiest way of mental calculation when performing multiplication. Among these 2 sutras, Urdhava- Tiryakbhyam employs parallel multiplication and exhibits high degree of parallelism compared to other parallel multipliers.

This paper deals with the implementation of 24bit High speed floating point Vedic multiplier based on Urdhva Tiryakabhya sutra. The advantages of Vedic Multiplication over the conventional multiplication techniques are discussed.

II. ARCHITECTURE OF THE SYSTEM

A. **Vedic mathematics**[2] is the name given to the old system of mathematics which was find out from the "Vedas".Because of the easiness of vedic multiplication over conventional method, it can be easily adopted to practical situations. Swami Bharati Krishna Tirthaji Maharaj (1884- 1960), re-introduced the concept of ancient system of Vedic mathematics. The word 'Vedic' is derived from the word 'Veda' which means the storing house of all knowledge. The Sutrams Urdhava- Tiryakbhyam and Nikilam Sutrams give easiest way of mental calculation when performing multiplication. Vedic Mathematics is a domain which gives various effective algorithms which can be applicable to various branches of Engineering such as digital signal processing and computing. The number of logic levels and logic

delay is being reduced using the Urdhva- Tiryakbhyam sutra. Vedic mathematics is a mental calculation method that provides worldwide acceptance because of its easiness and advantages.

B. The word **"Urdhva-Tiryakbhyam"** means "Vertically- crosswise" in Sanskrit. This multiplication method can be applied to all cases of algorithm for N bit numbers. Urdhava-Tiryakbhyam [UT Sutra] employs parallel multiplication and exhibits high degree of parallelism compared to other parallel multipliers. In conventional parallel multiplication method partial products get summed up after the generation of all partial products. In the case of Urdhava-Tiryakbhyam, multiplication vertically and crosswise means summation will takes place just after partial products for a column gets generated. This high degree parallelism gives better speed compared to other parallel multiplication.

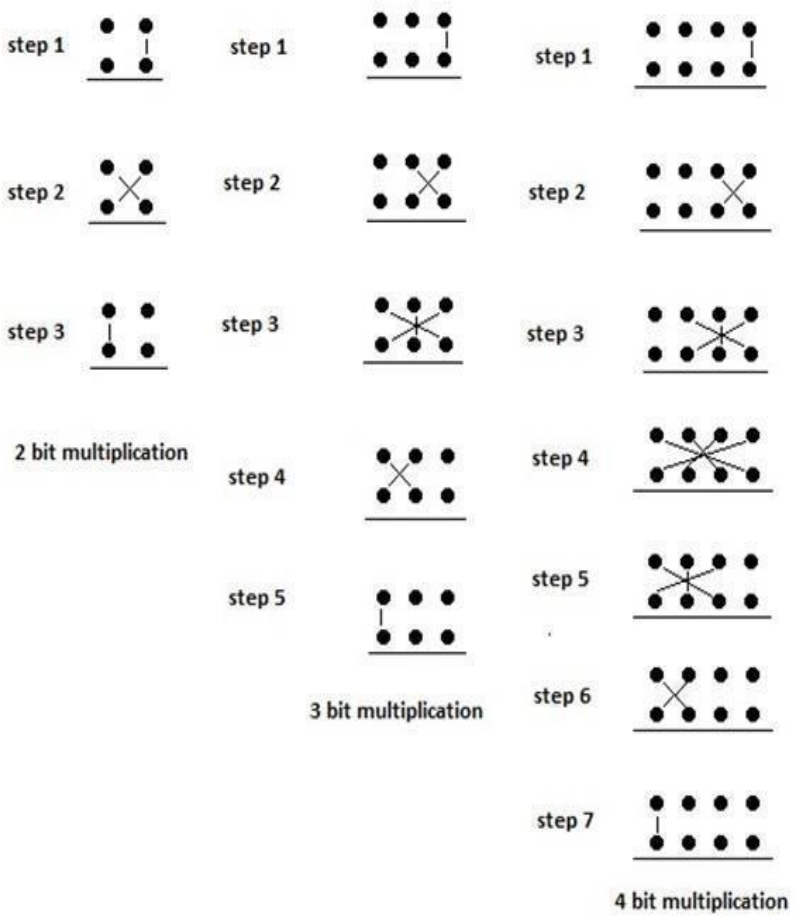


Fig 1 Line diagram of UT Sutra

Implementation of fast vedic multiplier will improve the performance of the current processors. Figure 1 shows the line diagram of UT sutra. This Sutram shows how to multiply a large bit [N x N, of N bits] by breaking it into smaller numbers of size (N/2 = n, say) and these smaller numbers can again be broken into smaller numbers (n/2 each) till we reach multiplicand size of (2 x 2) Thus, the entire multiplication process is simplified [3] and is shown in figure 2.

C. **Floating point multiplication**: For DSP applications, IEEE 754 floating point standard is widely used today. The IEEE [Institute of Electrical and Electronics Engineers] defines a Standard for floating-point representation and arithmetic. This IEEE754 standard is the widely accepted representation for floating numbers even though there are many other representations [5].Consider a floating point number - 2.42 *103. The '-' symbol indicates the sign component of the number, the '242' indicates the significant digits of the number and atlast the '3' indicates the scalar factor component of the number. The significand digits is termed as the *mantissa* of the number and scalar factor is called as *exponent* of the number. The general representation format is of the following and is shown in figure 3:

(-1) S* M * 2E (1)

Where, S - Sign bit.
M - Mantissa bit
E - Exponent bit

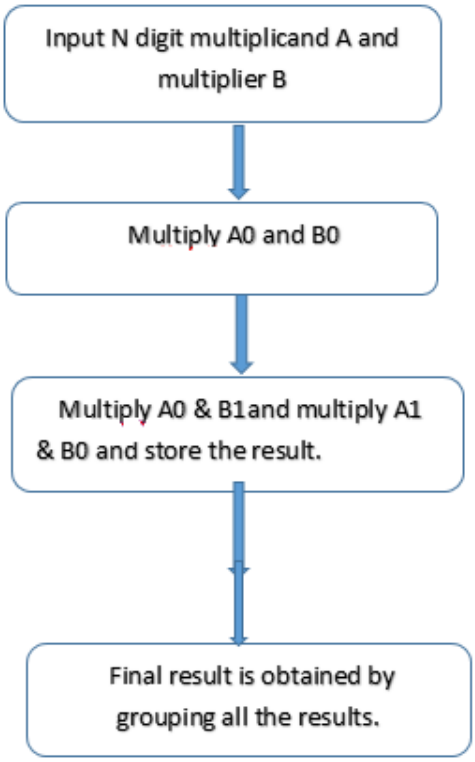


Fig 2 Vedic Multiplier Flowchart

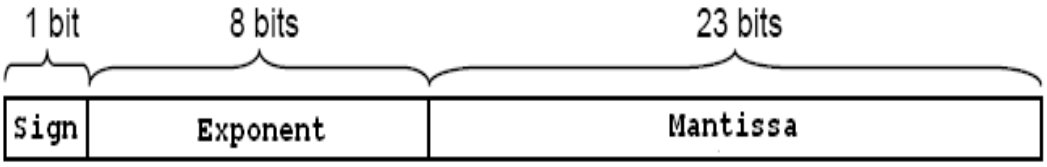


Fig 3 IEEE-754 Single Precision Floating Point Pattern.

III DESIGN STEPS OF SINGLE PRECISION FLOATING POINT MULTIPLIER

In this paper a Single precision floating point multiplier which can handle over flow, under flow and rounding of the result are designed. Fig 4 shows the multiplier structure that includes the addition of exponents, multiplication of mantissa, and sign calculation.

A. Floating Point Multiplication Algorithm

Multiplication of two floating point binary digits represented in IEEE 754 format is interpreted as:

$$V = (-1)^{Sign} * 2^{(exponent - bias)} * 1.fraction$$

The steps for multiplying two floating point number is given below:

1. Multiply 2 significand bits; i.e. (1.M1*1.M2).
2. Place a decimal point in the result.
3. Add the exponent bits; i.e. (E1 + E2 – *Bias*).
4. For obtain the sign bits, do XOR of 2 bits; i.e. s1 xor s2.
5. Do Normalization of the result; i.e. obtaining 1 at the MSB of the result.
6. Truncating the results to fit in the available bits.
7. Checking the underflow and overflow cases.

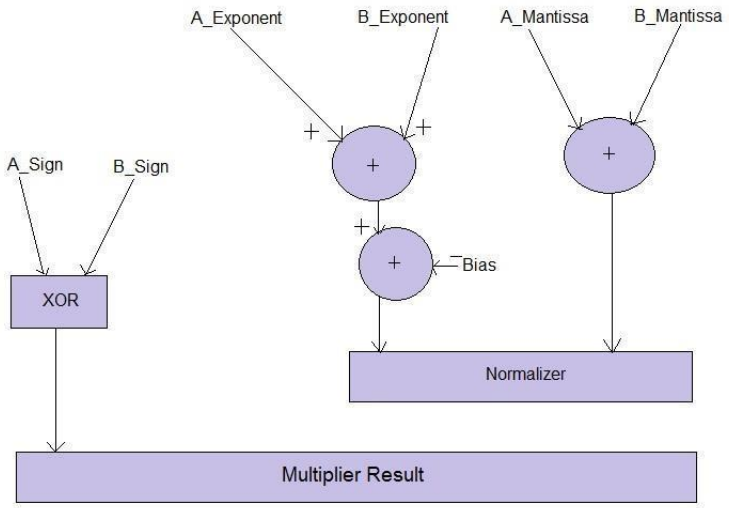


Fig 4 Floating point multiplier diagram

IV PROPOSED VEDIC MULTIPLIER

The proposed design uses vedic mathematics based on Urdhva Tiryakabhyam sutra for the multiplication of the mantissa part in IEEE 754 single precision floating point multiplication. In this proposed multiplier the base block used as first stage implementation is 3*3 block which is shown in figure 5. Here we needs 24bit vedic multiplier for the multiplication of mantissa part.

The 3*3 block consists of two half adders, one full adder and three 2 bit adders as shown in figure 5.

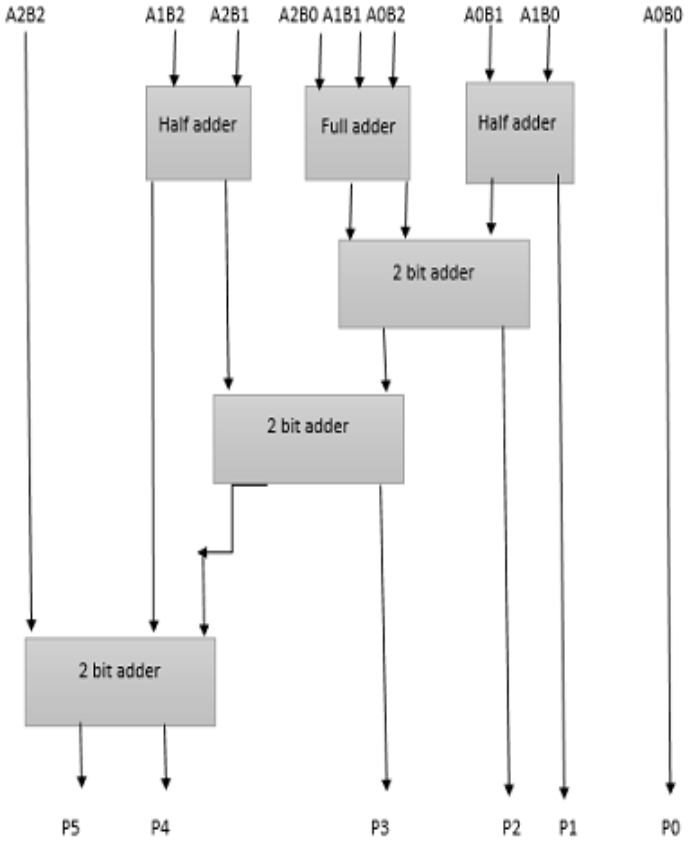


Fig 5 Hardware implementation of 3*3 block

From this 3*3 block, 6*6 multiplier block is designed and is shown in figure 6.

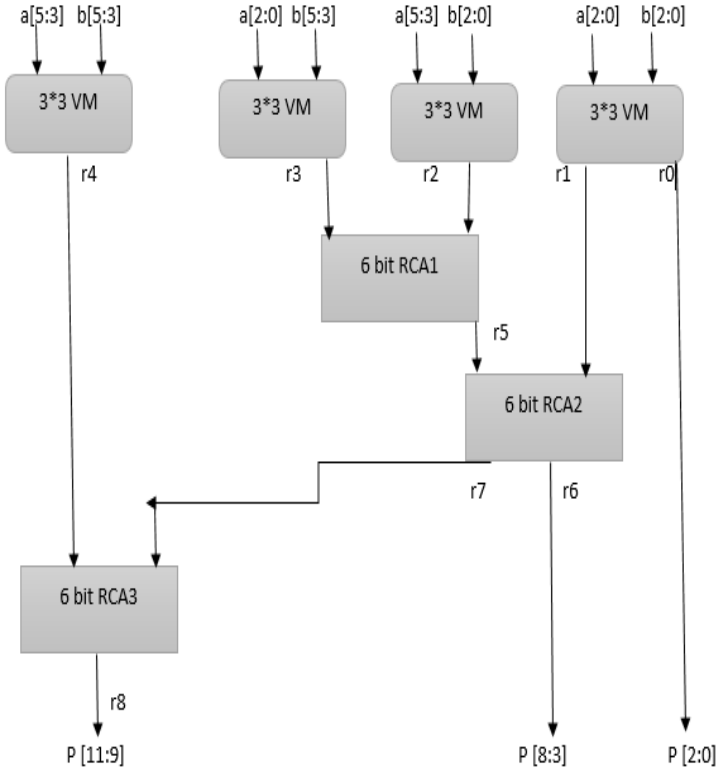


Fig 6 Proposed 6*6 bit VM

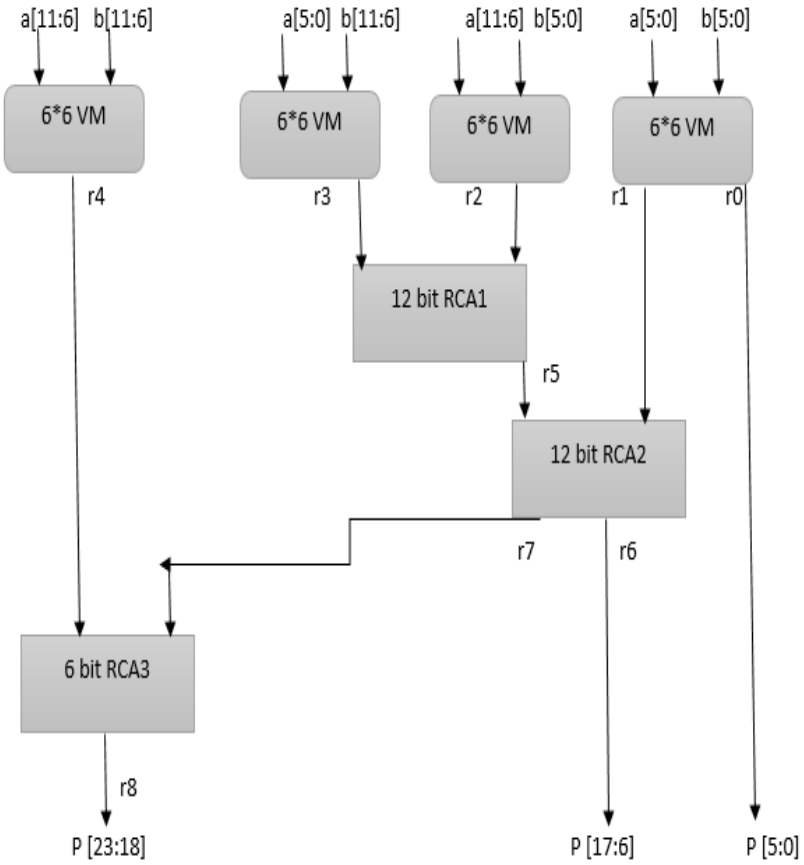


Fig 7 Proposed 12*12 bit VM

From this 6*6 multiplier block, 12*12 multiplier block is designed and similarly from this 12*12 multiplier block, 24*24 multiplier block is designed and implemented and are shown in figure 7 and 8 respectively. These blocks require vedic multipliers and ripple carry adders for getting the final output.

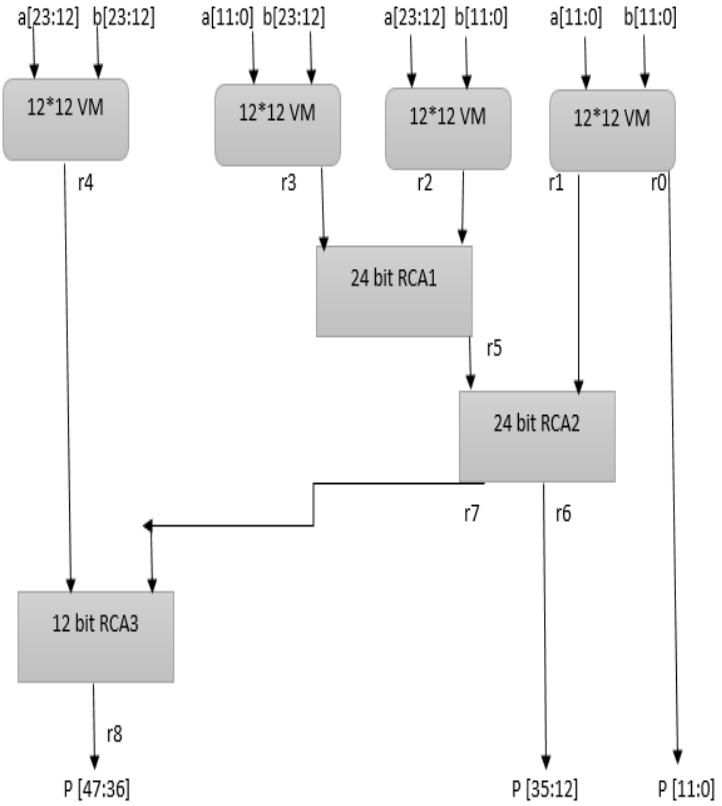
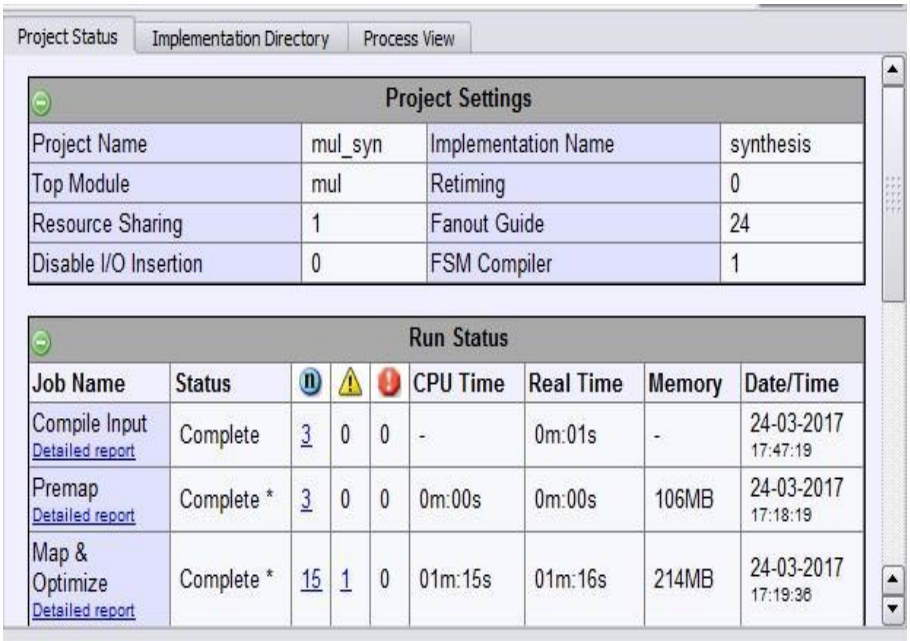


Fig 8 Proposed 24*24 bit VM

V RESULTS

The implementation of IEEE754 multiplication using conventional multiplication method and vedic multiplication using Urdhva-Tiryakabhyam method is performed and different parameters like CPU speed, memory utilization, area, estimated frequency is compared and analyzed. From the results shown below, we can find that the parameters like area, memory, CPU speed consumed by vedic multiplication technique is less than the conventional technique.



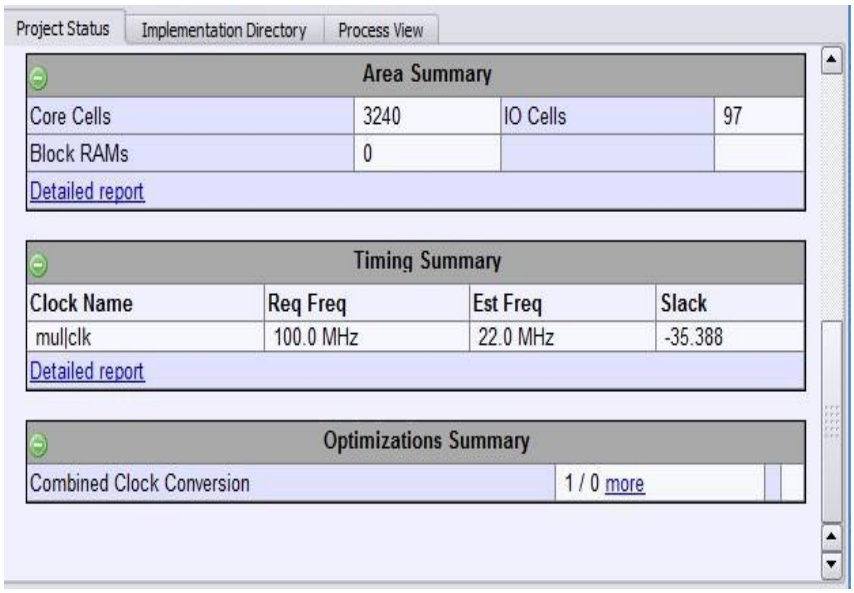


Fig 9 Synthesis result of 24bit ieee754 multiplication using conventional multiplier.

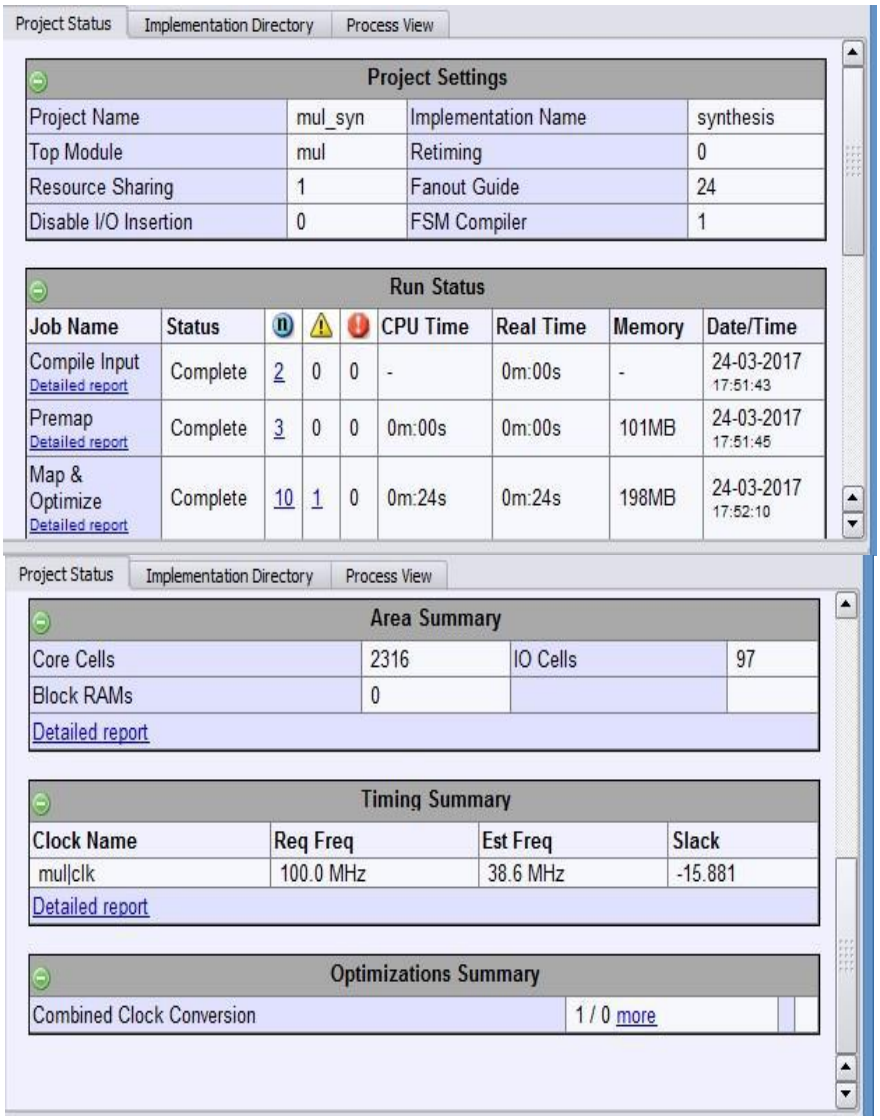


Fig 10 Synthesis result of 24bit ieee754 multiplication using UT sutra

Sl No:	Parameters of comparison	Conventional Multiplier	Vedic Multiplier
1	CPU time	1m:15s	0m:24s
2	Memory Usage	214 MB	198 MB
3	Cell Usage	3240	2316
4	Timing Summary	-35.388	-15.881

Fig 11 Comparison between conventional & vedic multiplier

VI CONCLUSION

This paper deals with the implementation of 24 bit High speed floating point Vedic multiplier for FFT computation. The advantages of Vedic Multiplication over the conventional multiplication techniques are discussed. The comparison between both techniques is shown in the result. From the result we can find that the parameters like area, memory, CPU speed consumed by vedic multiplication technique is less than the conventional technique. The performance is improved by using carry save adder or ripple carry adder at the addition part. This will be done as future work.

The proposed vedic multiplication method is entirely different from conventional multiplication design. Here larger blocks are designed from the smaller blocks. The design and implementation difficulties for inputs of large number is decreased and modularity is increased. This will help in designing FFT structure. An FFT circuit has been described that provides the high performance with Small area which has wide range of applications in communication, signal and image processing. Urdhva Tiryakbhyam from Vedic Mathematics is a general multiplication formula that can be equally applied to all cases of multiplication. The conventional multiplication method needs more time & area on hardware than Vedic multiplication techniques. The most important matter is that performance speed is increased by increase in length of bit.

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