Scientific Journal of Impact Factor (SJIF): 5.71

e-ISSN (O): 2348-4470
p-ISSN (P): 2348-6406

International Journal of Advance Engineering and Research Development

Volume 5, Issue 02, February -2018

Review of Low Powered High Speed and Area Efficient Full Adders

R.Senthil Ganesh[1], K.Hemamalini[2], V.Indhu[3], S. Kamala Prabha[4]

[1]*Assistant Professor, Electronics and Communication Engineering, Info Institute of Engineering, Tamilnadu.*
[2,3,4]*UG Scholar, Electronics and Communication Engineering, Info Institute of Engineering,Tamilnadu.*

Abstract— *Adders are the basic building block of all digital systems. Addition is the basic operation performed in all arithmetic operations. Addition is the important operation in arithmetic operation because all the other operations are done using addition. Developing technology is in need of the high performance and low power digital circuits. In order to achieve that we should increase the performance and reduce the power consumption of full adder. Here the comparative analysis of speed, average power consumption, static power dissipation, Power Delay Product [PDP] of various full adders such as full adder 9A, full adder 9B, 10T full adder, 10T adder 1,13A full adder, Gate Diffusion Input [GDI], modified full adder 9A, modified full adder 9B, Static Energy Recovery Full Adder [SERF] and the conventional 28T full adder was performed.*

Keywords *— PDP, Full Adders, GDI, SERF*

I. INTRODUCTION

The combinational circuit that adds two bits is called as half adder. A full adder is the one that adds three bits. The full adder is designed by the combination of two half adders. The addition is the fundamental operation in multiplication, division and subtraction [13]. The delay in any full adder will reduce the performance of any processor. The driving capability and the transistor count are some of the important factors to be concentrated in the design of any full adder. Additional buffers can be used if the driving ability gets lags but this will lead to the additional power consumption which will reduce the system efficiency. Adders are calculated for much number representation like binary coded decimal or excess. The adders mostly works on binary numbers. Adders are not only used for addition they are also used for other operations in processor like calculating the address, increment and decrement operators and also for other simple operations. Full adders are used in all digital circuits because it is easy to build a long chain of full adders and in that some full adders are used for addition, some for subtraction, some for multiplication and some for division.

Several researches have been made over the last decades to reduce power consumption, silicon area, and transistor count and to increase the speed and efficiency of the full adders. In this paper we have compared delay, PDP, transistor count of various full adders. ***Table 1 e***xplains truth table and***Figure 1***is the basic block diagram of full adder designs, Section III compares various full adder designs and Section IV briefs the conclusion.

Input			Output	
A	B	Cin	Sum	Carry
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

Table 1. Truth Table of Full Adder

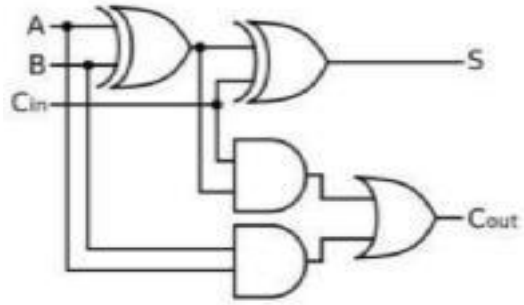

Figure 1. Basic Block Diagram of Full Adder

II. FULL ADDERS DESIGNS

A. Conventional 28T Full Adder

The conventional CMOS adder consist of large number of transistors. It is not area efficient with large fan-in's, so the power consumption will be high because it having more number of PMOS in the pull up network. So input capacitance will be very high, this causes high delay. It is having high input noise and the main advantage of this adder is that it will operate at low voltages [1]. Full swing outputs are produced because of pull up and pull down network in the circuit [2]. The PMOS block in the static CMOS circuit is the main disadvantage of the circuit because it has low mobility when compared to the NMOS. Hence it is needed to be sized up to get good performance [3].

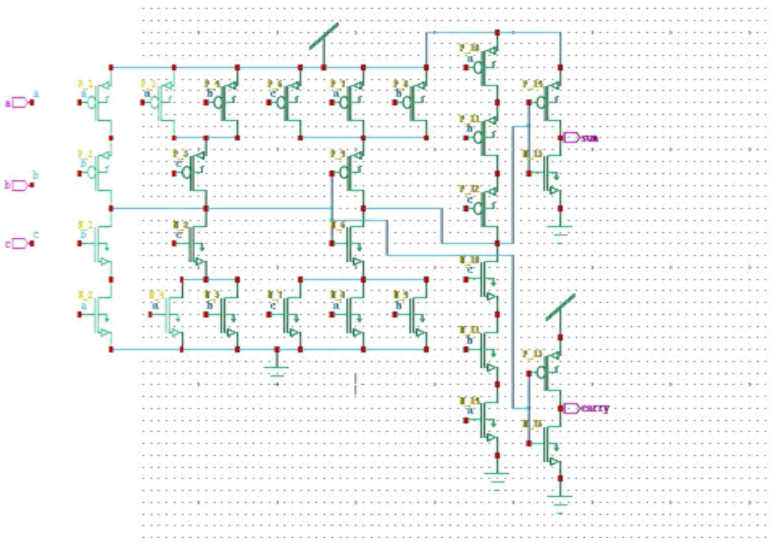

Figure 2. Conventional 28T Full Adder

B. Full Adder 9A and 9B

Sum is calculated by cascading the Static energy recovery X-NOR with the groundless X-NOR and the C_{OUT} is calculated by multiplexing B and C_{IN} controlled by A X-NOR B. These adders will consume less power at high frequencies and it works at high speed as compared to conventional 28T full adder and 10 transistor circuits [1]. In full adder 9B it resembles the inverter based X-OR as in the full adder 9A but the difference is that the V_{DD} connection in the inverter based X-OR is connected to input A. Since the new X-OR gate has no power supply. It is called as groundless X-OR and a new X-NOR gate is named as groundless X-NOR [4].

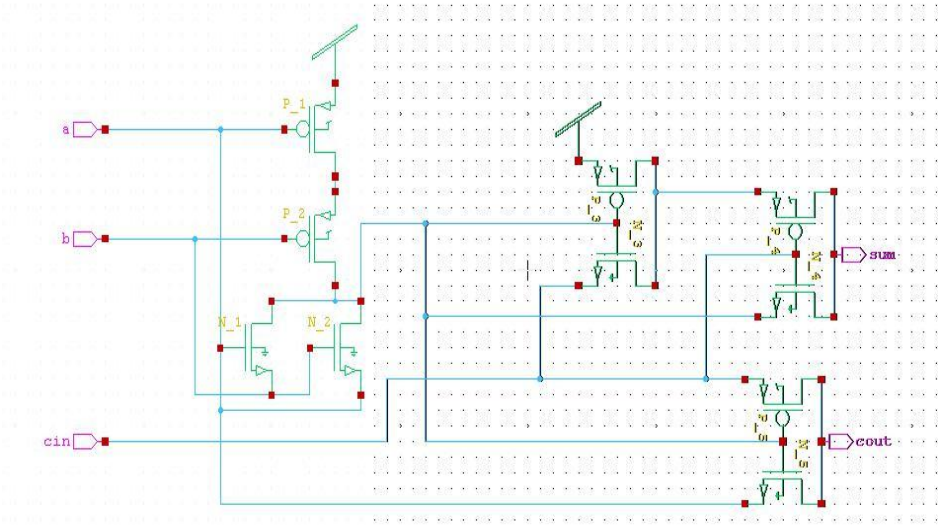

Figure 3. Full Adder 9A

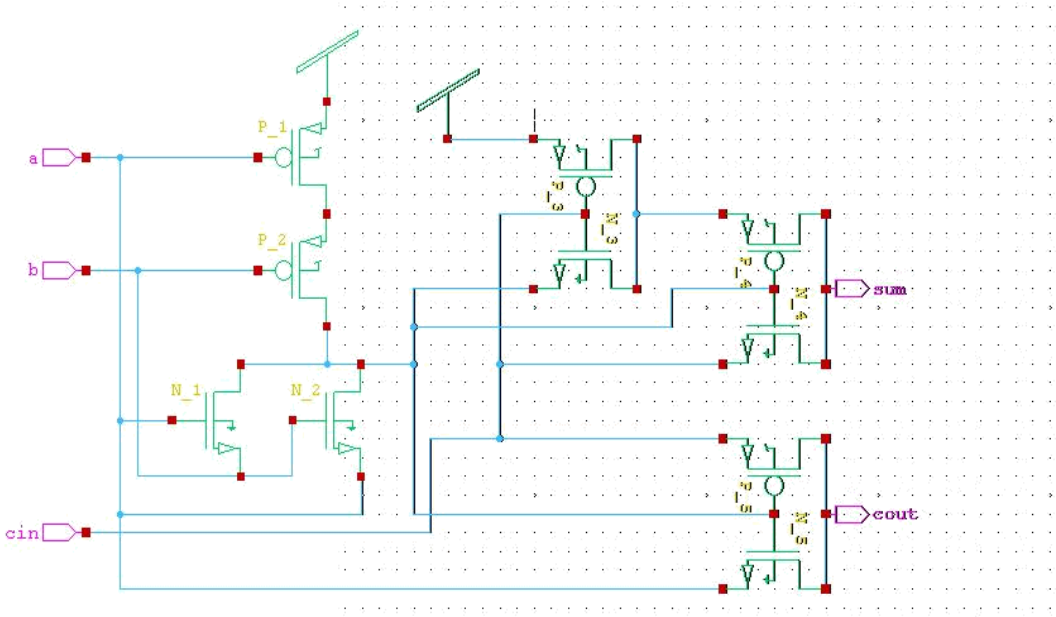

Figure 4. Full Adder 9B

C. 13A Full Adder

It is constructed using SER [Static Energy Recovery] X-NOR and Inverted X-NOR and C_{OUT} is designed using multiplexer. The average power in this will be in terms of Nano watts. The advantage is that it having better delay and low power compared to 10 transistors, SERF full adders in all loading conditions [4]. The main disadvantage is that it having double threshold losses, so the speed of operation is low. These problems restrict the full adder from operating in low voltages or cascading with extra buffering. The average power and static power dissipation are in the range of Nano watts [9].

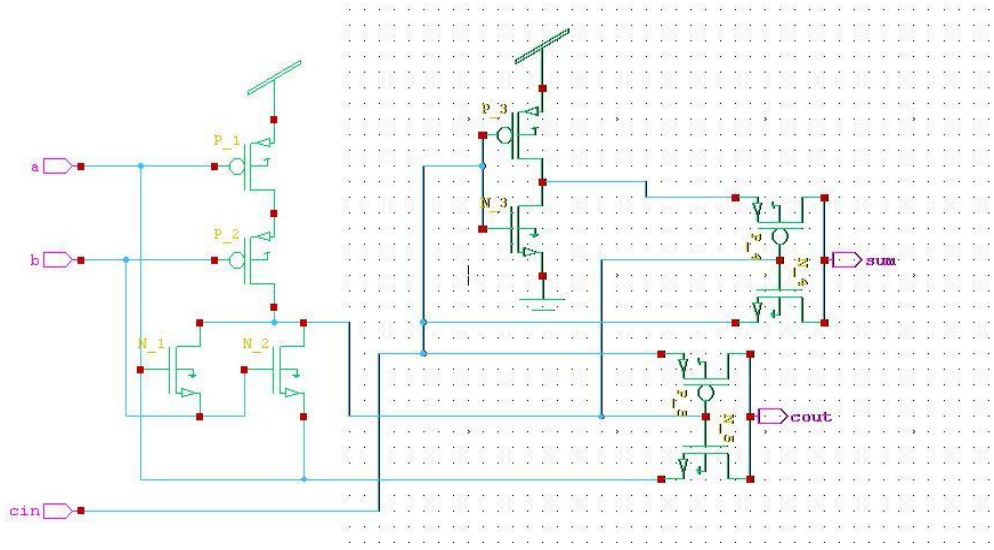

Figure 5. 13A Full Adder

D. SERF Adder

The important fact about this design is that the energy recovery logic reuses its charge, so the power consumption will be less. There is no direct path to ground and hence the power dissipation is also decreased. The charge stored in the load capacitance is reapplied to control gates, due to these effects it became more energy efficient. But the main disadvantage is that it does not provide full swing for internal nodes, so the power consumption is more and the circuit becomes slower. The design also had multiple threshold problems, so that it cannot be cascaded at low power supply. The circuit consists of two X-NOR and sum is calculated from the output of the second stage of the X-NOR circuit. The C_{OUT} can be calculated by multiplexing A and C_{IN} controlled by A X-OR B. When both the inputs A and B are equal to zero the capacitor is charged by V_{DD}, in the next stage B reaches a high voltage, keeping A at low voltage, the power discharge through A but some charges retained in A, so when A reaches a high voltage we need not to charge it fully so the energy consumption is less. [5]

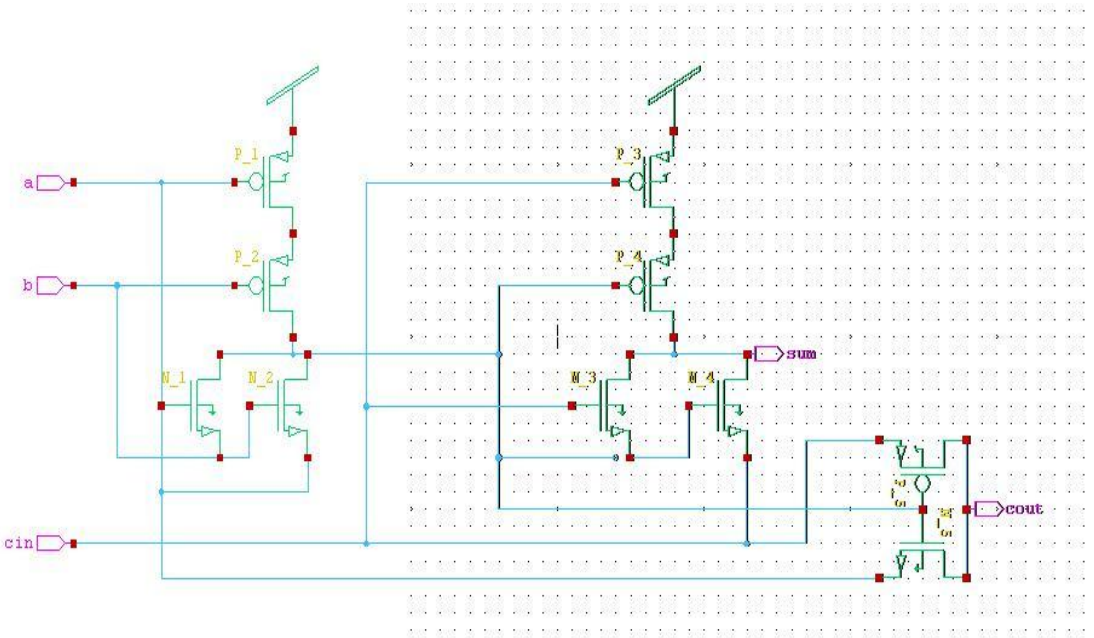

Figure 6. SERF Adder

E. Gate Diffusion Input [GDI] Adder

The design has 3 inputs namely G, P, and N, G→common state input for PMOS and NMOS, P→input to the source or drain of PMOS and N→input to the source or drain of NMOS [6]. When V_{DD} =1, without having swing drop from previous stage, GDI functions as an inverted buffer and will recover the voltage swing. This feature will make it for a self-swing restoration. The advantage of this design is that it consumes low power and provides high performance. These features will give extra two input to use which makes it flexible than the usual CMOS design ,this feature make it more power efficient without using large number of transistors. The main disadvantage of GDI is that it requires twin well CMOS or silicon on insulator process for realization, but it is more expensive [5].

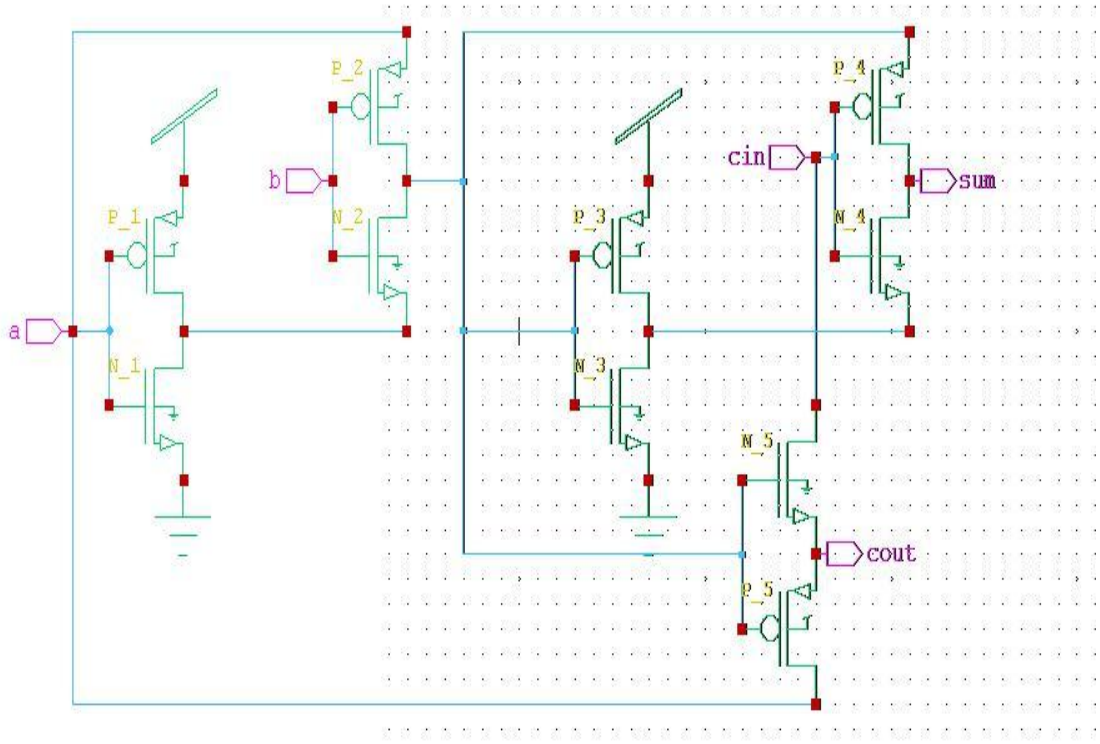

Figure 7. Gate Diffusion Input [GDI] based Adder

F. Modified Full Adder 9A and Full Adder 9B

The circuit consists of 3 X-OR (or) 3 X-NOR with 2X1 multiplexer where the 3X1 X-NOR is used to control the 2X1 multiplexer whose output is the C_{OUT} of the full adder is used to control the output. The second 2X1 multiplexer is controlled by input carry whose output is the sum output of the full adder. The design showed high speed, low power and low static power dissipation in terms of Nano watts. The delay and average power of the modified full adder 9A and full adder 9B are less when compared to full adder 9A and full adder 9B. The overall power delay product of this modified full adder 9A is improved from 52% to 72% at 1.8V supply and for modified full adder 9B the power delay product is improved from 72% to 82% at 1.8V supply[10].

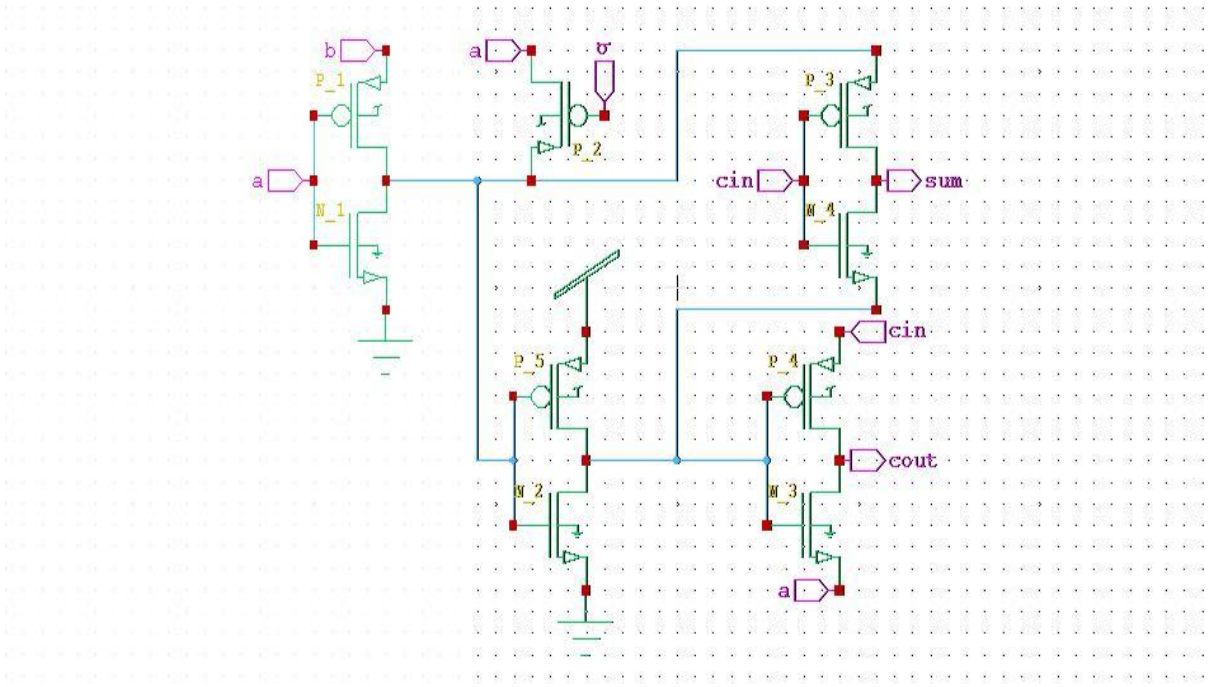

Figure 8. Modified Full Adder 9A

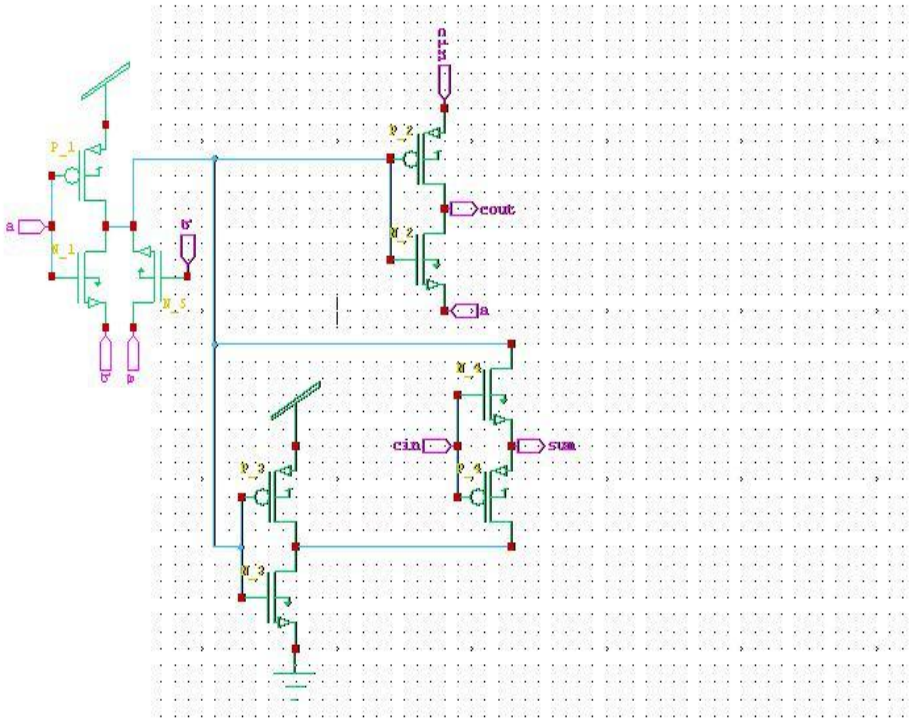

Figure 9. Modified Full Adder 9B

G. 10T Full Adder

The design uses hybrid logic design style. It consumes less power, area and small delay. It is difficult to maintain the full output voltage swing because it is having only few number of transistors. The output voltage swing gets reduced because of threshold losses. They suffer from threshold voltage problems because of few numbers of transistors [7]. The main disadvantage is that it having high capacitance at the input. The circuit design is implemented by using two X-OR gate and one 2X1 multiplexer is used. The design is implemented by two X-OR operations for sum and 2X1 multiplexer are used for calculating C_{OUT}. The C_{OUT} delay is reduced by giving negative bias at the body terminal of the 2X1 multiplexer that makes the transistor to work faster.This leads to faster operation [8].

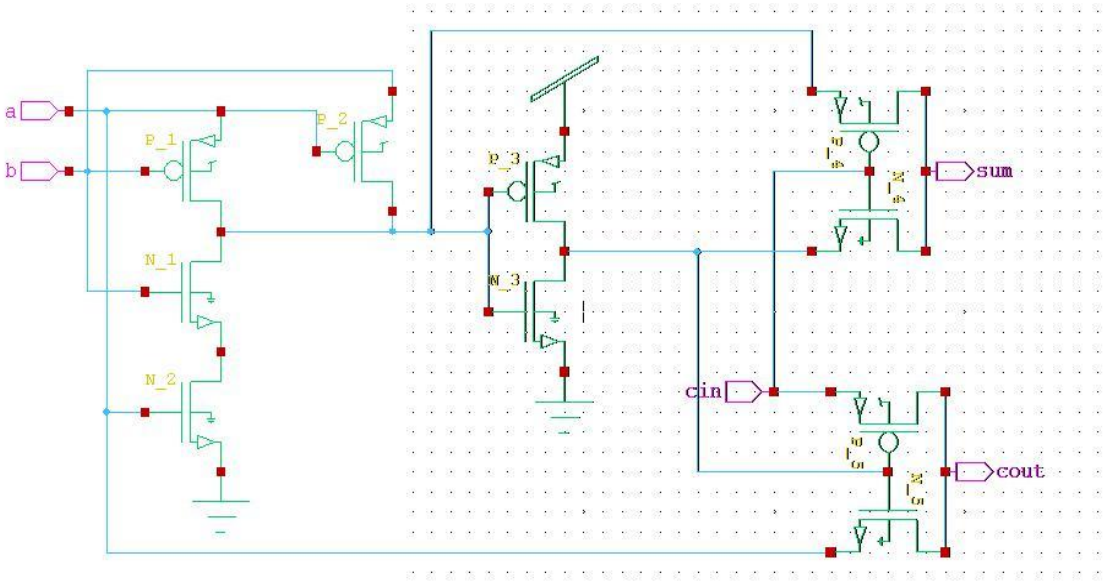

Figure 10. 10T Full Adder

H. 10T adder 1

In this circuit, sum and carry are generated using 2X1 multiplexer. In this design, X-NOR and X-OR logic is generated using three transistors. It consumed more power due to short circuit current logic. It may not work at low voltages or cascading directly without extra buffers due to threshold losses. The advantage of this adder is it occupies less area as compared higher count transistors and the disadvantage is, it is difficult to maintain full voltage swing because of fewer number of transistors in the circuit [11].

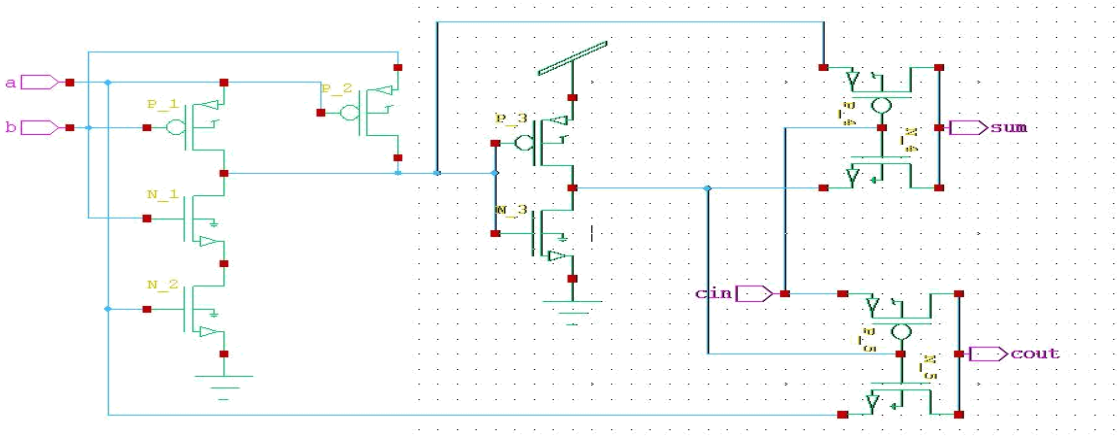

Figure 11. 10T adder 1

III. RESULT AND COMPARISON

ADDER	POWER CONSUMED(nW)	DELAY(ns)	PDP(aJ)	TC	Area(um2)	STAT(nW)
9A	5.87	0.03632	0.21	10	6	3.84
9B	9.67	0.05423	0.52	10	6	3.81
10T	2.55	0.01925	0.05	10	6	2.01
10T 1	0.0224	0.01342	0	10	6	0.01413
13A	8.01	0.03542	0.28	10	6	5.66
28T	12.8	0.14492	0.78	28	18	7.21
GDI	18	0.19597	0.89	10	6	10.5
M 9A	15.9	0.02191	0.35	9	6	1.95
M 9B	20	0.0288	0.58	9	6	3.84
SERF	15	0.03727	0.56	10	6	3.8

Table 2. Result and Comparison

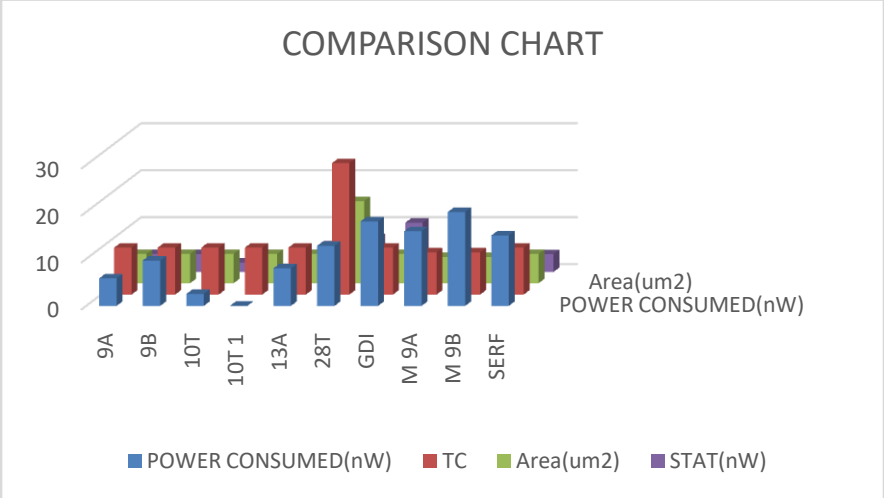

Figure 13. Comparison Chart

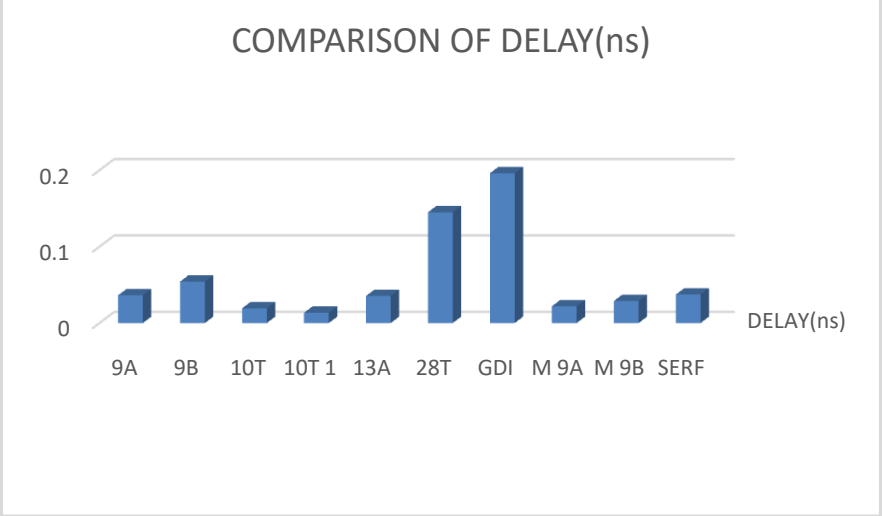

Figure 14. Comparison of Delay

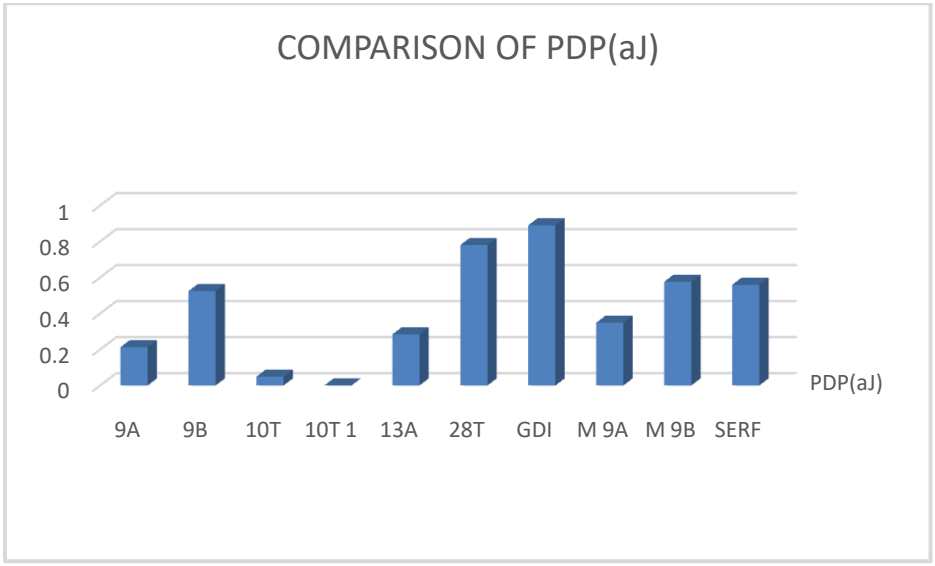

Figure 15. Comparison of PDP

IV. CONCLUSION

From the above discussion, comparison of various full adders is made. When comparing the full adders with average power consumption, static power dissipation, power delay product and delay, then 10T adder 1 gives the better result. In case of comparing the full adders with the transistor count modified 9A full adder and modified 9B full adder is good. The conventional 28T full adder is having high static power dissipation, power delay product, transistor count and area when comparing with the various full adders discussed above. When analyzing the results in power consumption point of view, 10T adder 1(0.0224nW) is much ahead of frequently used conventional 28T full adder (12.8nW) and it is better than all the above adders which discussed in this paper.

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