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Design of a Low-Voltage, Power & Double Tail Comparator Using CNTFET

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Abstract- *The need for ultra low-power, area efficient and high speed analog-to-digital converters is pushing toward the use of dynamic regenerative comparators to maximize speed and power efficiency. In this paper, an analysis on the delay of the dynamic comparators will be presented and analytical expressions are derived. From the analytical expressions, designers can obtain an intuition about the main contributors to the comparator delay and fully explore the tradeoffs in dynamic comparator design. Based on the presented analysis, a new dynamic comparator is proposed, where the circuit of a conventional double tail comparator is modified for low-power and fast operation even in small supply voltages. Without complicating the design and by adding few transistors, the positive feedback during the regeneration is strengthened, which results in remarkably reduced delay time. Post-layout simulation results in a 32nm CMOS technology confirm the analysis results. It is shown that in the proposed dynamic comparator both the power consumption and delay time are significantly reduced. The maximum clock frequency of the proposed comparator can be increased to 2 G and 1.1 GHz at supply voltages of 1.2 V and 0.6 V, while consuming 1.4 mW and 153 μW, respectively. The standard deviation of the input-referred offset is 7.8 mV at 1.2 V supply.*

Index Terms- *ultra low voltage power, double tail CMOS, UDSM etc.,*

I. INTRODUCTION

COMPARATOR is one of the fundamental building blocks in most analog-to-digital converters (ADCs). Many high-speed ADCs, such as flash ADCs, require high-speed, low- power comparators with small chip area. High-speed comparators in ultra deep sub micrometer (UDSM) CMOS technologies suffer from low supply voltages especially when considering the fact that threshold voltages of the devices have not been scaled at the same pace as the supply voltages of the modern CMOS processes [1]. Hence, designing high-speed comparators is more challenging when the supply voltage is smaller. In other words, in a given technology, to achieve high speed, larger transistors are required to compensate the reduction of supply voltage, which also means that more die area and power is needed. Besides, low-voltage opera- tion results in limited common-mode input range, which is important in many high-speed ADC architectures, such as flash ADCs. Many techniques, such as supply boosting methods [2],[3], techniques employing body-driven transistors [4], [5], current-mode design [6] and those using dual-oxide processes, which can handle higher supply voltages have been developed to meet the low-voltage design challenges. Boosting and bootstrapping are two techniques based on augmenting the supply, reference, or clock voltage to address input-range and switching problems. These are effective techniques, but they introduce reliability issues especially in UDSM CMOS technologies. Body-driven technique adopted by Blalock [4], removes the threshold voltage requirement such that body driven MOSFET operates as a depletion-type device. Based on this approach, in [5], a 1-bit quantizer for sub-1V modulators is proposed. Despite the advantages, the body driven transistor suffers from smaller transconductance (equal to gmb of the transistor) compared to its gate-driven counterpart while special fabrication process, such as deep n-well is required to have both nMOS and pMOS transistors operate in the body-driven configuration. Apart from technological modifications, developing new circuit structures which avoid stacking too many transistors between the supply rails is preferable for low-voltage operation, especially if they do not increase the circuit complexity. In [7]–[9], additional circuitry is added to the conventional dynamic comparator to enhance the comparator speed in low supply voltages. The proposed comparator of [7] works down to a supply voltage of 0.5 V with a maximum clock frequency of 600 MHz and consumes 18 μW. Despite the effectiveness of this approach, the effect of component mismatch in the additional circuitry on the performance of the comparator should be considered. The structure of double-tail dynamic comparator first proposed in [10] is based on designing a separate input and cross coupled stage. This separation enables fast operation over a wide common-mode and supply voltage range [10].

In this paper, a comprehensive analysis about the delay of dynamic comparators has been presented for various architectures. Furthermore, based on the double-tail structure proposed in [10], a new dynamic comparator is presented, which does not

require boosted voltage or stacking of too many transistors. Merely by adding a few minimum-size transistors to the conventional double-tail dynamic comparator, latch delay time is profoundly reduced. This modification also results in considerable power savings when compared to the conventional dynamic comparator and double-tail comparator. The rest of this paper is organized as follows. Section II investigates the operation of the conventional clocked regenerative comparators and the pros and cons of each structure are discussed. Delay analysis is also presented and the analytical expressions for the delay of the comparators are derived. The proposed comparator is presented in Section III. Section IV discusses the design issues. Simulation results are addressed in Section V, followed by conclusions in Section VI.

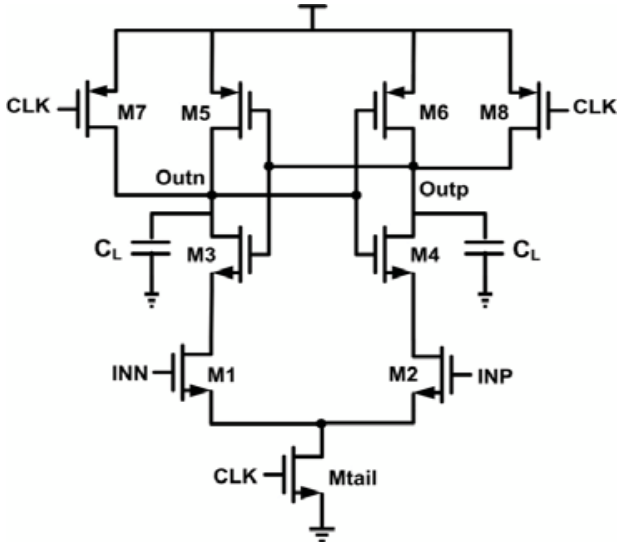


Fig. 1. Schematic diagram of the conventional dynamic comparator.

I .a. conventional dynamic comparator

The schematic diagram of the conventional dynamic comparator widely used in A/D converters, with high input impedance, rail-to-rail output swing, and no static power consumption is shown in Fig. 1 [1], [17]. The operation of the comparator is as follows. During the reset phase when CLK = 0 and Mtail is off, reset transistors (M7–M8) pull both output nodes Outn and Outp to VDD to define a start condition and to have a valid logical level during reset. In the comparison phase, when CLK = VDD, transistors M7 and M8 are off, and Mtail is on. Output voltages (Outp, Outn), which had been pre-charged to VDD, start to discharge with different discharging rates depending on the corresponding input voltage (INN/INP). Assuming the case where VINP > VINN, Outp discharges faster than Outn, hence when Outp (discharged by transistor M2 drain current), falls down to VDD–|Vthp| before Outn (discharged by transistor M1 drain current), the corresponding pMOS transistor (M5) will turn on initiating the latch regeneration caused by back-to-back inverters (M3, M5, and M4, M6). Thus, Outn pulls to V_{DD} and Outp discharges to ground. If VINP < VINN, the circuits works vice versa. As shown in Fig. 2, the delay of this comparator is comprised of two time delays, t0 and tlatch. The delay t0 represents the capacitive discharge of the load capacitance CL until the first p-channel transistor (M5/M6) turns on. In case, the voltage at node INP is bigger than INN (i.e., VINP > VINN), the drain current of transistor M2 (I2) causes faster discharge of Outp node compared to the Outn node, which is driven by M1 with smaller current. Consequently, the discharge delay (t0) is given by

$$t_0 = \frac{C_L \left| V_{thp} \right|}{I_2} \cong 2\frac{C_L \left| V_{thp} \right|}{I_{tail}}. \qquad \text{.....(1)}$$

In (1), since I2 = Itail/2 + _Iin = Itail/2 + gm1,2_Vin, for small differential input (_Vin), I2 can be approximated to be constant and equal to the half of the tail current. The second term, t latch, is the latching delay of two cross coupled inverters. It is assumed that a voltage swing of Vout = VDD/2 has to be obtained from an initial output voltage difference _V0 at the falling output (e.g., Outp). Half of the supply voltage is considered to be the threshold voltage of the comparator following inverter or SR latch [17]. Hence, the latch delay time is given by, [18]

$$t_{latch} = \frac{C_L}{g_{m,eff}} \cdot \ln\left(\frac{\Delta V_{out}}{\Delta V_0}\right) = \frac{C_L}{g_{m,eff}} \cdot \ln\left(\frac{V_{DD}/2}{\Delta V_0}\right) \qquad (2)$$

where gm,eff is the effective transconductance of the back-to back inverters. In fact, this delay depends, in a logarithmic manner, on the initial output voltage difference at the beginning of the regeneration (i.e., at t = t0). Based on (1), _V0 can be calculated from (3)

$$\begin{aligned}\Delta V_0 &= \left| V_{outp}(t=t_0) - V_{outn}(t=t_0) \right| \\ &= \left| V_{thp} \right| - \frac{I_2 t_0}{C_L} = \left| V_{thp} \right| \left(1 - \frac{I_2}{I_1} \right). \end{aligned} \qquad (3)$$

The current difference, _Iin = |I1 − I2|, between the branches is much smaller than I1 and I2. Thus, I1 can be approximated by Itail/2 and (3) can be rewritten as

$$\begin{aligned}\Delta V_0 &= \left| V_{thp} \right| \frac{\Delta I_{in}}{I_1} \\ &\approx 2 \left| V_{thp} \right| \frac{\Delta I_{in}}{I_{tail}} \\ &= 2 \left| V_{thp} \right| \frac{\sqrt{\beta_{1,2} I_{tail}}}{I_{tail}} \Delta V_{in} \\ &= 2 \left| V_{thp} \right| \sqrt{\frac{\beta_{1,2}}{I_{tail}}} \Delta V_{in}. \end{aligned} \qquad \text{..... (4)}$$

In principle, this structure has the advantages of high input impedance, rail-to-rail output swing, no static power consumption and good robustness against noise and mismatch [1]. Due to the fact that parasitic capacitances of input transistors do not directly affect the switching speed of the output nodes, it is possible to design large input transistors to minimize the offset. The disadvantage, on the other hand, is the fact that due to several stacked transistors, a sufficiently high supply voltage is needed for a proper delay time. The reason is that, at the beginning of the decision, only transistors M3 and M4 of the latch contribute to the positive feedback until the voltage level of one output node has dropped below a level small enough to turn on transistors M5 or M6 to start complete regeneration. At a low supply voltage, this voltage drop only contributes a small gate-source voltage for transistors M3 and M4, where the gate source voltage of M5 and M6 is also small; thus, the delay time of the latch becomes large due to lower transconductances. Another important drawback of this structure is that there is only one current path, via tail transistor M tail, which defines the current for both the differential amplifier and the latch (the cross-coupled inverters). While one would like a small tail current to keep the differential pair in weak inversion and obtain a long integration interval and a better Gm/I ratio, a large tail current would be desirable to enable fast regeneration in the latch [10]. Besides, as far as M tail operates mostly in triode region, the tail current depends on input common-mode voltage, which is not favorable for regeneration.

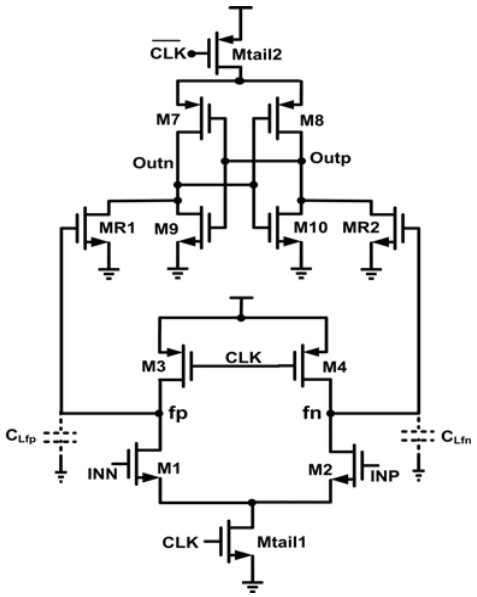


Fig 2 Conventional double tail comparator

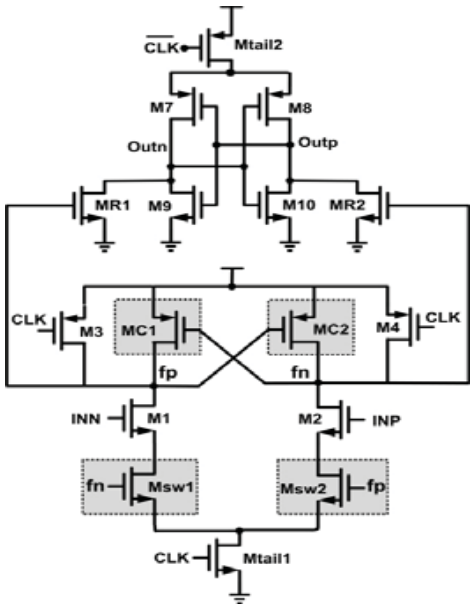


Fig 3 Double tail comparator FINAL STRUCTURE

I B Conventional double tail comparator : The operation of this comparator is as follows During reset phase (CLK = 0, Mtail1, and Mtail2 are off),transistors M3-M4 pre-charge fn and fp nodes to V_{DD}, which in turn causes transistors MR1 and MR2 to discharge the output nodes to ground. During decision-making phase (CLK = V_{DD}, Mtail1 and Mtail2 and also provides a good shielding between input and output, resulting in reduced value of kick back noise [10] turn on), M3 -M4 turn off and voltages at nodes fn and fp start to drop with the rate defined by IMtail1/Cfn(p) and on top of this, an input-dependent differential voltage _Vfn(p) will build up. The intermediate stage formed by MR1 and MR2 passes _Vfn(p) to the cross coupled inverters

I.C final structure: The operation of the proposed comparator is as follows during reset phase (CLK = 0, *M*tail1 and *M*tail2 are off, avoiding static power), *M*3 and *M*4 pulls both fn and fp nodes to V_{DD}, hence transistor *M*c1 and *M*c2 are cut off.

I.D conventional double tail comparator: Intermediate stage transistors, *M*R1 and *M*R2, reset both latch outputs to ground. During decision-making phase (CLK = V_{DD}, *M*tail1, and *M*tail2 are on), transistors *M*3 and *M*4 turn off. Furthermore, at the beginning of this phase, the control transistors are still off (since fn and fp are about V_{DD}). Thus, fn and fp start to drop with different rates according to the input voltages. Suppose $V_{INP} > V_{INN}$, thus fn drops faster than fp, (since M_2 provides more current than M_1). As long as fn continues falling, the corresponding PMOS control transistor (*M*c1 in this case) starts to turn on, pulling fp node back to the V_{DD}; so another control transistor (*M*c2) remains off, allowing fn to be discharged completely. In other words, unlike conventional double-tail dynamic comparator, in which _Vfn/fp is just a function of input transistor transconductance and input voltage difference (9), in the proposed structure as soon as the comparator detects that for instance node fn discharges faster, a PMOS transistor (Mc1) turns on, pulling the other node fp back to the V_{DD}.Therefore by the time passing, the difference between fn and fp (_Vfn/fp) increases in an exponential manner, leading to the reduction of latch regeneration time.

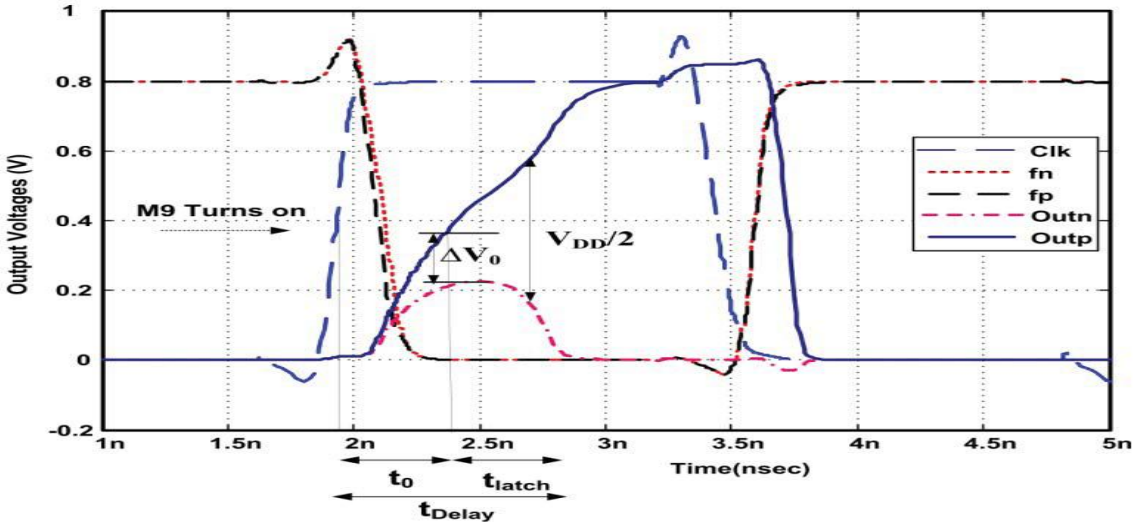


Fig:4 transient simulations of the conventional double-tail dynamic Comparator for input voltage difference of _Vin = 5 mV, Vcm = 0.7 V,and V_{DD} = 0.8 V

Replacing MOSFET with CNTFET: CNTFET utilizes a single carbon nano-tube or an array of carbon nano-tubes as the channel material instead of bulk silicon in the traditional MOSFET structure. It was first demonstrated in 1998.The structure of CNT described by an index with a pair of integers (n, m) that define its chiral vector.

$$d_t = \frac{L}{\prod} = \frac{a}{\prod}\sqrt{n^2 + nm + m^2}$$

$$\theta = \tan^{-1}\left(\frac{\sqrt{3}n}{2m+n}\right)$$

Carbon nanotube is i) Metallic when n = m

ii) It has a small Band gap when n – m = 3i

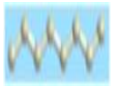
iii) Semiconducting when n – m ≠ 3i .

The chiral angle is used to separate carbon nano tubes into three classes differentiated by their electronic properties:

Arm chair (n = m, Θ= 30°),

Zigzag (m = 0, n > 0, Θ = 0°),

Chiral (0 < |m| < n, 0 < Θ < 30°). Table:1

Type	Chiral vector (c)	Leng th of chiral vector (L)	Chiral angle (Ø)	Number of Hexagons in a unit cell (N)	Shape of the cross section.
Arm chair	(n,n)	Sqrt(3). n .a	30^0	2π	Cis –type 
Zing zag	(n,0)	n.a	0^0	0	Trans type 
Chi ral	(n,m)	A(sqrt[n^2+nm+n^2])	0^0 < IØI <30^0	2 [n^2+nm+n^2] / d_R	Mix of above

Advantages of CNTFET: Better Control over channel formation. Better threshold voltage, sub-threshold slope, high mobility, current density, transconductance.

I. E Comparison between MOSFET & CNTFET:

(i) In case of Si-MOSFET switching occurs by altering the channel resistivity but for CNTFET switching occurs by the modulation of contact resistance.
(ii) CNTFET is capable of delivering three to four times higher drive currents than the Si MOSFETs at an overdrive of 1 V.
(iii) CNTFET has about four times higher transconductance in comparison to MOSFET.

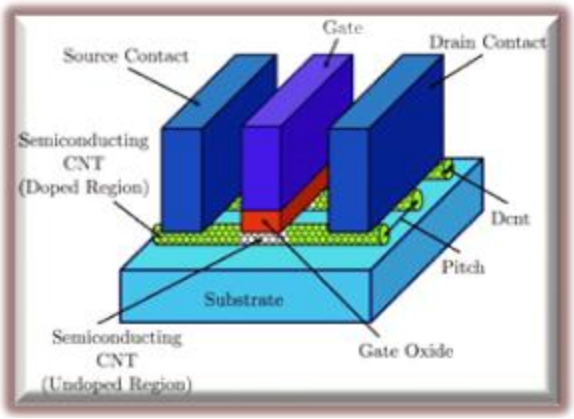


Fig 5a Ballistic CNTFET model

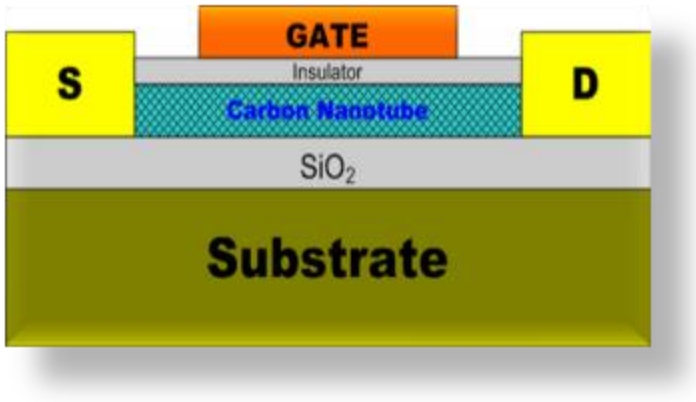


fig 5b MOSFET Model

The resistance of short 1 – D conductors is independent of composition or length and depends only on available conduction channels and transmission at the contact. This is called Ballistic conduction. This means that backscattering does not occur. This behavior is dominant in MOSFET – like CNTFET and hence indicates maximum performance The resistance of short 1 – D conductors is independent of composition or length and depends only on available conduction channels and transmission at the contact. This is called Ballistic conduction. This means that backscattering does not occur.This behavior is dominant in MOSFET – like CNTFET and hence indicates maximum performance

Channel Length (L_{ch}): The channel length is chosen to reduce the occurrence of scattering. 10nm is chosen as it is less than Mean Free Path and scattering does not occur.

Chirality Vector: Diameter of CNT is between 1.2nm and 1.8nm.In this range, the chirality vectors for zigzag tubes is (16,0) (17,0) (19,0) (20,0) (22,0). (17,0) is chosen as the chirality vectors **Diameter , it** is given by

$$D = \frac{n\sqrt{3}a_{cc}}{\prod}$$ Where n=chirality vector & acc=lattice constant = 0.142 nm for grapheme Diameter obtained is 1.33nm.

Pitch It is the minimum distance 2 adjacent carbon nanotubes.it is calculated by

$$Pitch = \frac{W_g - d}{N - 1}$$ Oxide Thickness (tox) For channel length of 10nm, the tox is prescribed to be 2nm.

Wg = Gate width = 32nm,d = Diameter,N = Number of Parallel Channels = 9 Pitch is calculated to be 4nm.

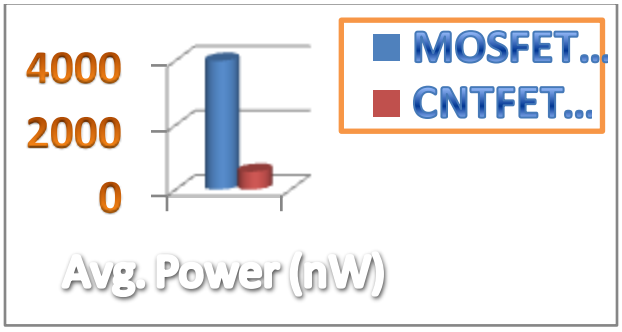


Fig 6 a AVG Power of MOSFET&CNTFET

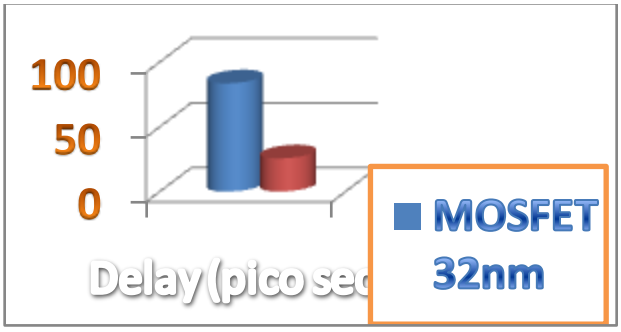


Fig 6 b AVG Delay of MOSFET

II.SIMULATION RESULTS

In order to compare the proposed comparator with the conventional and double-tail dynamic comparators, all circuits have been simulated in a 32nm CMOS technology with V_{DD} = 1.2V.

Table 2 parameter Vs CNTFET comparisons

parameters	CNTFET (32 nm)
channel length	32nm
diameter	0.144nm
lss	32nnm
ldd	32nm
tox	4nm
k	16
pitch	20nm
chiral vector	(19,0)

II.1 Simulation Results for the proposed comparator:

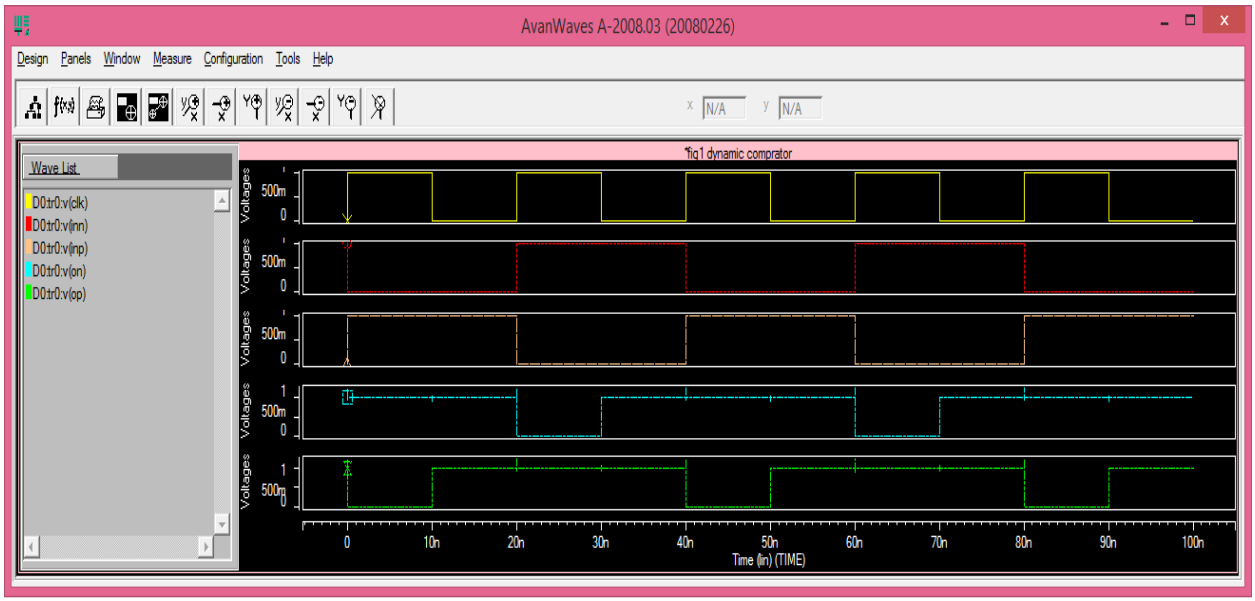


Fig7: Conventional comparator

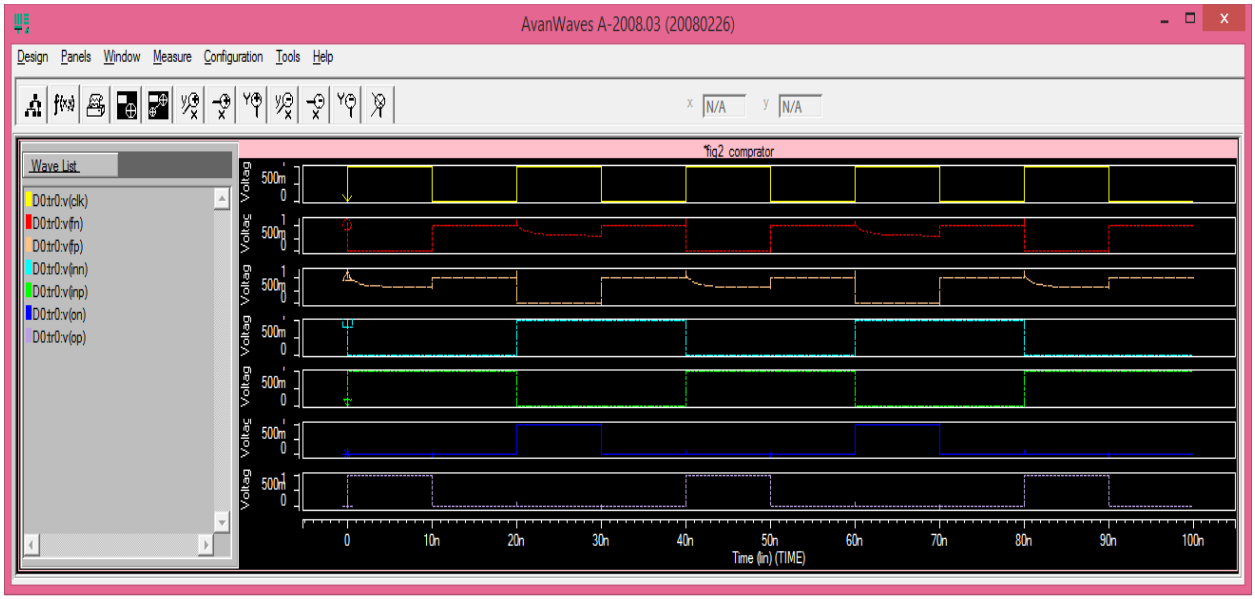


Fig8: Single Tail dynamic comparator

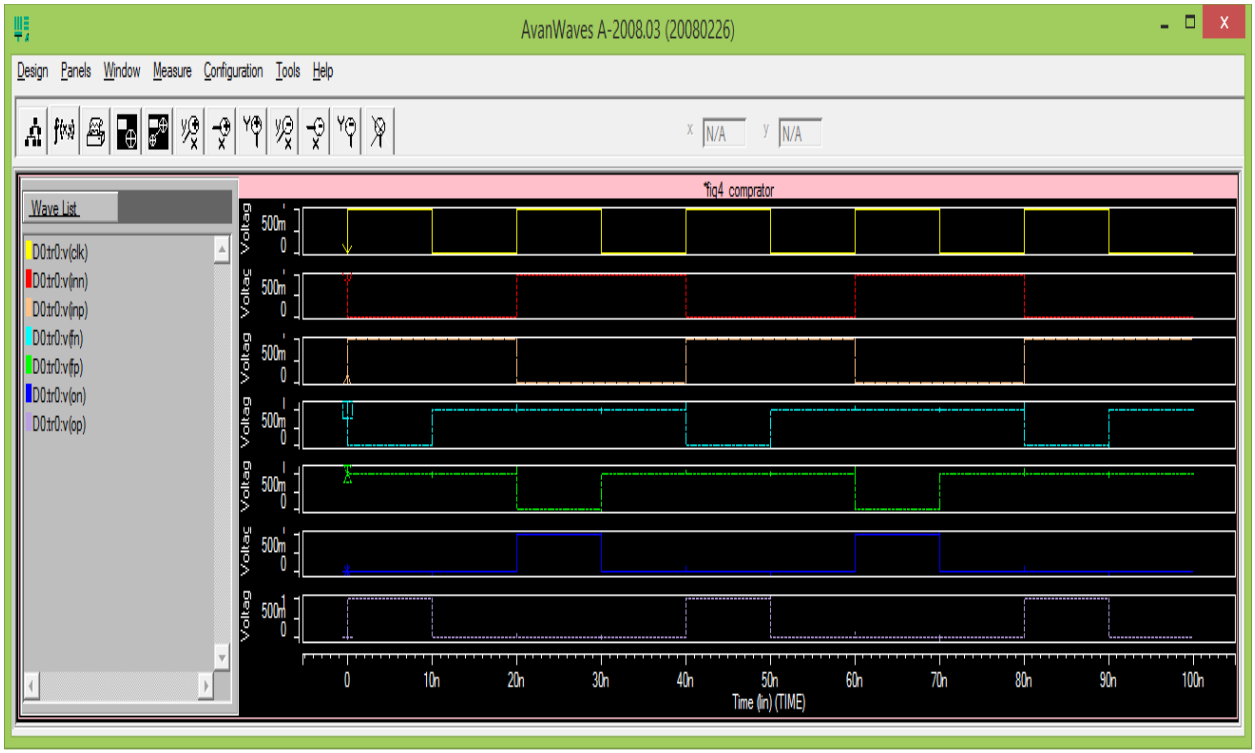


Fig9: Double Tail comparator

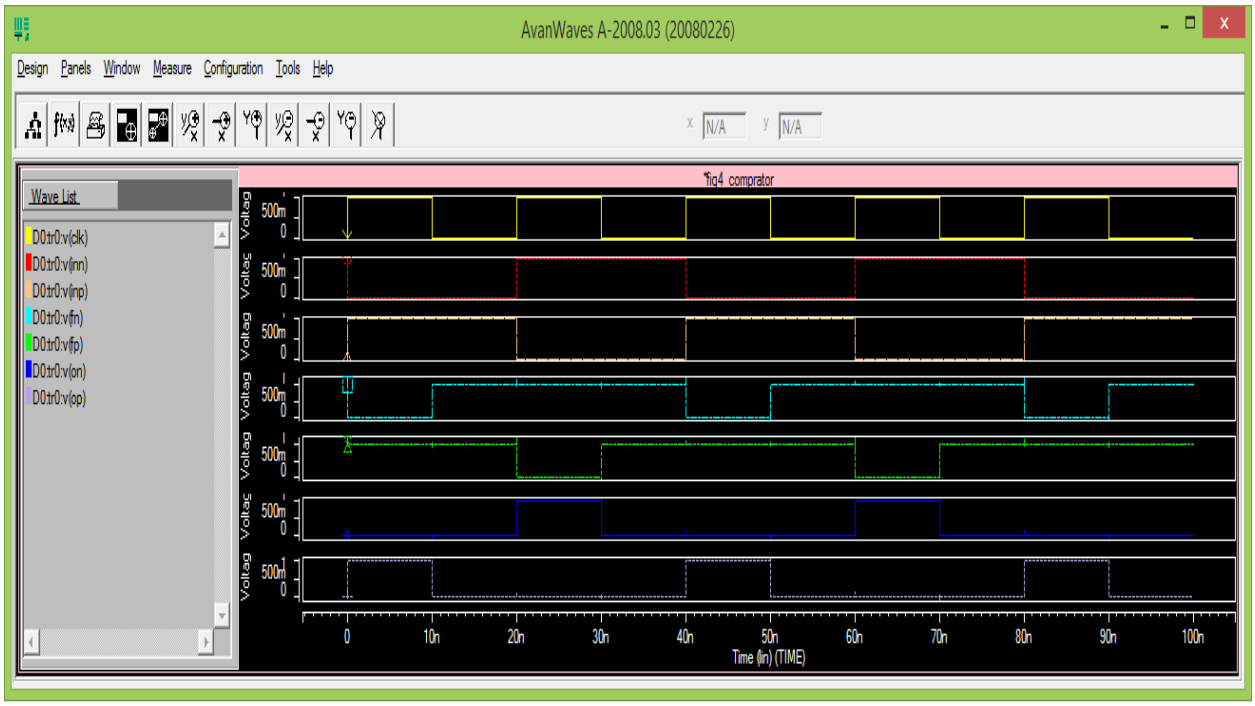


Fig 10: proposed Double tail Comparator

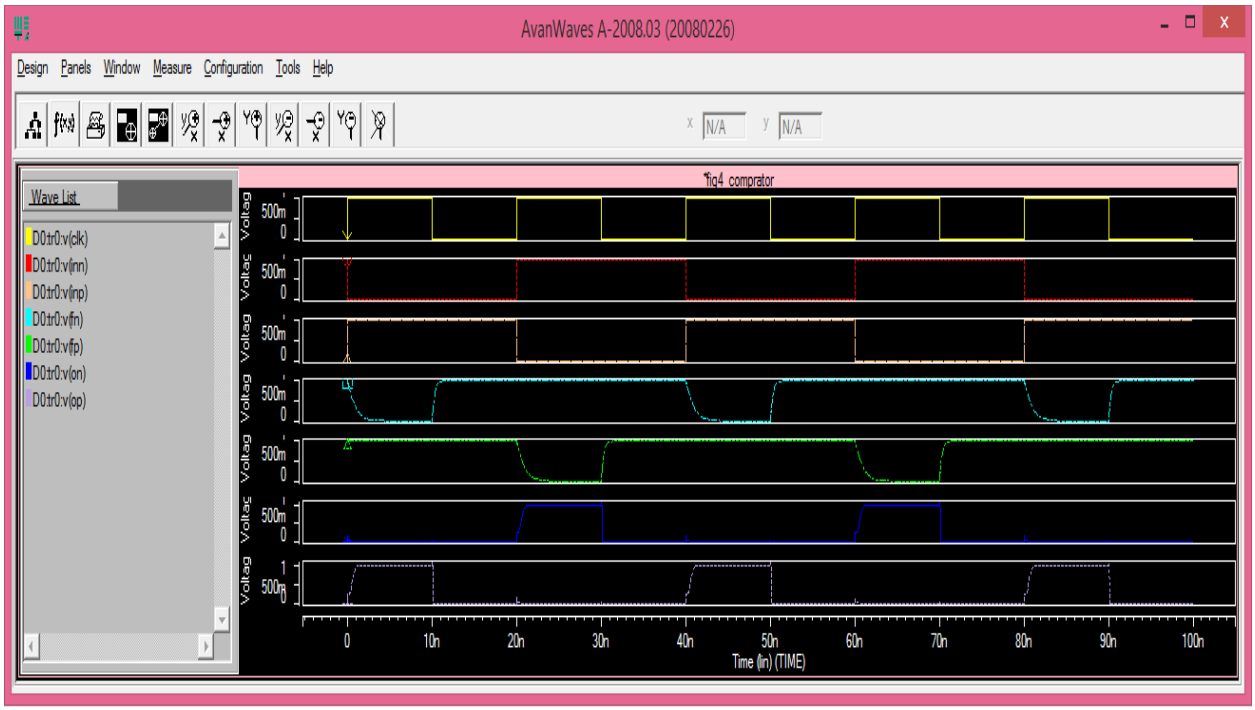


Fig:11 Double tail comparator using CNTFET

II.2 RESULTS COMPARISIONS

Table 3 comparison of conventional with proposed comparators (MOSFET)

S.no	Comparator structure	Conventional dynamic Comparator	Double-tail dynamic comparator	Proposed dynamic comparator	
				Main Idea	Final structure
1	Technology CMOS	32 nm	32 nm	32 nm	32 nm
2	Supply Voltages (V)	1V	1 V	1 V	1 V
3	Frequency	500 MHz	500 MHz	500 MHz	500 MHz
4	Avg power	109 nw	214.2 nw	256.3 nw	263.4 nw
5	Delay	4.986 psec	5.40 psec	6.83 psec	7.941 psec
6	Power delay product	0.5 aJ	1.15 aJ	1.75 aJ	2.09 aJ
7	Offset voltages	0.35 V	0.36 V	0.364 V	0.365 V
8	Leakage power	61.1nW	0.14 µW	0.14 µW	0.14 µW

Table 4 comparison of conventional with proposed comparators using CNTFET

S.no	Comparator structure	Conventional dynamic Comparator	Double-tail dynamic comparator	Proposed dynamic comparator	
				Main Idea	Final structure
1	Technology CMOS	32 nm	32 nm	32 nm	32 nm
2	Supply Voltages (V)	1V	1 V	1 V	1 V
3	Frequency	500 MHz	500 MHz	500 MHz	500 MHz
4	Avg power	2.19 nw	4.04 nw	4.95 nw	6.4 nw
5	Delay	4.47 psec	3.75 psec	3.83 psec	4.641 psec
6	Power delay product	9.78*10^-21J	15.1 *10^-21J	19.05 *10^-21J	29.4 *10^-21J
7	Offset voltages	0.35 V	0.36 V	0.364 V	0.365 V
8	Leakage power	27.8 pW	95 pW	38.4 pW	46 pW

III. FUTURE SCOPE

The CNTFET model can be implemented in any digital circuit for both combinational and sequential. Reliability, cost and performance issues have to be addressed. Current limitations in the design technology make the proposed model difficult to manufacture.

IV. CONCLUSION

In this paper, we presented a comprehensive delay analysis for clocked dynamic comparators and expressions were derived. Two common structures of conventional dynamic comparator and conventional double-tail dynamic comparators were analyzed. Also, based on theoretical analyses, a new dynamic comparator with low-voltage low-power capability was proposed in order to improve the performance of the comparator. Post-layout simulation results in 0.032-µm CMOS technology, CNTFET confirmed that the delay and energy per conversion of the proposed comparator is reduced to a great extent in comparison with the conventional dynamic comparator and double-tail comparator. According to results obtained for mosfet and cntfet the cntfet is 90-94 % efficiency in terms of power and delay.

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VI. AUTHORS BRIEF PROFILE

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[3]Dr K RAMESHBABU working as professor, C CET, affiliated to Pondicherry University, Puducherry. He did B.E(ece), M.E, Ph.D having 20+ years of Experience in the field of Teaching completely. he is Guest professor for various colleges affiliated universities like Anna.University,Shivaji University,JNTU etc.he is member of IEEE,ISTE,VSI.IJCSIT, IRED he is reviewer for many journals & published 18+ papers in international journals and conferences & also conducted, attended many Faculty Development Programmes .his area of interest image processing,vlsi,digital electronics etc.

