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AREA OPTIMIZATION AND PERFORMANCE IMPROVEMENT OF CARRY SPECULATIVE ADDITION BY MODIFYING BLOCK ADDER AND ERROR CORRECTION CIRCUIT

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Abstract: *This paper proposes carry speculative addition using modified error correction, block adder design to reduce critical path delay there by reducing area and power consumption. The modified error correction block and block adder possesses less number of gates compared with existing circuit. The complete proposed Carry Speculative Addition using modified error correction and block adder with a data latching circuit to get continuous data into circuit architecture is implemented using Verilog HDL and the design is simulated using Xilinx ISE and vivado 2016.4,artix 7 family device XC7A100TCSG324-1.*

Keywords: *Full adder, speculation, critical path delay, variable latency, error detection, error recovery.*

I.INTODUCTION

Adder is the one of the most basic element in digital systems. The performance of an adder depends on amount of power consumed by the circuit, space occupied, time taken to produce output after application of inputs and accuracy of obtained result. Ripple carry adder is the traditional adder used for performing addition operation in digital systems, due to large latency produced by this circuit it is modified using lookahead carry generator. The resultant lookahead adder is not suitable for addition of data with large bit length because of its low speed performance, high area. Using pipelining concept the performance of adder was increased but there is more power consumption [2]. Some designs are developed from the observations that critical path is rarely activated in traditional adders, based on speculation technique by sacrificing exactness in result.

These approximations increase the performance by reducing power consumption with a simplified circuit, where strict requirements are relaxed. Speculation technique is an optimization technique based on prediction mechanism for reducing delay in arithmetic circuits. The variable latency unit exhibit the property that the number of cycles taken to compute their outputs varies depending on the input values. By adopting emerging concept in VLSI design, speculative techniques a variable latency carry speculative adder was designed [1]. Replacement of internal carry generator block with single AND, OR gate implementation doesn't give satisfactory sum for all combination [3]. Now in our project we are going to reduce the area occupied by the existing circuit, power consumption, propagation delay of existing carry speculative adder by modifying the block adder and error correction circuits. These adders are useful in applications such as DSP, Microprocessors, Video compressions, Image processing applications which involve large number additions.

II.EXSITINGTECHNIQUE

2.1 CARRY SPECULATIVE ADDER

CARRY SPECULATIVE ADDER (CSPA) is used to reduce the critical path delay of arithmetic circuit which is designed based on carry speculation technique with an assumption that the carry out bit generated at a particular position of input bits depends only up to previous 'x' bits rather than up to LSB bit. This architecture uses carry predictor, internal carry generator, sum generator blocks and multiplexers. The block diagram of carry speculative adder is as shown in the figure1

The n-bit CSPA is divided into small block adders all those block adders operates parallel. A carry predictor circuit is used as selection line to the multiplexer whose inputs are connected to the bit pattern coming from internal carry generators with one connected to binary one (Vdd) and other to binary zero (gnd). The size of each block adder is x-bit, there are 'm' independent block adders and '(m-1)' carry predictor circuits in the CSPA, where m = (n/x).

2.1.1 CARRY PREDICTOR

In order to reduce the critical path delay a carry predictor circuit is designed to predict carry out bit of corresponding block adder. This circuit uses the bits that are near to MSB bits of corresponding block adder as input to generate predicted output. Which results minimum loss of accuracy but improvement in performance.

Since the probability of effecting the carry out bits due to bits near to LSB is low. If we use 'k' previous bits of block adder from MSB (including MSB) to predict the carry out bit from corresponding block adder then the probability that

carry out bit be binary one is 1/2^k because the probability of propagate signal Pi (ai XOR bi) having a value of binary one is 1/2 in each position.

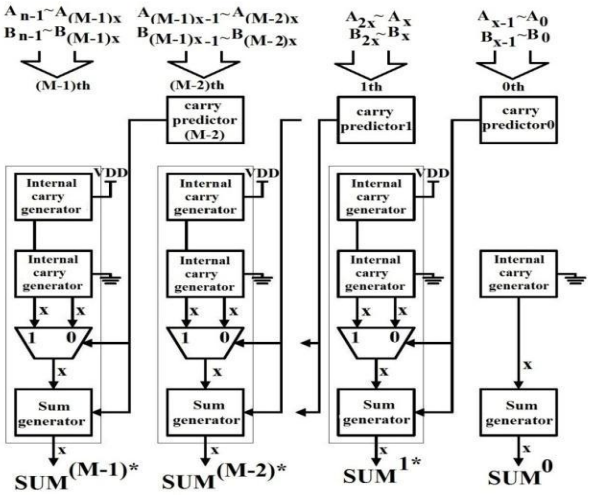

Figure1.CSPA implementation

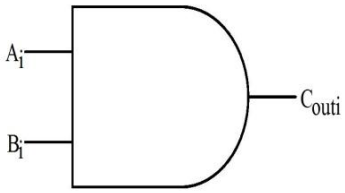

Figure2.Carry predictor circuit (Cout=predictedoutput)

2.1.2. INTERNAL CARRY AND SUM GENERATOR:

In traditional adders (Ripple carry, Lookahead carry adders) we use full adders by cascading two half adders and an OR gate to generate sum bit, and carry bit. The gate level implementation of full adder with input bits as Ai, Bi and output bits Ci, Si is shown in the figure.3

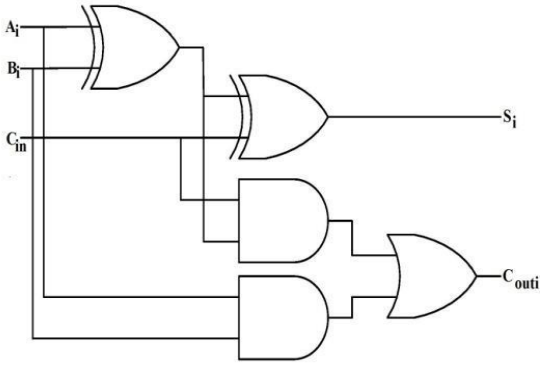

Figure3.Block diagram of full adder

But in CSPA block adder the sum generator and carry generator blocks are implemented separately to generate sum and carry bit by using an additional logic gate compared with the traditional full adder block as shown in figure.4

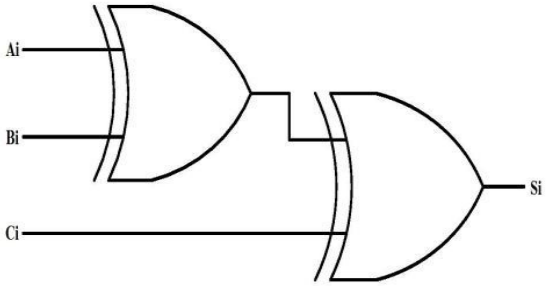

Figure 4(a)Block diagram of Sum generator

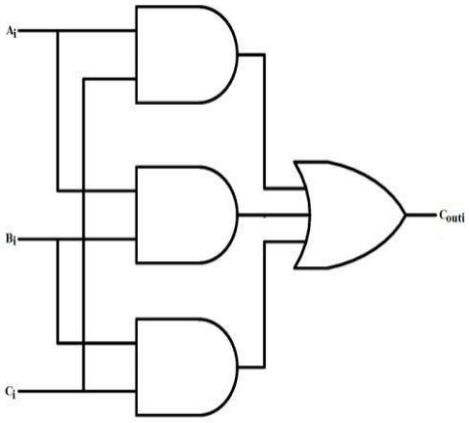

Figure4(b) Block diagram of Carry generator

But the modified full adder block implementation as two separate blocks results in path delay reduction in generating carry bit. Since the traditional adder block is three gate level implementation but the internal carry generator of CSPA is a two level implementation.

2.1.3. BLOCK ADDER:

The block diagram of block adder in the existing CSPA is as shown in figure 5

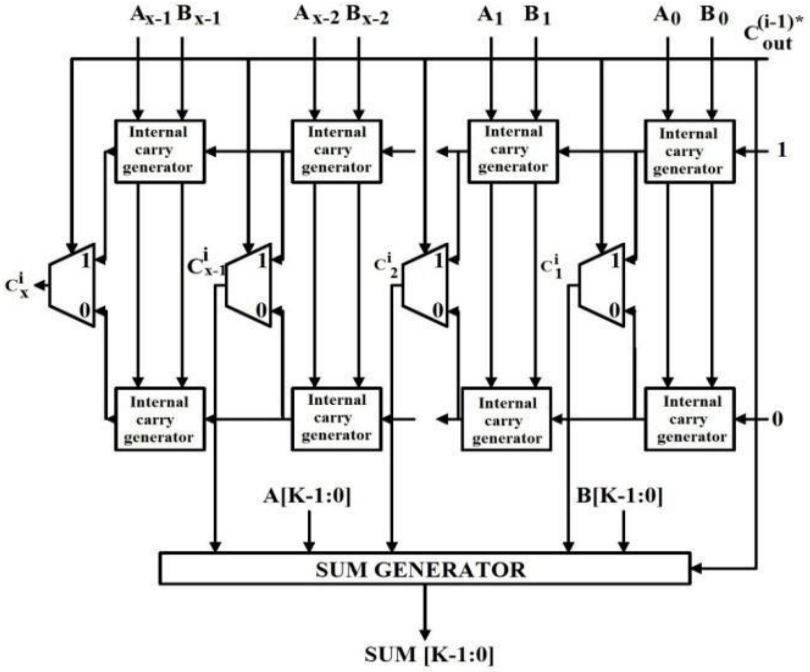

Figure 5. Block diagram of the Block adder

For an 'x' bit block adder, it consists of 'x' number of two bit multiplexer, sum generators and '2x' number of two bit internal carry generators.

From the block diagram shown in fig.5, 'x' number of internal carry generators are connected in cascade with ci in the carry generator block at right most side of block adder (i.e., with input bits A0,B0) as binary one and output from each carry generator block is connected to input of 2x1 mux. The same structure but with ci in the carry generator block at right most side of block adder as binary zero and the output from each carry generator block is connected to other input of mux. When the input pattern is arrived both these blocks operates parallel. The output of carry predictor with input data taken from data applied to right adjacent block adder is used as selection line to all 2x1 mux to select carry bit pattern. The selected bit pattern is propagated to sum generator block (except the carry bit selected from MSB bits applied to corresponding block adder) along with predicted carry to generate partial sum.

2.1.4 ERROR DETECTION:

In CSPA, the addition operation is based on speculation which may produce accurate or inaccurate results. To check whether the partial sum generated by the block adders are accurate or inaccurate the error detection circuit is designed as shown in the figure.6

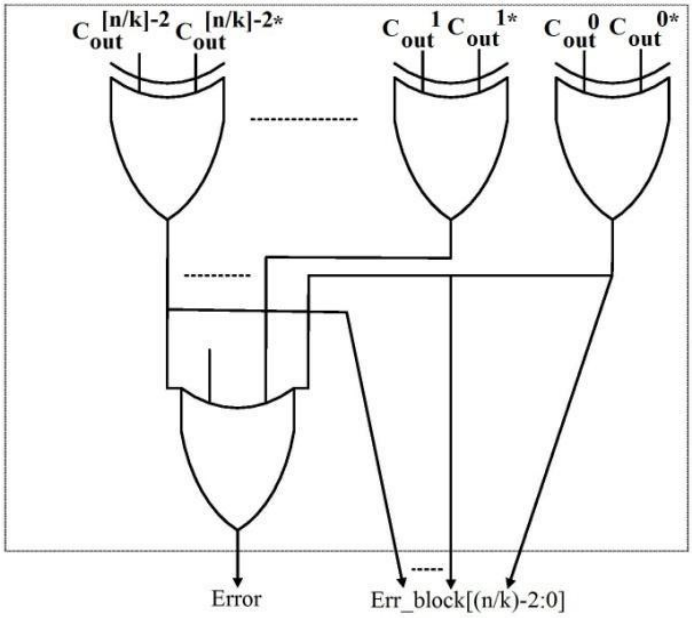

Figure.6. Block diagram of error detection

This circuit uses XOR gates to compare the actual carry out bit (Couti) from "ith" block adder with the output of ith carry predictor block (Couti*) having inputs that are taken from respective block adder. If both are same then the partial sum generated from the block adder using (couti*) the output of carry predictor circuit is accurate. This circuit consist of '(m-1)' XOR gates, m=n/x .If the output of XOR gate is one then it represent occurrence of error. All the outputs from the XOR gates are applied to OR gate, the output of or gate indicate whether the 'n' bit sum produced is correct or incorrect.

2.1.5 ERROR RECOVERY

The output from the each XOR gate (ERR_blk[i]) is used as selection line to generate the correct sum from the partial sum bits (SUMi*) obtained from the block adder.The error recovery circuit is as shown in the figure.7

From the observation that from all possible combinations of input data occurrence of error is getting binary zero as output of carry predictor instead of binary one. Hence if error occurred then the partial sum generated from the block adder is one less than the actual sum.

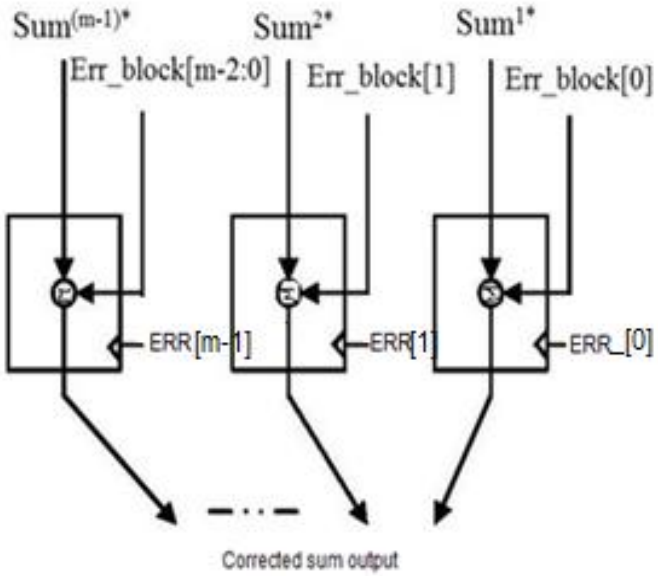

Figure7. Block diagram of Error Recovery Circuit

The error detection block shows that partial sum from block adder is added with ERR_blk signal, if error occurred then one is added to the output of block adder otherwise zero is added.Here the addition operation require two gate level sum generator, carry generators.

2.1.6 VARIABLE LATENCY CARRY SPECULATIVE ADDER:

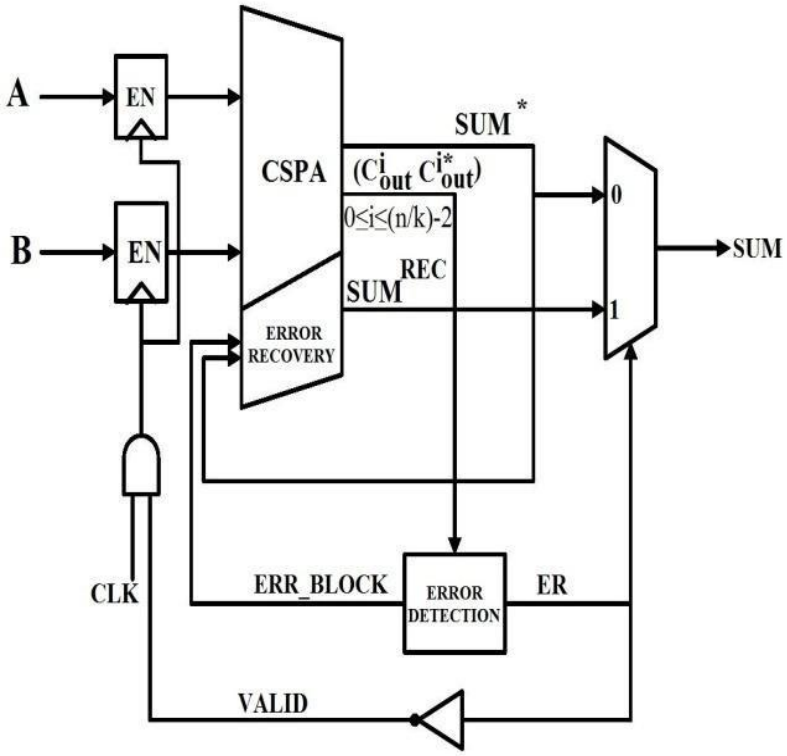

Figure 8. CSPA implementation with Variable latency

A variable latency design can reduce circuit timing waste when critical path delay is used as execution period. In variable latency design, two clock cycles are used.

Figure8 shows the CSPA with error detection and recovery circuits. When an input pattern is arrived, Variable Latency Carry Speculative Adder (VLCSPA) gives the result of the Carry Speculative Adder i.e., SUM* in a cycle. The error detection circuit gives Error block signals and error signal. The Error block signals that are generated by the error detection circuit indicates which block adder generated inaccurate results and the accurate results. The error signal indicates if an error is occurred or not. If the error signal ER indicates 0 and the VALID signal is indicates 1 when the results are accurate. Then, the results calculated by the Carry Speculative Adder are correct and are used as the output. If the Error signal indicates 1 and the VALID signal indicates 0when the results are inaccurate, then the results calculated by the Carry Speculative Adders are not correct and the correct results are recovered from Error Recovery Circuit in one more cycle and result is given as SUMREC. If an error is occurred, the input registers are disabled and no new input is loaded in the circuit. The average latency of the Variable Latency Carry Speculative Adder
(VLCSPA) is close to that of the Carry Speculative Adder since the error rate of the Carry Speculative Adder is low.

III.PROPOSEDTECHNIQUE

In VLCSPA a full adder block is implemented with two separate sum and carry generators with an extra logic which lead to increase area and power consumption.To compensate this some modifications are done in block adder design and in error recovery block.

3.1 MODIFIED BLOCK ADDER

In the existing CSPA block adder to the right most internal carry generator blocks the input carry ci is known.If ci=1 then the actual two level internal carry generating is equivalent to single OR gate,and if ci=0 then equivalent to AND gate. Hence compared with existing block adder one level path delay, 6 logic gates are reduced. The block diagram is as shown in the figure.9

3.2 MODIFIED ERROR RECOVERY CIRCUIT

From observations it is clear that if we use single AND gate with MSB bits of block adder as inputs as carry prediction circuit an error occurred only when one of the input bit to predicted circuit is binary one and the actual carry propagated to this combination is one in those cases the carry out from block adder is binary one but predicted carry is binary zero. In those situations the ERROR signal is used as enable signal to the select sum from error recovery block.

From fig10 error recovery block consists of XOR gates with input bit pattern are carry bit pattern generated for ci=1 (Pi) case and the half adder sum for the input bit pattern applied to that block, which is obtained after first level in the sum generator block.

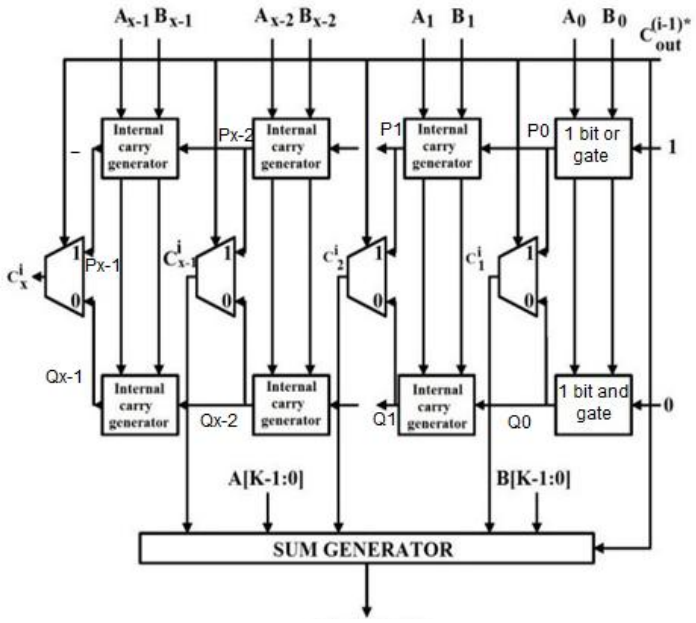

Figure 9. Block diagram of block adder with Modified carry generators

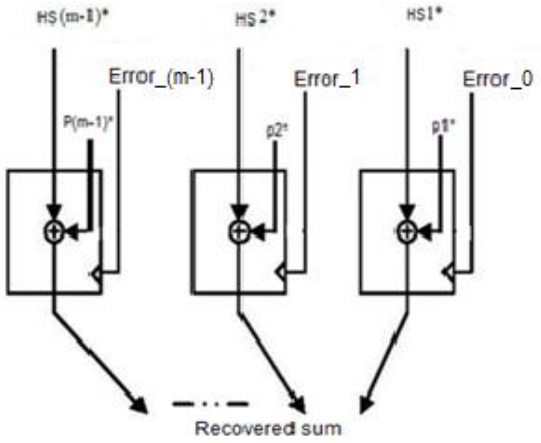

Figure 10. Block diagram of modified Error Recovery Circuit

3.3 VARIABLE LATENCY CARRY SPECULATIVE ADDER USING MODIFIED BLOCKS:

In variable latency carry speculative adder, Carry Speculative Adder ,error detection circuit, error recovery circuit ,data latching circuit and multibit multiplexer are used as shown in figure 11.When an input pattern is arrived, VLCSPA gives the result of the CSPA (i.e., SUM*) in a cycle. The error detection circuit gives Error_ block signals and error signal. The error recovery circuit recovers the results when an error occurs based on the Error_block, the results from error recovery circuit and cspa are given to multibit multiplexor and the error is used as multiplexor select signal .when the ER signal is "1" which selects recovers signal from error recovery circuit. When the ER signal is "0" which selects results from CSPA

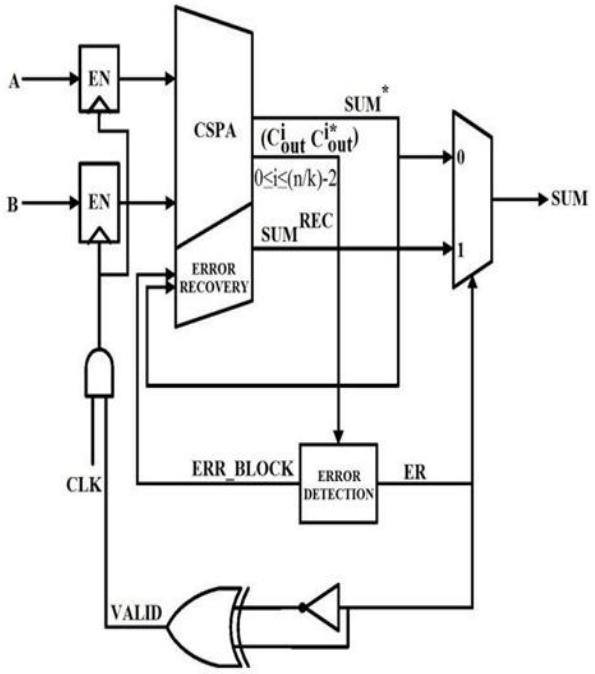

Figure.11CSPA modified implementation with Variable latency

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When an error is occurred, the input registers are disabled and no new input is latched in the circuit. This data latching which consists of not gate is replaced with Xor gate. In the latching circuit, an exclusive or operation is performed between error signal and complement of error signal. The valid signal enabling latch new data into input registers after the old data is recovered.

IV. EXPERIMENTALRESULTS

Carry Speculative Addition using Modified Blocks architecture is implemented in Verilog HDL and simulated the designed architecture using Xilinx vivado2016.4, Artix7 family device Xc7a100Tcsg324-1.This adder is implemented for three widths. In each case, the maximum combinational path delay, number of LUT'S required and Power Analysis is calculated. Table I Table II and Table III show the results of CSPA adders for three widths. From the simulation results the number of LUT'S is decrease by 36%,whileperformance of CSPA with modified Blocks is improved by 20%, and Power is reduced by 5%.

Table I: Maximum Combinational Path Delay of CSPA and CSPAM

ADDER BIT LENGTH	DELAY(ns)	
	Existing CSPA	Modified CSPA
16	3.098	2.921
32	4.656	3.296
64	5.215	3.814

Table II: Number of LUT'S in existing and modified CSPA

ADDER BIT LENGTH	AREA	
	Existing CSPA	Modified CSPA
16	70	37
32	76	39
64	173	150

Table. III: Power analysis of existing and modified CSPA

ADDER BIT LENGTH	POWER (W)	
	Existing CSPA	Modified CSPA
16	11.83	11.08
32	25.293	24.654
64	49.417	46.454

V. CONCLUSION

From the results it is clear that implementation of CSPA with modification in error detection block and in block adder reduce the power consumption, maximum combinational path delay and utilization of LUT's.In this paper, two types of carry generators are used for input carry one and carry zero implementation of separate design, a data latching circuit is also implemented in variable latency design to use continuous input to adder without area overhead. This type of adders used in DSP applications, image processing and video compression applications involves large number of addition

REFERENCES

[1] Carry Speculative Adder with Variable Latency for Low Power VLSI, by Subhashinee A and Rajasekaran C , Department of Electronics and Communication Engineering, K S Rangasamy College of Technology, Tiruchengode, India

[2] High Speed and Low-Power VLSI-Architecture for Inexact Speculative Adder by Rahul Shrestha, Member, IEEE School of Computer &Electrical Engineering, Indin Institute of Technology(IIT) Mandi, rahulshrestha@iitmandi.ac.in

[3] Performance Improvement And Area Optimization Of Carry Speculative Addition Using Modified Carry Generators, Ijsret Paper By Y PrudhviBhaskar, S K Ahemed Ali, B V Pavan Kumar, Department of ECE, SASI Institute of Technology and Engineering, Tadepalligudem, Andhra Pradesh, India.

[4] DIGITAL DESIGN With An introduction to the Verilog HDL, Fifth Editin, by M. MORRIS MANO , MICHAEL D. CILETTI

[5] Ing-Chao Lin, Senior Member, IEEE, Yi-Ming Yang, and Cheng-Chian Lin, "High-Performance Low-Power Carry Speculative Addition With Variable Latency", IEEE transactions on very large scale integration (vlsi) systems

[6] Gai Liu, Ye Tao, Mingxing Tan, and ZhiruZhang,Computer Systems Laboratory, Electrical and Computer Engineering, "CASA: Correlation-Aware Speculative Adders"

[7] Junjun Hu and WeikangQian, Shanghai "A New Approximate Adder with Low Relative Error and Correct Sign Calculation", 2014

[8] V. Gupta, D. Mohapatra, A. Raghunathan, and K. Roy, "Low-power digital signal processing using approximate adders," IEEE Trans. Comput.- Aided Design Integr. Circuits Syst., vol. 32, no. 1, pp. 124–137,

