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A STUDY OF HYBRID FULL ADDER FOR LOW POWER AND HIGH SPEED APPLICATIONS

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ABSTRACT-*This paper present a review on the study of different logic style of full adders and taking positive aspects of these design style to form a hybrid for low power consumption and minimum propagation delay .In this paper our main focus is to find out the module of full adder which consume more power and then reducing the transistor count. so that it can be used in many applications like mobile phones ,PDA, laptop etc .as full adder is basic building block of various circuits.*

Keywords- *full adder, hybrid, transistor count, propagation delay etc.*

I. INTRODUCTION

The industry of electrical and electronics has seen a rising and unmatched growth and development since he last few decades. The whole credit of this unprecedented hike in growth goes to the world of telecommunications, integrated circuits that are being used in the field of computing and the consumer electronics. In the early era of 1950's, single transistor were being used and now we have covered a great distance to use the ULSI (Ultra Large Scale Integration) systems where a single chip has the power to withhold more than 50 million transistors

A. Need of Low Power VLSI Design

First of all, it is very important to understand what actually power dissipation is. It is actually the rate through which energy is being transferred from certain source to the device in use. Power dissipation [4] acts as an actual hurdle in designing any device. There are many reasons why this issue is emerging these days. Some of the major issues are being discussed over here

The devices such as notebook computers, laptops etc have a must need of long lasting battery. Most of the applications that are portable use the Nickel Cadmium(NiCd) batteries which are rechargeable. The battery industry has been working over the life of batteries from over the decade to extend the hours a battery can work without being recharged. There are continuous efforts to develop batteries which are much more efficient than the NiCd and have higher capacity in terms of energy but still not much growth has been noticed. Till the turn of century, only about 40% of the energy density has been improved. There are some better and advanced technologies like the Nickel-Metal Hydride (Ni-MH) batteries which have good characteristics of energy density, but still their lifetime is also low. Thus, it is clearly visible that we can have only limited improvement and gains with the advent of battery technology. Therefore, it is important to develop low power design techniques so as to increase the working efficiency of the portable devices [8].

II .LITERATURE SURVEY

Parth Bhattacharyya (2014) In this article a hybrid 1-bit full adder configuration utilizing both corresponding metal-oxide-semiconductor (CMOS) rationale and transmission gate rationale is accounted for. The outline was executed firstly for 1 bit and after that reached out having 32 bit too. This circuit implementation was executed utilizing Cadence Virtuoso instruments in 180nm and 90-nm innovation. Pakkiraiahchakali et al (2012)In this paper, took into consideration the input techniques of gate diffusion where the power required for computation was very low. With the help of this, the digital combinational system can be easily designed that too with the less transistor count and along with the full swing. Through this the latency was reduced to much higher extent and thus a carry ahead header was designed which consumed very less power and where the speed was very high.[4]BalakrishnaBatta et al (2012)In this paper entertained with the fact that to design the low power circuitry, one of the best present techniques was the GDI technique. The digital circuit designed on the basis of this technique enabled the reduction in the amount of power being consumed along with the transistor count of the digital circuit and the propagation delay. When the comparison was made among GDI, CMOS and other full adders, it was found out by them that

the size of the chip is reduced to a greater extent with the GDI technique and there is fabrication with very high density.[9]C. Wey et al (2012**)** In this paper proposed an efficient strategy where a common Boolean logic is being shared within all the adders so that less computational area and power are being required. With the help of this technique, whichever adder cells are duplicate can be removed out. This way the speed of the conventional carry adder can be hiked up and also the number of transistors required can be lessen up. He came to a conclusion that the speed of this proposed CSLA design was much high and there was very less propagation delay.[15]S.Wairya (2011)This paper introduces a similar investigation of low-power, high speed and low voltage circuits of full adder. Their plan depends on XNOR-XOR (4T) plan full adder circuits joined in a solitary unit. This framework helps in reducing the power use and the multiplication delay while keeping up low unusualness of method of logical arrangement. Reenactment comes about show the prevalence of the composed adder circuitry in contrast to the regular TG, Hybrid adder and CMOS circuits regarding delay, power delay product (PDP) and power at low voltage. Clamor examination demonstrates focused on high recurrence and high temperature attractively in full adder circuit's function. Recreation comes about uncover that the composed circuits display bring down power delay product (PDP) and more power effectiveness and quicker when contrasted with the accessible full adder circuits having low value of voltage. The outline was actualized on UMC 0.18µm processing models when implemented on Cadence Virtuoso Schematic Composer tool at 1.8 V single finished voltage supply and recreations are completed on Specter S.[2]
M.Aguirre-Hernandez et al. (2011)We exhibit two rapid and low powered full-adder cells composed with an option inner logic structure and pass logic transistor rationale styles that prompt have a decreased power-delay product .We did an examination against other full-adders uncovered as having a low PDP, to the extent speed, control usage and zone. All the full-adders were formed with a 0.18-µm CMOS advancement, and were had a go at using a total test bench that allowed to gage the current taken from the full-adder inputs, other than the current gave from the power-supply. Post-arrange reenactments exhibit that the proposed full-adders outmaneuver its accomplices demonstrating an ordinary PDP ideal position of 80%, with only 40% of relative region. [3]

III. ADDITION METHODOLOGY

A. Logical Designs Techniques

The CMOS technology is developed by taking up the complement of the pull-up PMOS transistor and Pull-down NMOS transistor. Most of the predictable networks are the MOSFET[10] networks but if we look at a circuitry level, the design of the circuit needs to be optimized in such a way that it should have very less number of transistors within it. Also, the power consumption needs to be much optimized along with the reduction delay. Pass Transistor Logic (PTL) is a low power digital circuit which is obtained by the NMOS transistor.

A control signal is connected over the gate of the transistor and all the while an input signal is being connected towards the source of the transistor. To solve the problems, a lot of PTL techniques have been introduced in the market. With the help of the transmission gate (TG), a number of complex logic functions can be simply entertained. In this, just a few complementary transistors have to be used. Machinery is being introduced so as to improve the dissipation of the power. There are number of logic styles having different performance parameters where each of them has certain specialties. In the conventional domain some of the best design styles being accommodated are dynamic CMOS logic, transmission gate full adder (TGA), static complementary metal–oxide–semiconductor (CMOS) and complementary pass-transistor logic (CPL)[4]. Hybrid logic design style is also there which is being used by some other adders having integration of more than one logic style. With the help of these designs, the performance of the adders can be boosted up.

IV. HYBRID FULL ADDER

Nowadays, battery operated portable devices like laptops, notebooks, cellular phones etc are widely used in the market. These devices have demand of the VLSI with the designs that are ultra large scale integrated and also where the power delay is very low. Full adder being the basic building block of all the circuits and it is important to reduce its power and delay. Over the years researchers have been focusing over the full adder only as it is the basic and the fundamental unit behind the building of all the circuit applications. To implement out the 1-bit full adder, different logical methods were being researched out where each method has its own benefits and issues. There have been two designs that have been investigated out so far. They are as follows:[16]
1) Static style
2) Dynamic style.
The static adders are the one which are efficient with simple design and less requirement of power along with more reliability. But the area required for the chip is very large as compared to the dynamic adders.[17]

A. Existing full adder module

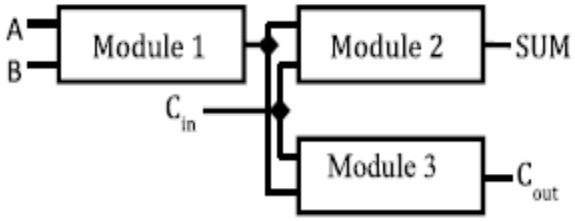

Figure 1. Block Diagram of Full Adder

The proposed circuit of full adder is represented by three blocks as shown in Fig. 3.3.1 Block 1 and block 2 are the XNOR blocks. These two blocks are responsible for generating the SUM(sum signal) and block 3 generates the Cout(output carry signal). Each and every block is designed in such a way that whole circuit of adder works in an optimized manner. The delay, power and the area results are always in the favor.
Each block is discussed in details below:
A) XNOR Block
In our proposed circuit of full adder, the function of the XNOR module is to consume the power required for the operation of entire circuit. Thus this block is designed in such a way that power is being consumed in the most optimized way and of course without the degradation of the voltage. Presented below is the Fig.2 which clearly shows the modified version of the XNOR circuit. This circuit consumes reduced power with the help of the use of weak inverter. In these inverters the channel width of the transistors tends to be small. The transistors here are Mp and Mn1 [1].

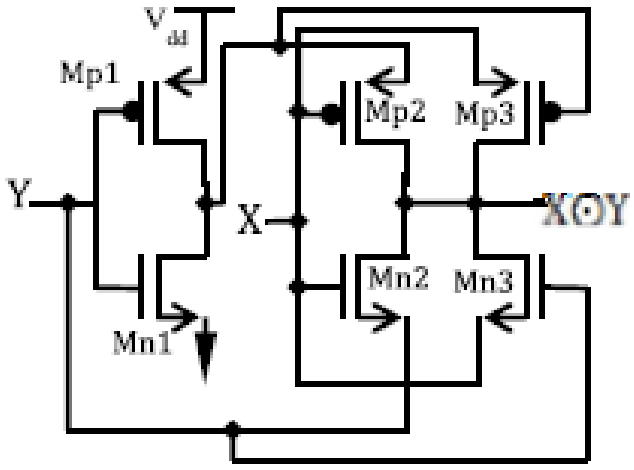

Figure 2. XNOR block

In our design, the XNOR block has employed 6 transistors but the arrangement of the transistors is done in a different manner. This XNOR offers very low power and in return high speed when compared with the conventional 6 T XOR-XNO implementation.
B) Carry Generation Block
In the existing circuit, the transistors Mn8, Mp8, Mp7, and Mn7 are used for the output carry signal. There is a single transmission gate Mp7 and the Mn7 through which the input carry signal i.e. the Cin propagates out. This way the complete carry propagation path is reduced significantly. Then, the stronger transmission gates being used which are having larger width of the channel are used to further reduce the delay in the propagation of the carry signal. These transistors are Mn7, Mp7, Mn8, and Mp8.[2]

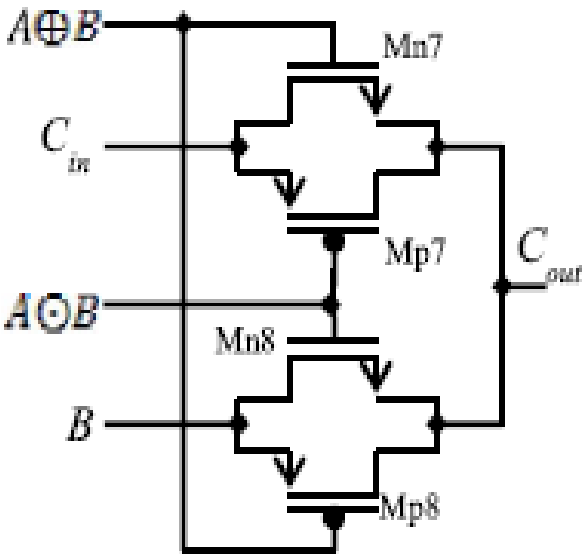

Figure 3. Carry Generation block

V. CONCLUSION

We have discussed various logical techniques of full adder and parameters like power delay and power delay product for its improved performance further work can be done on reducing power consumption and delay for high speed so it can be more efficient to work on various applications.

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