Scientific Journal of Impact Factor (SJIF): 5.71

e-ISSN (O): 2348-4470
p-ISSN (P): 2348-6406

International Journal of Advance Engineering and Research Development

Volume 5, Issue 04, April -2018

IMPLEMENTATION OF PRIMARY SYNCHRONIZATION SIGNAL DETECTION IN LTE

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Abstract: *Long Term Evolution (LTE) is an advanced Standard for the Mobile communication Systems and it is developed by Third Generation Partnership Project(3GPP).Synchronization is the Important Component of Practical Communication System . Primary Synchronization Detection is the primary task in Receivers . This paper presents Implementation of low power, High speed Primary Synchronization detection in Xilinx Vertex FPGA . A high Performance Primary Synchronization Signal detection is derived.. This offers a new synchronization system for low power and minimal effort outline. The reduction of the complication of the fundamental synchronization signal for LTE can attain by the proposed algorithm.*

Keywords- *LTE, Orthogonal frequency division multiplexing, primary synchronization signal (PSS), centrally symmetric matched filter, Low power, low cost.*

I. INTRODUCTION:

The fast development of phone users and the increasing interest for broadband wireless communication has prompted the advancement of LTE to supplant the wideband code division multiple access (WCDMA)- based air interface by the third Generation Partnership Project (3GPP). A few least prerequisites of LTE incorporate packet information support with top information rates of 300 Mbps in the downlink and 75 Mbps in the uplink, a maximum lower latency of 10 ms MAC layer round trip delay, and adaptable data bandwidth adaptability. These prerequisites result to the advancement of orthogonal frequency division multiplexing (OFDM)- based multiple access and modulation, multiple-input-multiple-output (MIMO) antenna plans, and versatile adjustment and coding with cutting edge channel coding, space time coding and cross breed programmed rehash request (ARQ) conventions.

In communication, synchronization is a critical task. It is utilized to secure the physical cell identity (PCI) or Cell ID which can be additionally utilized as a component of cell determination, handover techniques and channel estimation. The two synchronization signals utilized here are Primary Synchronization Signal (PSS) and Secondary Synchronization Signal (SSS). To expand unwavering quality and to keep up communication in remote to be well grounded and commendable data rate, a Multiple input multiple output (MIMO) briefs that the receiver and transmitter contains in excess of one antenna. To meet the synchronization a standout amongst other strategies is that the received signal underneath blurring atmosphere has been used amid the past in purposes that require a larger information. Orthogonal frequency division multiplexing is powerful in such a case.

A devoted synchronization channel is suitable in LTE for transmitting two synchronization indicators, the Primary Synchronization signal (PSS) and the other one Secondary Synchronization Signal (SSS)[6]. Inside the PSS basing 62 subcarriers every succession are synchronized to get mapped on 62 subcarriers found symmetrically around the DC-supplier. They are transmitted inside the two OFDM symbols of the first and 6th sub-frame (sub-frame record 0 and 5), i.e. each 5ms. The PSS sign incorporates Zadoff-Chu sequences in frequency zone which are orthogonal, i.e., their dot product is zero and are at 90 degrees to each other. Each arrangement compares to a division identity Ns = 0, 1 or 2 inside a group of three parts (physical cell). UE's at the cell edge would encounter a composite channel from a few cells, which would impact in channel appraises that don't mirror the individual channels to the particular cells if there was once just a single cell-common PSS. Subsequently, 3 unique PSS signals are delineated, more every now and again than not to be relegated all together that neighbor cells can utilize special PSS indicators [7].

The downlink frame structure of the LTE framework is appeared in Figure 2. Every radio frame (10 ms) is separated into 10 sub-frame of 1 ms. Each sub-frame comprises of 2 slots. There are 7 OFDM symbols for every slot. There are two sorts of synchronization channels primary and the other one, secondary Synchronization Signals that are time division multiplexed. Every radio frame contains two equivalent separated sets of PSS and SSS symbols. For identification of Symbols , PSS and SSS are set neighboring to one other in the last two OFDM symbols of the principal slot inside a sub-outline [7]. So as to give great timing detection execution, the synchronization sequence in UMTS frameworks ought to have great auto-

connection. Because of this property, the Zadoff Chu sequences were picked as the synchronization sequence for UMTS frameworks. For LTE frameworks, the synchronization succession is drawn to the focal band of whole bandwidth due to the OFDMA based downlink air interface.
In this paper, we propose designs for PSS Synchronizer that have been actualized in Verilog HDL. The functional simulation and the synthesis are performed by using XILINX ISE. The execution of our proposed designs is assessed on the basis of two purposes, which are the area utilization and the timing.

II.LITERATURE REVIEW :

A. Synchronization Signals in LTE System

Synchronization Signals in LTE System. The data of physical cell identity is done by Synchronization Signals which are named as PSS And SSS. PSS gives the Physical Layer ID(NCellID 2) or Physical cell Identity and SSS gives the Physical cell Identity Layer Or Cell Group ID(NCellID 1) .They are 3 varieties of NCellID 2 esteem, which are [0, 1, 2], while NCellID 1 has 168 varieties which are [0 • • • 167]. Hence, there will be 504 varieties of estimation of PCI (3*168 = 504). From the estimation of NCellID 1 and NCellID 2, the estimation of PCI can be resolved as below.

$$PCI = (3 * NCellID_1) + NCellID_2 \quad (1)$$

According to LTE standards PSS is located at the seventh symbol of each half-frame and the SSS is located at the sixth symbol. Their positions on the frame structure is shown in figure :

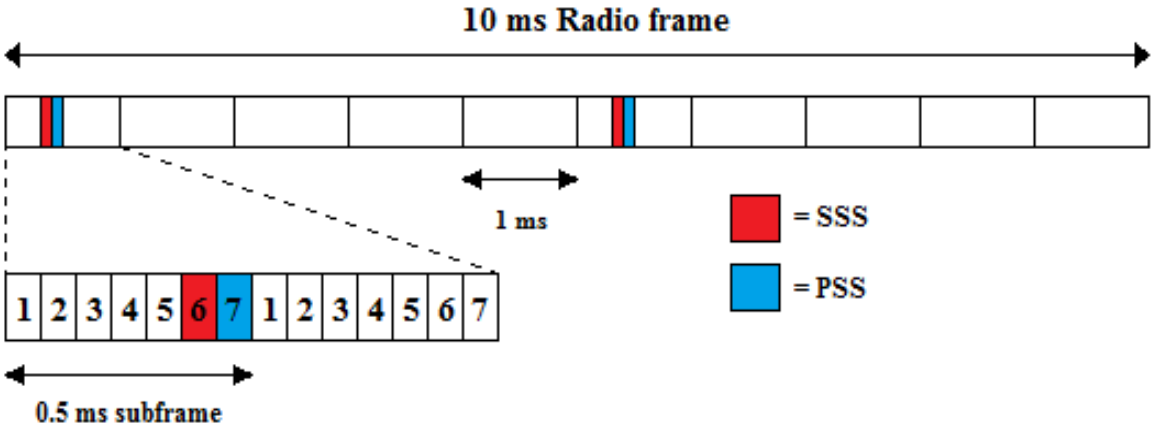

Figure 1.Radioframe

B. Primary Synchronization Signal (PSS) Generation

PSS are derived from the zadoff_chu Sequences in The Frequency Domain which has consistent amplitude zero auto relationship (CAZAC) sequence. This zadoff chu sequences are utilized in light of the fact that it has a decent correlation result. Three root file esteems are characterized for PSS, which are 25, 29, and 34, every one of which compares to the sector ID 0, 1, and 2 [4].
The Mathematical Equation for to obtain the Values of PSS is defined as

$$d_u(n) = \begin{cases} e^{-j\frac{\pi un(n+1)}{63}} & n = 0, 1, \cdots, 30 \\ e^{-j\frac{\pi u(n+1)(n+2)}{63}} & n = 31, 32, \cdots, 61 \end{cases} \quad (2)$$

Where the value u is the root index that differs the PSS as shown in Table I.

TABLE I RELATION BETWEEN NCELLID 2 AND ROOT INDEX IN PSS GENERATION

$N_{ID}(2)$	Root Index u
0	25
1	29
2	34

The Equation (2) will make 3 sets of PSS value, respectively PSS0, PSS1, and PSS2, each of which has 62 values. Every set of PSS values corresponds to the NCellID 2 number or physical layer ID [0, 1, 2].

III.PROPOSED SYSTEM DESIGN

A.Architecture Design Methodology :

To get the data of NCellID or Physical cell identity, past examinations have given a few purpose of perspectives, as portrayed. We selected that each PSS and SSS has their own coveted yield which is unique and have a tendency to be independent. In this paper for the most part to get the coveted yield from PSS is NCellID 2 (physical layer ID). Similarly, the coveted yield from SSS is NCellID 1 (cell aggregate ID). After these two have been done, the last calculation can be performed to discover physical cell identity. The major perform of the PSS is to identify the limit of a frame the position non-coherent identification approach desires to be utilized on the beneficiary for the reason that there will not be perceived reference at first. The typical non-coherent detection approach is coordinated channel that might be used to notice PSS successfully. The arrangement is given to the subcarriers round DC and changed over to time subject with the help of 64-component IDFT. To perceive this signal on the receiver, the relationship with the time field signal of the ZC sequence is figured in(2). Where W is DFT matrix.

$$C_u(m) = (W^H d_u)^H y \qquad (2)$$

Where W is DFT matrix, y is the progressive 64-by-1 received vector, and du is 64-by-1 vector made out of du (m) is punctured at DC.
Then, from (2), the coefficients of the matched filter can be obtained in (3)

$$coeff = (W^H d_u)^H \qquad (3)$$

Where

$$coeff = [coeff(63) coeff(62) .. coeff(1) coeff(0)]$$

and the matched filter can be expressed

$$MF = \sum_{k=0}^{63} coeff(k) y(t-k)$$

$y(k)$ is the received signal.

As of the power utilization conviction, additional power is dropped for a 10-bit simple to digital change than a 1-bitADC, as 10-bit pipelined ADC has a couple of amplifiers in it. To have course towards low-power choice, Primary SS recognition approach using 1-bit ADC is proposed. At each 10ns the adjustment in synchronization signal happens. The rate of sampling of the recipient is 122.88 MHz; anyway, the date cost of entered information to the matched filter is 1.92 MHz [9]. Hence, 9600 examples should be buffered by method for the matched filter as yield for each 5ms, which isn't subject and cost viable. To outfit you with a low rate choice, a procedure of down-sampling by the utilization of eight is utilized on the yield of matched filter. Fundamental synchronization signal is intended for mobile search and handover in 3GPP LTE ways, that is

transmitted each 5 ms. Search time of PSS recognition is a primary criteria when estimating its efficiency[10]. As discussed previously about Multiple info and Multiple yield in LTE, the expectation is that that there are four receiving antennas and four transmitting antennas in the simulated LTE MIMO procedure.

B.H*ardware implementation of matched filter :*

In PSS detection the correlate detection has key significance which is gained by Matched Filter. The Matched Filter is an overwhelming aspect inside the PSS recognition. A 64 tapped matched filer set up ,which calculates sixty four precarious multiplications. Since 84 matched filters are necessary inside this system, a whole of 5376 things of multiplication is necessary, which is exorbitant rate and low effective in receiver part. The useful implementation of this matched filter may likewise be confounded. Exorbitant power utilization may bring about erroneous impact which result at receiver not to be aware of the right signal[11]-[12]. As of getting non-coherent nature of matched filter in the event that it impacts its result less affectivity of most vital synchronous identification.

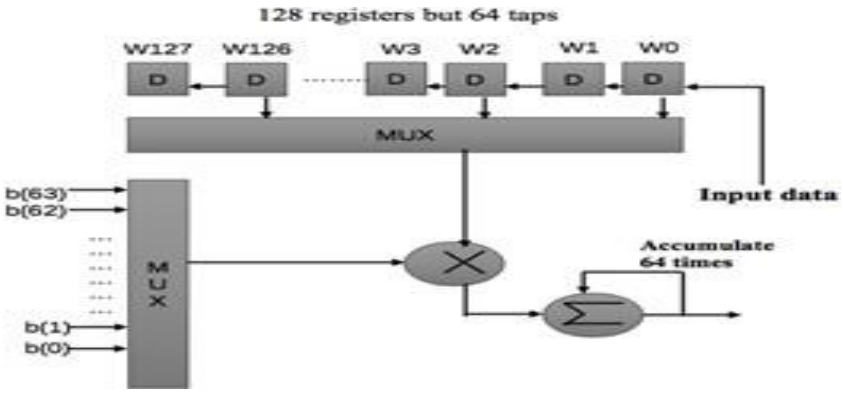

Figure 2. Matched filter.

With a specific end goal to overcome dealy the current matched filter architecture, a matched filter design that fuses parallel preparing is proposed. The proposed design is appeared in fig 3.Here the input information which is fed at 1.92MHz is handled parallelly. Hence, there will be no shifting of information amid each input clock. Because of it, the impact of propagation delay can be overcome.

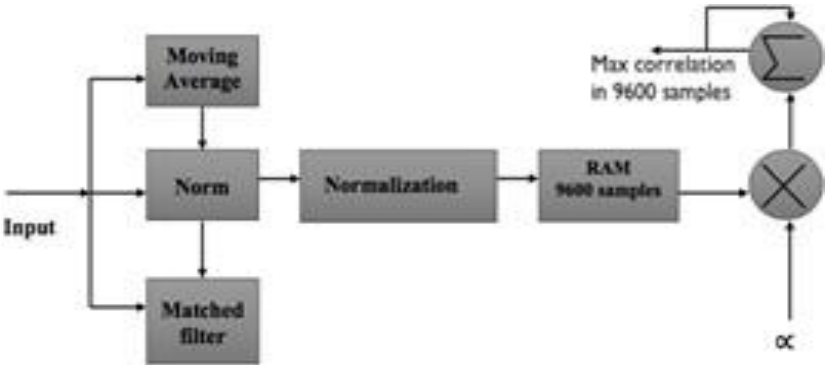

Figure 3. PSS detection architecture.

The above figure briefs the PSS design for detection which incorporates a single ram memory. This design is without down sampling where 9600 samples are to be stored by which makes area consumption increases

C .Area efficient PSS detection architecture

For the reason that 84 matched filters are required inside the framework, a total of 5376 units of complex multiplications is required, which isn't ought to for a sensible correspondence due to high cost of duplication unit in the collector. In practice, the inspecting cost of the data of the coordinated channel is 1.92 MHz while the clock is 122.88 MHz, which infers that only a single multiplication can be used all through 64 cycles instead of using sixty four units of troublesome duplications showed up in fig.2. Hence, 84 models of extend increases are acceptable for the complete procedure[13]. Thus, best 1200 relationship esteems must be secured in RAM with 1200 locations, which scale back the RAM estimation of the entire approach with the example of a portion of just about 8. This architecture is substantially more proficient than of the orthogonal structure is extensively productive than of the typical design, which diminishes the cost of the chip fundamentally[14]. From the power point of view, not only 10-bit ADC decreases the power utilization, yet the equipment of cutting edge reliability in addition does.

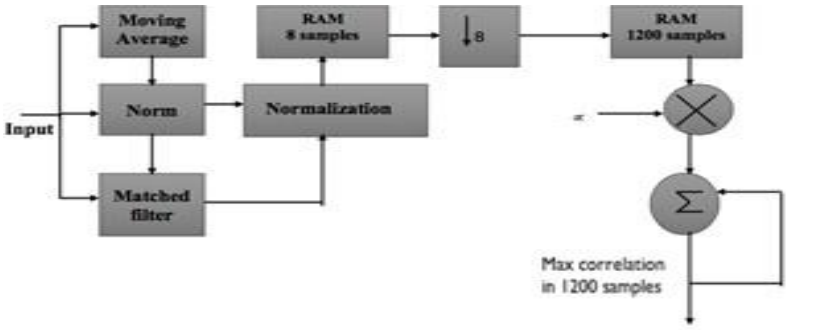

Figure 4. Area efficient PSS detection architecture

D.Modified area Efficient Architecture

The area efficient architecture is altered by changing matched filter design and making the PSS samples in to group to accomplish less complex multiplications. Subsequently delay of changed circuit diminishes which gives high performance. The above matched filter halfway symmetrically one. To go for low multiplication, the fundamental topic can utilize N-1 samples of PSS tests. For instance, if N=64, there are 62 centrally symmetric examples of the PSS signal. These sample sets may likewise be conveyed past to multiplication, so the matched filter can likewise be connected with the aid of lowered multiplications per single correlation.

The difficult multiplication can be lessened by using clustering the PSS samples, way gathering the comparative examples for expansion and after that go for multiplication.

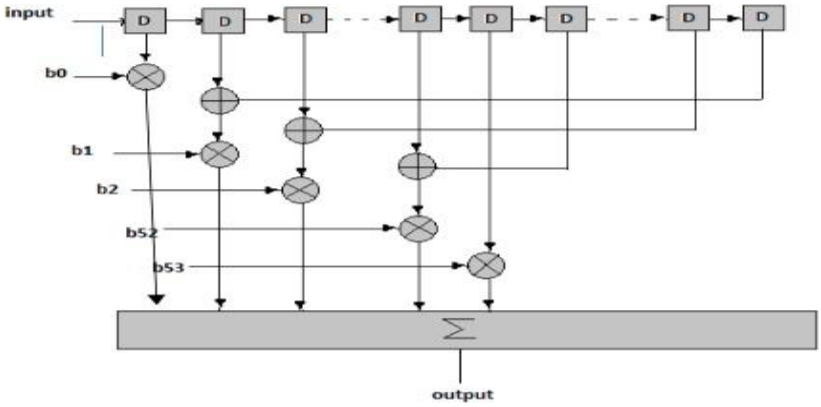

Figure 5. Centrally symmetric matched filter

IV.Results and discussion

The comparison of normal architecture of PSS detection with area efficient architecture, which included centrally symmetric matched filter in terms of area, power, delay are shown in the following table I, wave form result in Figure 6.

Architecture	Area	Power	Delay
Normal architecture	6343	2.646	5.212
Area efficient architecture	3282	0.828	5.136
Modified area efficient architecture	3437	1.104	4.582

Table I. Comparison of different architectures

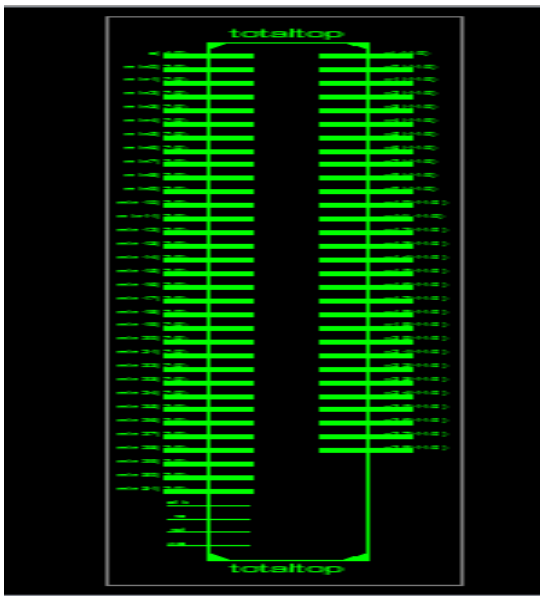

Figure 6. RTL Schematic Block representation

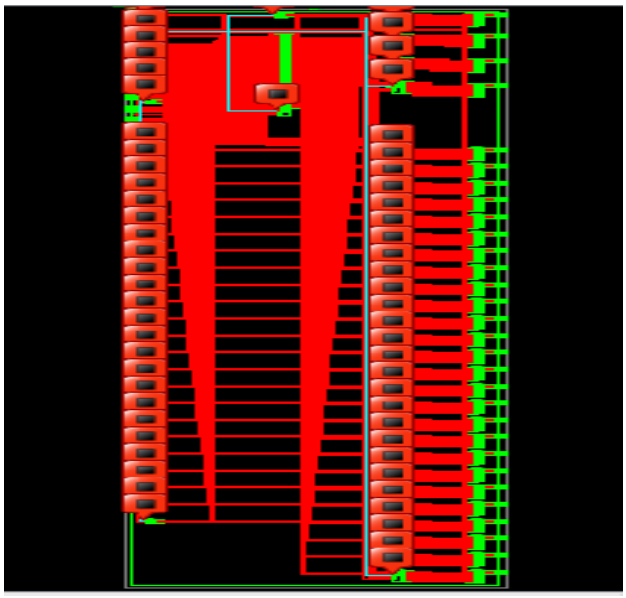

Figure 7.RTL schematic Technological view

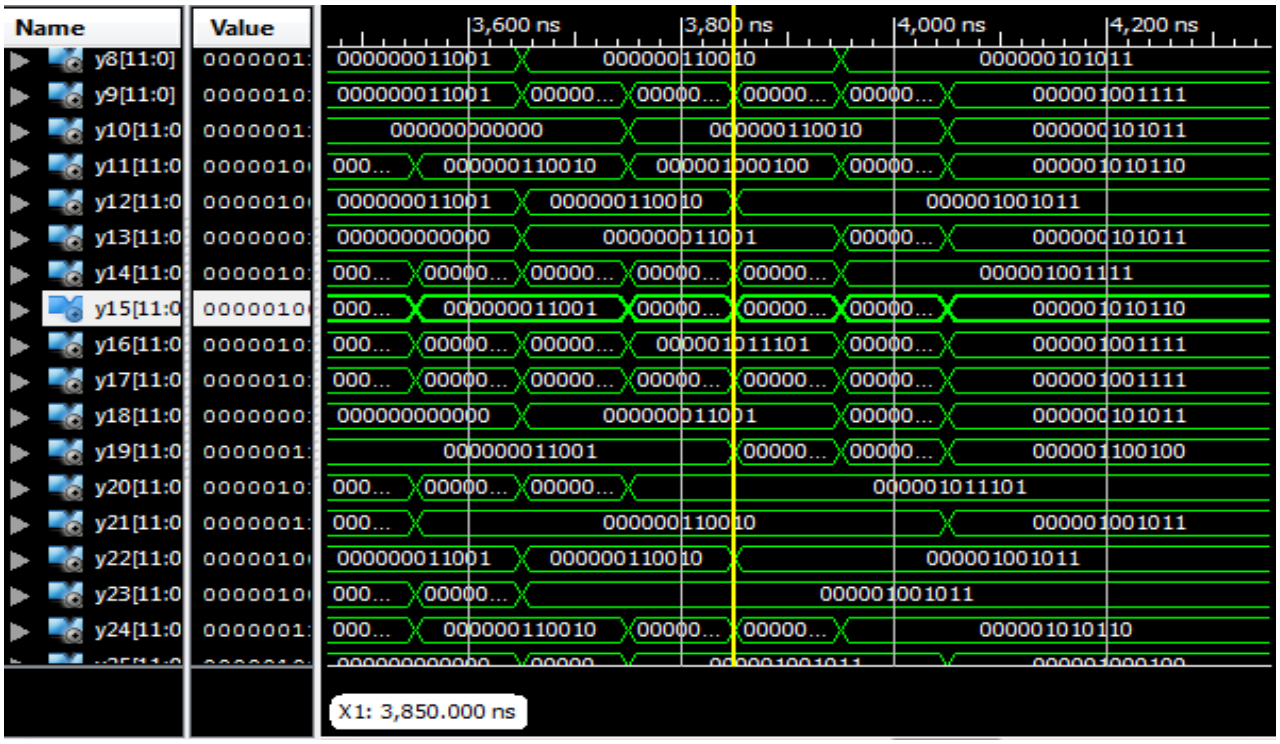

Figure 9. Waveform for modified area efficient architecture

V.CONCLUSION

This paper presents VLSI implementation of PSS detection in LTE with excessive throughput MIMO OFDM transceiver. As the discipline and energy consumption of the general implementation structure are too significant acceptable, and to put into effect, so a more functional implementation structure is proposed where PSS is detected efficiently. A centrally symmetric Matched Filter , which offers low matched filter design complexity, has been offered. The important symmetry allows for including symmetric samples prior to multiplication, thus minimizing the multiplication effort through half. For that reason a lot minimize power and low cost which renders it's viable within the implementation of UE chip.

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