

Design of 5-bit Flash ADC through Domino Logic in 180nm, 90nm, and 45nm Technology

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Abstract— In this paper high speed 5-bit Flash analog to digital converter (ADC) through Domino logic is designed in 180nm, 90nm, and 45nm CMOS technology with sampling rate of 4GS/s. Domino logic allows rail to rail logic swing. It was developed to speed up the circuit. The physical circuit is more compact than previous design compare to power and delay. This can be used for high speed applications. Flash analog to digital converter is ideal for applications requiring very large bandwidth, but they consume more power than other ADC architectures and are generally limited to 8-bit resolution.

Keywords— Comparator, Encoder, Domino logic, Power, Delay.

I. INTRODUCTION

To convert analog information into digital information Flash ADC is one of the fastest methods. Flash ADCs are highly used in applications where large bandwidth is required such as radar processing, sampling oscilloscopes, data acquisition and satellite communication applications. Flash analog to digital converter have the highest speed of any type of ADC [1]. It is also called as parallel converter because of its parallel structure. It uses one comparator per quantization level (2^N-1) and 2^N resistor string. The reference voltage is divided into 2^N values, each of which is fed into a comparator. The comparator compares the input voltage with the each reference voltage value and results the binary output in terms of '0's and '1's at the output of the comparator that is called as thermometer code which consists of string of '0's and '1's. A thermometer code exhibits all zeros for each resistor level if the value of input voltage is less than the reference voltage and one's if the input voltage is greater than or equal to the reference voltage.

Block diagram of N-bit Flash ADC is shown in Fig. 1.

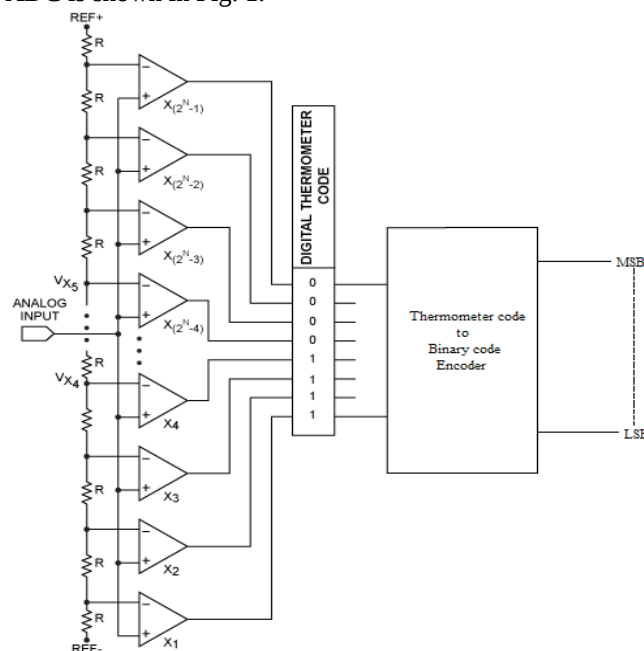


Figure 1:Block diagram of Flash ADC

The proposed Flash ADC is designed using Domino logic style for reducing the power consumption and increasing the speed as compared to the current mode logic style. Domino logic is presented in section 2. The design of proposed comparator using dominologic is presented in section 3. The design of proposed encoder using domino logic is presented in section 4. The analysis of proposed Flash ADC and simulation results are shown in section 5 and finally conclusion in section 6.

2. DOMINO LOGIC

Domino logic was developed to speed up circuits. Domino logic is a CMOS-based assessment of the dynamic logic techniques based on either PMOS or NMOS transistors. It allows a rail-to-rail logic oscillates. Cascade structure consisting of several stages each stage ripples the next stage for assessment, similar to a domino falling one after the other. The structure of Domino logic is shown in Fig.2.

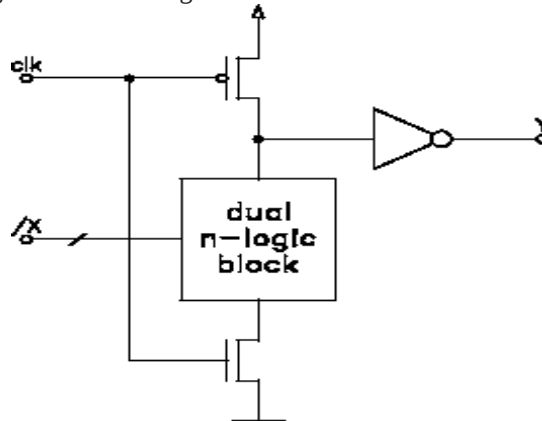


Figure 2 Basic structure of Domino logic

In dynamic logic, a problem occurs when cascading one gate to the next. The precharge "1" state of the first gate may cause the second gate to discharge prematurely, before the first gate has reached its correct state. This absorb the "precharge" of the second gate, which cannot be replace until the next clock cycle, so there is no recapture from this error. In order to cascade dynamic logic gates, one solution is Domino Logic, which inserts an ordinary static inverter between stages.

Domino logic consisting of the two phase when CLK=0 it occurs the "Precharge" phase, when CLK=1 it occurs "Evaluation" phase. In Domino logic input values is changed only during Precharge phase, if the value is changed during the Evaluate phase it can interrupt the output voltage.

3. COMPARATOR

Comparator plays a essential role in the design of an analog to digital converter [4]. Power dissipation, offset Speed, gain, and resolution are the important parameters of any type of comparators. The fundamental aim of the comparator is to compare an input signal (V_{IN}) with a reference signal (V_{REF}) and to produce an output logic low or logic high depending on whether the input signal is greater or smaller than reference. We have different architectures of comparator for Flash ADC namely differential comparator, dynamic comparator, double tail dynamic comparator, etc. In this paper we will take double tail dynamic comparator through domino logic as the reference model and try to optimize in terms of transistors.

This comparator is an extension of double tail comparator [2]. At the output side Domino logic circuit is added to the double tail comparator. Here the Out n is given to the one input and out p is given as another logic circuit. Considering the two stages of the circuit, at each stage the output will be taken, inverted and given as next stage input. The output of first stage and second stage considered as out1, out2 respectively. The proposed comparator is shown in Fig. 3.

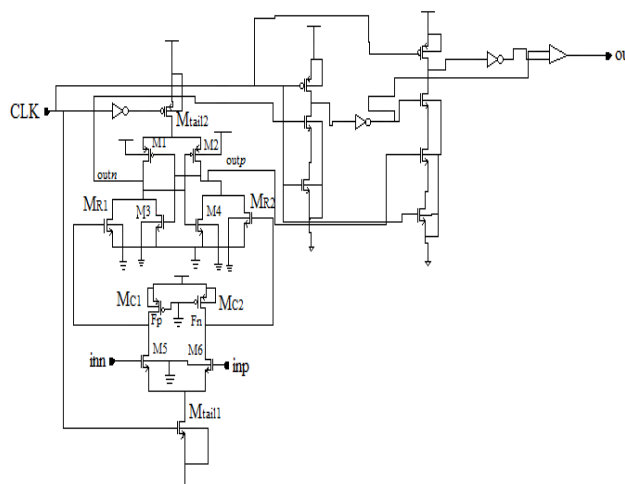


Figure 3 Double tail dynamic comparator through domino logic

The operation consists of two phases i.e. reset phase and comparison or regenerative phase. When CLK=0, the comparator is operated in Reset phase and CLK=V_{DD} the comparator is in comparison phase.

During reset stage i.e. CLK =0, M_{tail1} and M_{tail2} are off which overcomes static power consumption, M₃ and M₄ pulls both output nodes F_p and F_n to V_{DD}, hence transistors M_{c1} and M_{c2} are going to cut off. The transistors between input and latch stage (M_{R1} and M_{R2}), reset inverter latch outputs to ground/V_{SS}. While the comparator at decision making/comparison stage i.e. CLK =V_{DD}, then M_{tail1} and M_{tail2} are on and transistors M₃ and M₄ are turned off. Furthermore, at the beginning of this stage, the control transistors are still off where output nodes F_N and F_P are charged to V_{DD}. Thus, the nodes F_N and F_P starts to down with different charging rates based on the applied input voltages (V_{INN} and V_{INP}). Consider the case V_{INP}>V_{INN}, the node F_N drops faster than F_P, where transistor (M₂) gives high current than the transistor (M₁). As the node F_N continues to down for a long time, the corresponding PMOS or control transistor (M_{c1}) gets to turn on, and taking F_P node gets back to the V_{DD}. So, another PMOS control transistor (M_{c2}) remains turned off, which allows the node F_N to be completely discharge.

4. ENCODER

The comparators produce the output in a specific manner which is called thermometer code. The thermometer code is converted into binary code with the help of thermometer code to binary code conversion. The speed of the converter plays a vital role in the design of Flash ADC. For N-bit encoder requires 2^N inputs. Error handling capability and power dissipation are two vital parameters in the design of thermometer to binary code conversion [3]. Offset voltage in the comparator creates bubble error in the thermometer code. These bubble errors can reduce with the help of majority of '0's and '1's. So convert the thermometer code to gray code is one of the popular methods to reduce the bubble errors in thermometer code. We have different types of encoders for Flash ADC namely ROM encoder, fat tree encoder, multiplexer based encoder, etc. with different logic styles In this paper we will take thermometer code to binary code converter through domino lo as the reference model and try to optimize in terms of transistors . Block diagram of 4-bit Thermometer to binary code converter is shown in Fig.4.

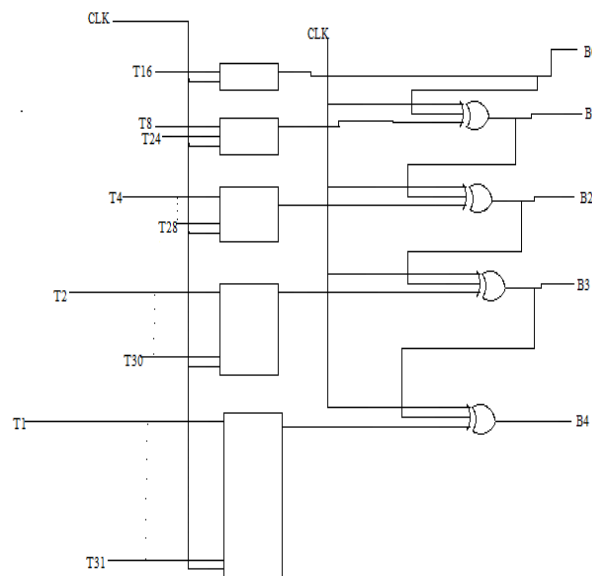


Figure 4 Block diagram of 5-bit Encoder

The equations between the thermometer codes to gray code is given below and derived from the truth table.

$$\begin{aligned} G_4 &= T_{16} & G_3 &= T_8 T_{24}' \\ G_2 &= T_4 T_{12}' + T_{20} T_{28}' & G_1 &= T_2 T_6' + T_{10} T_{14}' + T_{18} T_{22}' + T_{26} T_{30}' \\ G_0 &= T_1 T_3' + T_5 T_7' + T_9 T_{11}' + T_{13} T_{15}' + T_{17} T_{19}' + T_{21} T_{23}' + T_{25} T_{27}' + T_{29} T_{31}' \end{aligned}$$

The equations between gray code to binary code is given Below.

$$\begin{aligned} B_4 &= G_4 & B_3 &= G_3 \text{ XOR } B_4 \\ B_2 &= G_2 \text{ XOR } B_3 \\ B_1 &= G_1 \text{ XOR } B_2 & B_0 &= G_0 \text{ XOR } B_1 \end{aligned}$$

5. IMPLEMENTATION AND RESULTS

5.1. Comparator implementation

Fig 5 shows schematic of proposed comparator. From the Fig.5 we can see that the output buffers used at the output terminal is just to stabilize the output and bring it to logic level of either 0 or 1 depending on the output state.

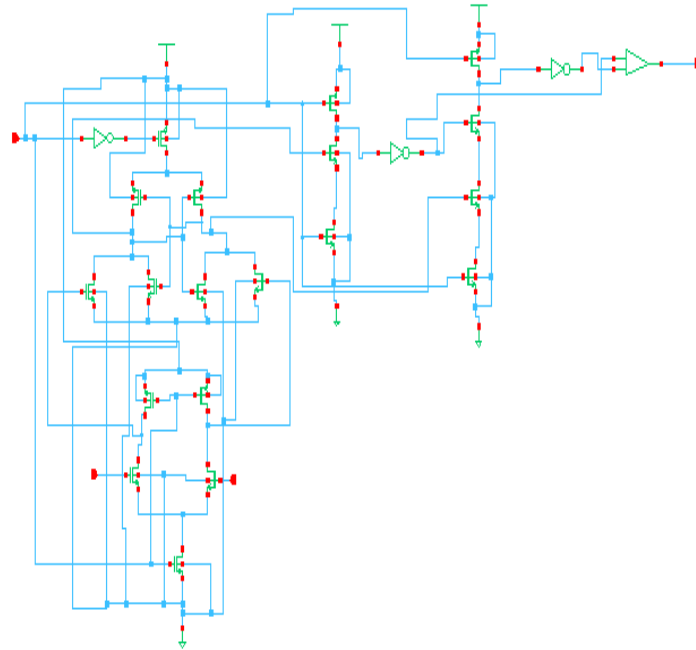


Figure 5 double tail dynamic comparator through domino logic schematic.

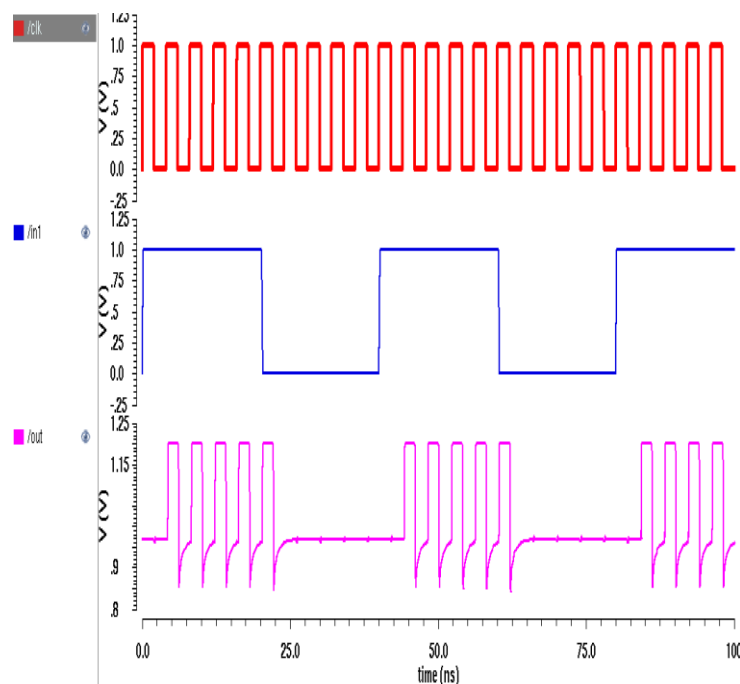


Figure 6 wave form of proposed comparator

5.2. Implementation of 5-bit Flash ADC

Flash analog to digital converter has the highest speed of any type of ADC. It uses one comparator per quantization level (2^N-1) and 2^N resistor string. The reference voltage is divided into 2^N values, each of which is fed into a comparator. Fig 7 shows the implementation of 5-bit Flash ADC.

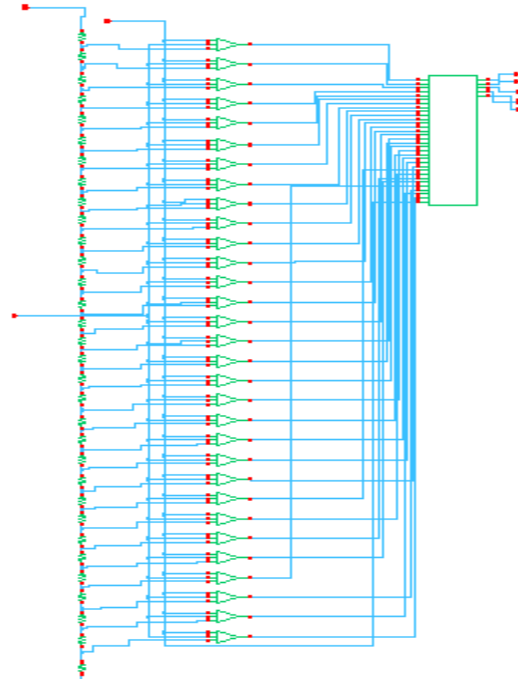


Figure 7 Schematic of 5-bit Flash ADC

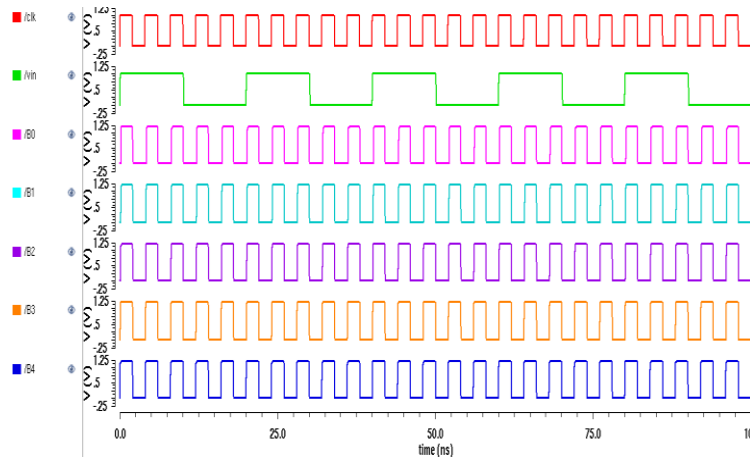


Figure 8 wave form of 5-bit Flash ADC

Table: Power and Delay of the Domino logic based 4-bit Flash ADC

Technology	180nm	90nm	45nm
Supply voltage	1.2v	1.2v	1.2v
Power	1.40uw	259.3nw	242.3nw
Delay	842.5ps	162.7ps	77.11ps
Sampling rate	250MHZ	250MHZ	250MHZ

6. CONCLUSION AND FUTURE SCOPE

Above circuits are implemented in 180 nm, 90nm, and 45nm technology using CADENCE Tool. The power dissipation for the proposed Flash ADC is reduced from in 180nm with 1.40uw to 45nm with 242.3nw. Also the propagation delay observed in proposed Flash ADC is 842.5ps with 180nm, which is further reduced in 45nm with 77.11ps. Offset voltage reduction can be a topic to work on in future to reduce the noise which gets incorporated to due to mismatch errors. Also further optimization can be done in order to reduce the number of transistors used in comparator design.

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