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Design and Verification of Dual Mode Logic (DML) for Power Efficient and High Performance

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Abstract — *The recently proposed dual mode logic (DML) gates family enables a very high level of power delay optimization flexibility at the gate level. In this paper, this flexibility is utilized to improve power efficiency and performance of combinatorial circuits by manipulating their critical and noncritical paths. An approach that locates the design's critical paths (CPs) and operates these paths in the boosted performance mode is proposed. The noncritical paths are operated in the low energy DML mode, which does not affect the performance of the design, but allows significant power consumption reduction. The proposed work is analyzed on 4bit carry skip adder, carry propagate adder, ripple carry adder and carry select adder. Simulations, carried out in a standard 180 nm digital CMOS process at different voltage levels V_{DD} from 1v to 1.8v, show that the proposed approach allows performance improvement along with reduction of energy consumption, as compared with a standard CMOS implementation.*

Keywords- *Dual Mode Logic, power efficient, high performance, critical paths, power-delay optimization.*

I. INTRODUCTION

The DML logic gates family was proposed in order to provide a very high level of power-delay (P-D) optimization flexibility. DML allows an on-the-fly change between two operational modes at the gate level: static mode and dynamic mode. In the static mode, DML gates consume very low power, with some performance degradation, as compared to standard CMOS gates. Alternatively, dynamic DML gates operation obtains very high performance at the expense of increased energy dissipation. A DML basic gate is based on a static logic family gate, e.g., a conventional CMOS gate, and an additional transistor. While DML gates have very simple and intuitive structure, they require an unconventional sizing scheme to achieve the desired behavior. This paper proposes to meet the delay requirements of CPs along with lowering the over-all power consumption of the design by utilizing the powerful modularity of DML. We propose and analyze a new approach, which locates the design's CPs and utilizes the on-the-fly modularity of DML to operate these paths in the boosted (dynamic) performance mode. The non-critical paths are operated in the low energy static DML mode, which does not affect the performance of the design. Since in most cases the majority of gates in the design are not on the CPs, the increase in energy consumption of the critical paths will be negligible in comparison to the general circuit consumption. Moreover, DML static gates dissipate less power than their CMOS counterparts, resulting in reduced power dissipation of the whole design.

II. DML OVERVIEW

A basic DML gate architecture is composed of an un-clocked static gate, e:g: CMOS, and an additional transistor M1, whose gate is connected to a global clock signal. In this paper we focus on DML gates where the static gate implementation is based on conventional CMOS. A DML gate implementation can be one of two: ``Type A" and ``Type B'', as shown in Figure 1(a-b) and Figure 1(c-d), accordingly. In the static DML mode of operation (Static mode), the M1 transistor is cut-off by applying the high Clk signal for ‘’Type A’’ and low Clk_bar for ``Type B" topology. Therefore, the gates of both topologies operate similarly to the static logic gate, CMOS in this case. For a dynamic operation of the gate (Dynamic mode), the Clk is enabled for toggling, providing two separate phases: pre-charge and evaluation. During the pre-charge phase, the output is charged to V_{in} ‘’Type A" gates and discharged to GND in ‘’Type B" gates. During evaluation, the output is evaluated according to the values at the gate inputs, in a similar fashion to NORA/np CMOS implementations. It was shown that DML gates have presented a very robust operation in both static and dynamic modes under process variations (PVT) and at low supply voltages. Dynamic mode robustness is mainly achieved by the intrinsic active restorer (pull-up in ‘’Type A’’ and pull-down in ``Type B"). This restorer also allows sustaining glitches, charge leakage and charge sharing. Unique sizing of the DML gate transistors is the key factor for achieving low energy consumption in the static DML mode (in which the topology of the gate is identical to the static gate). This sizing is also responsible for reduction of all capacitances of the gate. In a similar way, the unique transistor sizing enables evaluation through a low resistive network achieving fast operation in the dynamic mode. Power efficiency is achieved in the static DML mode at the expense of slower operation. However, the dynamic mode is characterized by high performance, albeit with increased energy consumption. These tradeoffs allow a very high level of flexibility at the system level. Figure 1(b) and Figure 1(d) show the footed “Type A” and the headed “Type B” DML gates, respectively. It allows successful pre-charge for a cascaded topology of standard Static gates\Synchronous devices to DML logic. Many aspects of DML gates

sizing, as well as preferred set of gates for ``Type A" and ``Type B" topologies, have been analyzed and discussed. The DML key achievement is that while presenting very high performance in the dynamic mode by the proposed sizing, the same topology also enables improved power efficiency in static mode, as compared to a conventional CMOS.

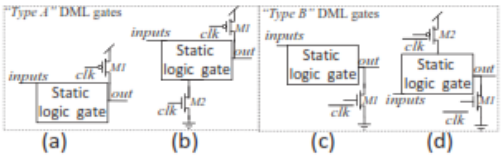
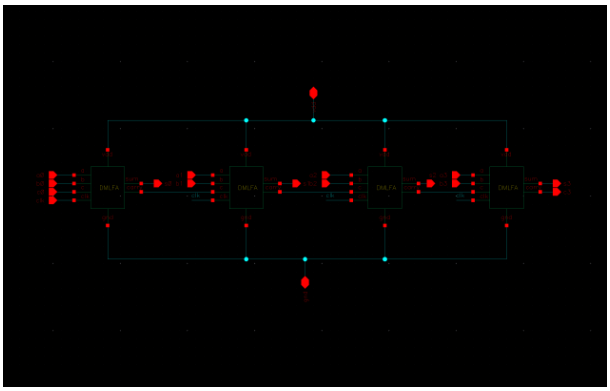


FIGURE 1 (a) General un-footed ``Type A'' DML gate (b) General footed ``Type A'' DML gate (c) General un-headed ``Type B'' DML gate (d) General headed ``Type B'' DML gate.

III. SIMULATION RESULTS

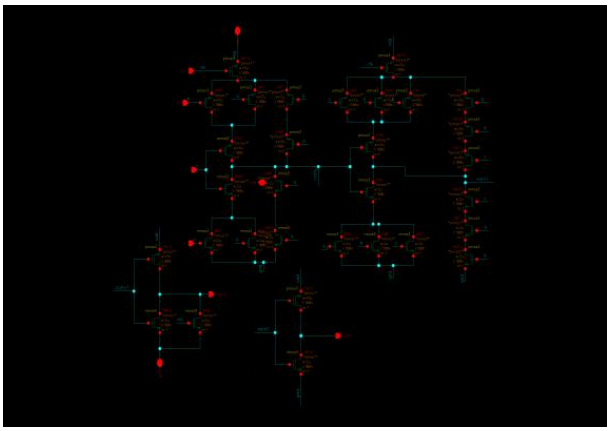
The modular benchmarks circuits, described in the previous section were simulated in a standard 180nm CMOS process, using the Spectre Cadence simulator. All energy and delay measurements are per-operation.

A. Ripple Carry Adder (RCA)



Block Diagram of the RCA

A full adder is a combinational circuit that performs the arithmetic sum of three input bits: augends Ai, addend Bi and carry in C_{in} previous adder. Its results contain the sum Si and the carry out, C_{out} to the next stage. This kind of adder is a "Ripple Carry Adder", since each carry bit "ripples" to the next full adder. So to design a 4-bit adder circuit we start by designing the 1 –bit full adder then connecting the four 1-bit full adders to get the 4-bit adder as shown in the diagram above.



Schematic of Full Adder

The Boolean equations of a full adder are given by:

$$S_{out} = ABC + AB'C' + A'B'C + BA'C'$$

$$= (AB'+BA')\,C + (AB+A'B')\,C'$$

$$S_{out} = A \oplus B \oplus C$$

$$C_{out} = AB + AC + BC$$

$$C_{out} = AB + C\,(A \oplus B)$$

Graphical view of Voltage VS Delay and Power

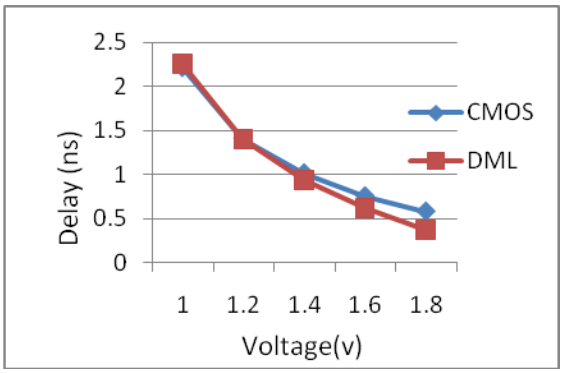


Figure: RCA Voltage Vs Delay

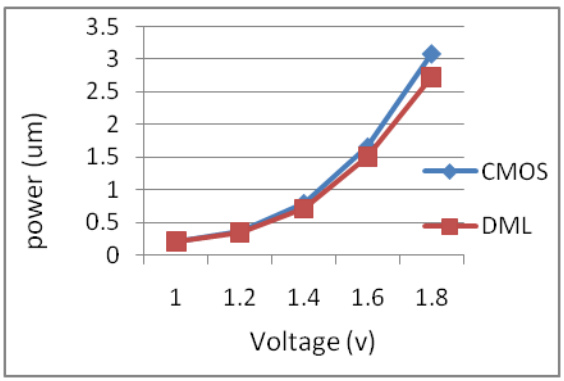


Figure: RCA Voltage Vs Power

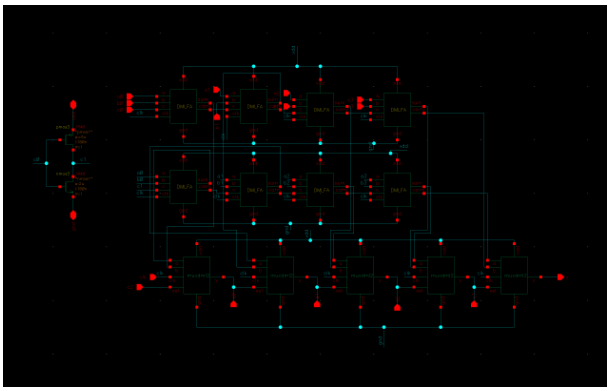
These two graphs show how the performance is increased and energy is reduced with the accordance of different voltages.

The below table shows that the comparison table of delay and power between the general CMOS and DML logic RCA. The DML RCA consumes less energy and gives high performance compared with the CMOS technology.

Comparison table between CMOS RCA and DML RCA

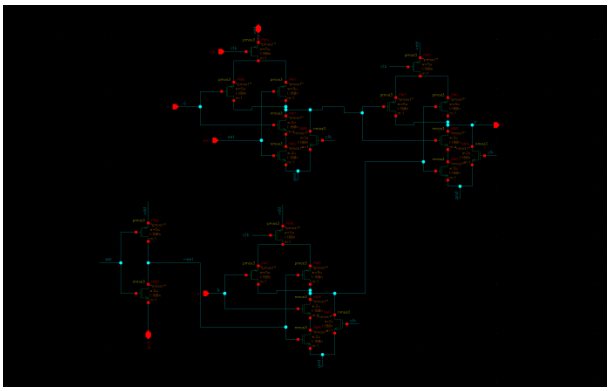
Voltage (V)	CMOS		DML	
	Delay (nS)	Power (µW)	Delay (nS)	Power (µW)
1	2.216	0.197	2.255	0.197
1.2	1.406	0.345	1.398	0.3416
1.4	1.015	0.7809	0.9423	0.7071
1.6	0.7547	1.647	0.619	1.501
1.8	0.5806	3.074	0.3738	2.726

B. Carry Select Adder (CSeA):



Block Diagram of the CSeA

The carry-select adder generally consists of two ripple carry adders and a multiplexer. Adding two n-bit numbers with a carry-select adder is done with two adders (therefore two ripple carry adders) in order to perform the calculation twice, one time with the assumption of the carry being zero and the other assuming one. After the two results are calculated, the correct sum, as well as the correct carry, is then selected with the multiplexer once the correct carry is known.



Block Diagram of MUX

Graphical view of Voltage VS Delay and Power

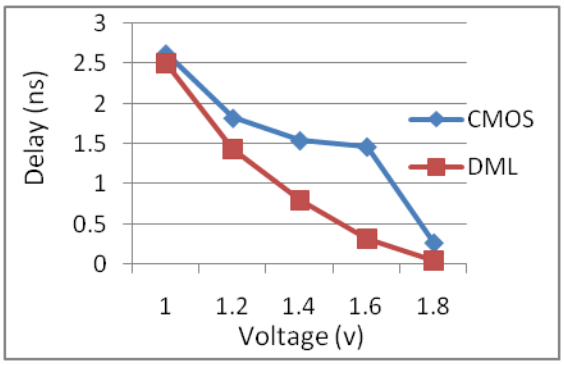


Figure: CSeA Voltage Vs Delay

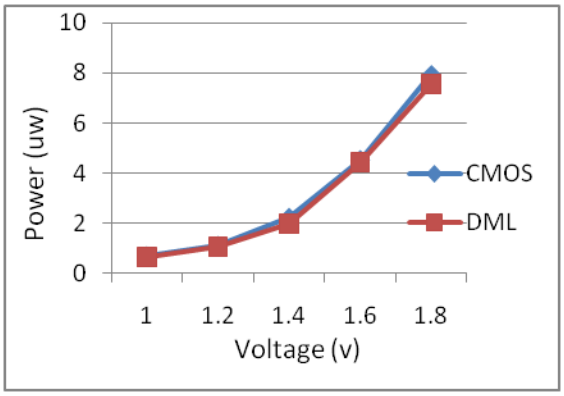


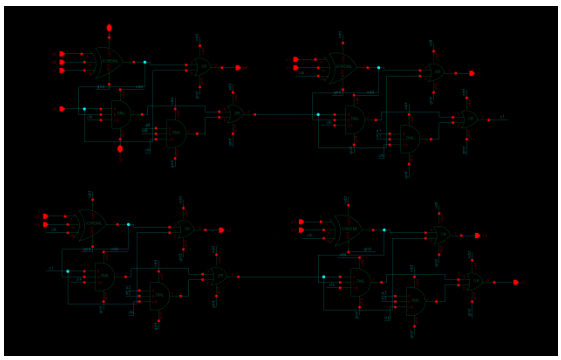
Figure: CSeA Voltage Vs Power

Comparison table between CMOS CSeA and DML CSeA

Voltage (v)	CMOS		DML	
	Delay (nS)	Power (µW)	Delay (nS)	Power (µW)
1	2.623	0.6982	2.501	0.641
1.2	1.819	1.114	1.433	1.052
1.4	1.539	2.24	0.7872	1.975
1.6	1.461	4.546	0.3153	4.436
1.8	0.2612	7.946	0.03923	7.551

C. Carry Propagate Adder (CPA):

Reducing the carry propagation delay of adders is of great importance. Different logic design approaches have been employed to overcome the carry propagation problem. One widely used approach employs the principle of carry propagation adder solves this problem by calculating the carry signals in advance, based on the input signals.



Block Diagram of CPA

Pi is known as the **carry propagate** signal since whenever P =1, the input carry is propagated to the output carry, i.e., *Ci+1 = Ci* (note that whenever *Pi* =1,*Gi=0*). ***Gi*** is known as the **carry Generate** signal since a carry (*Ci+1*) is generated whenever *Gi* =1, regardless of the input carry (*Ci)*.

Computed values of ***all*** the Pi's are valid one XOR-gate delay after the operands A and B are made valid. Computed values of ***all*** the G*i*'s are valid one AND-gate delay after the operands A and Bare made valid.

The Boolean expression of the carry outputs of various stages can be written as follows:

$$C_1=G_0+P_0C_0$$
$$C_2=G_1+P_1C_1$$
$$C_3=G_2+P_2C_2$$
$$C_4=G_3+P_3C_3$$

Graphical view of Voltage VS Delay and Power

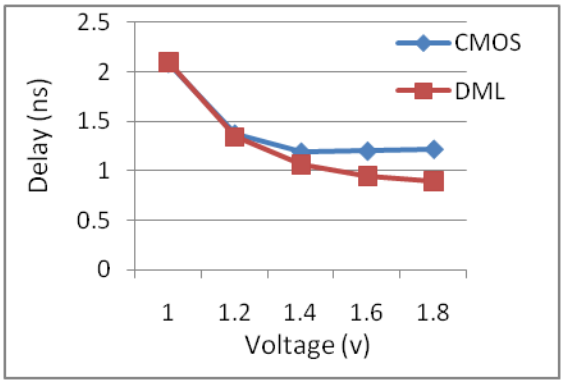


Figure: CPA Voltage Vs Delay

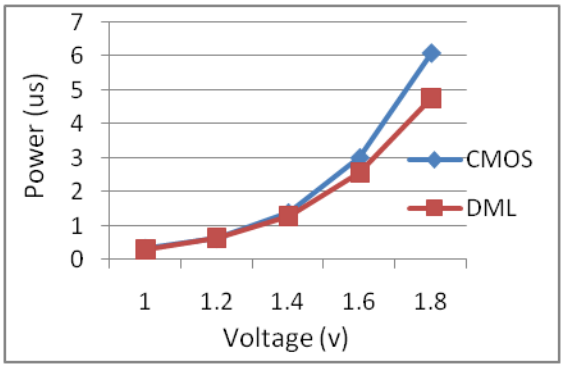
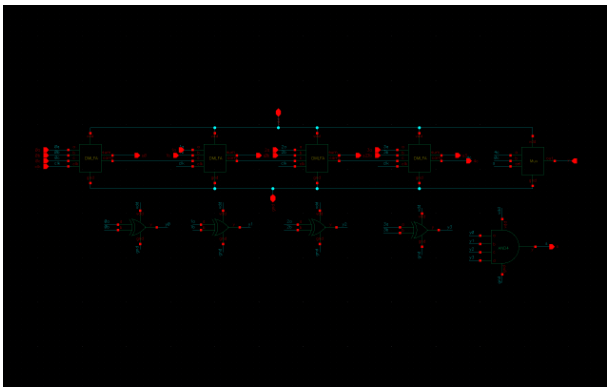


Figure: CPA Voltage Vs Power

Comparison table between CMOS CPA and DML CPA

Voltage (v)	CMOS		DML	
	Delay (nS)	Power (µW)	Delay (nS)	Power (µW)
1	2.081	0.3187	2.097	0.3047
1.2	1.368	0.6205	1.34	0.6393
1.4	1.186	1.372	1.06	1.291
1.6	1.195	3	0.9433	2.583
1.8	1.214	6.093	0.8923	4.764

D. Carry Skip Adder (CSA):



Block Diagram of CSA

The critical path of a carry-skip-adder begins at the first full-adder, passes through all adders and ends at the sum-bit $S_{n-1,}$ Carry-skip-adders are chained to reduce the overall critical path. The critical path for the skip logic in a carry skip adder consists only of the delay imposed by the multiplexer (conditional skip).

The number of inputs of the AND-gate is equal to the width of the adder. For a large width, this becomes impractical and leads to additional delays, because the AND-gate has to be built as a tree. A good width is achieved, when the sum-logic has the same depth like the n-input AND-gate and the multiplexer.

Graphical view of Voltage VS Delay and Power

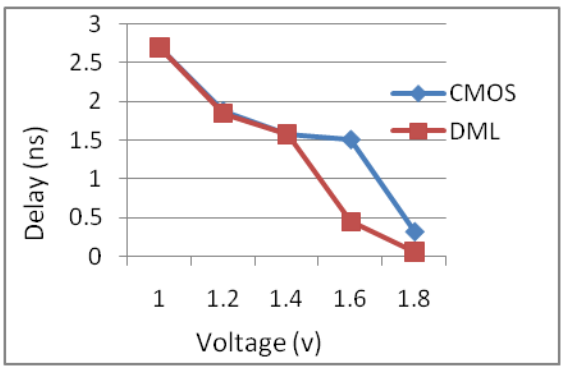


Figure: CSA Voltage Vs Delay

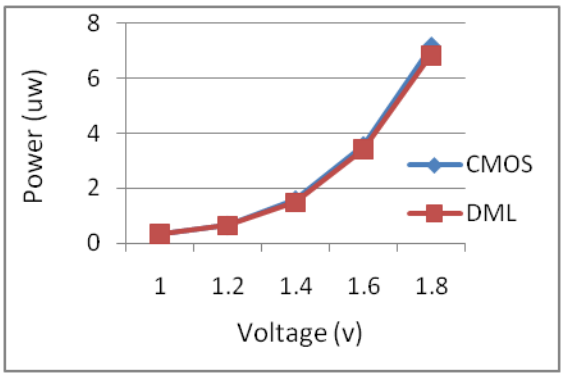


Figure: CSA Voltage Vs Power

Comparison table between CMOS CSA and DML CSA

Voltage (v)	CMOS		DML	
	Delay (nS)	Power (μW)	Delay (nS)	Power (μW)
1	2.694	0.3399	2.698	0.3371
1.2	1.874	0.6595	1.845	0.6517
1.4	1.572	1.58	1.576	1.498
1.6	1.504	3.551	0.4514	3.419
1.8	0.3155	7.16	0.05991	6.849

IV. ACKNOWLEDGMENTS

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V. CONCLUSION

Timing violation and energy minimization are important issues in all digital circuits. The invaluable possibilities, inherent to design with DML gates, leverage the flexibility of the design to meet timing along with reducing the total energy consumed by the circuit, as shown in this paper. Until now, meeting the timing was closely related to a rise in the consumed energy by conventional methods. In this work this paradigm is contradicted - both timing and low energy consumption requirements are met. We showed that the performance of the 180nm different adder's benchmark circuit was improved by, while also achieving reduction of energy consumption it is expected that these improvements will be even more significant for other designs.

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