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Design and Implementation of Low Power High-Speed 16-bit Arithmetic Units using different Multipliers in Cadence Virtuoso using 45nm technology

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Abstract— *A low power high-speed four Arithmetic Units are designed using different multipliers, each multiplier in each Arithmetic Unit. This project helps to choose a low power high-speed Arithmetic Unit in designing of different systems.AU stands for Arithmetic Unit, which is the main functional unit in most digital and high- performance systems The performance of Arithmetic Unit mainly depends on the performance of multiplier. The speed and area of the multiplier to be optimized is a major design issue. To determine the best solution for this problem is by comparing AU with different multipliers. Four different types of multipliers, Array, Wallace, Baugh-Wooley, Vedic multipliers were designed using half adders and full adders. Power and delay of Arithmetic Unit with different multipliers are compared. The working of AU using different multipliers helps to frame a better system with less power consumption and high speed. The entire design is done using CADENCE Tool with a power supply of 1V in GPDK 45nm technology***.***

Keywords— *Half Adder, Full Adder, Parallel Adders, Multipliers, Array Multiplier, Wallace Multiplier, Baugh-Wooley Multiplier, Vedic Multiplier, AU.*

I. INTRODUCTION

Exploitation of very large scale integration (VLSI) technology has developed to the point where millions of transistor can be implemented on a single chip. Complementary metal oxide semiconductor (CMOS) has been the backbone in mixed signal because it reducing power and providing good mix component for analog and digital design. An Arithmetic Unit (AU) is a Computation unit that performs various arithmetical operations such as Addition, Subtraction, and Multiplication. And that's why the AU is called the heart of microprocessor, microcontroller, and digital signal processor. To increase the efficiency of a multiplier numerous multiplication techniques have been developed to reduce the partial products and the methods of their addition but the principle behind multiplication remains the same in all cases. In signal processing applications, Multiplication is the most important arithmetic operation.

The efficiency of a system is determined by the speed of multiplier. The three main constraints which determine the performance of the system are speed, area and power requirement. This paper mainly concentrates on the performance of multipliers.

II. ARITHMETIC UNIT

An Arithmetic Unit (AU) is the main unit in Central Processing Unit that performs various arithmetic operations such as addition, subtraction, multiplication. The blocks in AU are Addition-subtraction block, multiplier block and a multiplexer. The addition-subtraction block performs both addition and subtraction by using a parallel adder and a selection line is used to select addition or subtraction to perform. Multipliers used in this are four different multipliers and the results from these blocks are given to the multiplexer. The blocks in AU are

A. Multipliers
B. Addition/Subtraction Block
C. Multiplexer

A. Multipliers

In this paper, four different multipliers are used. They are

a) ARRAY MULTIPLIER
b) WALLACE TREE MULTIPLIER
c) BAUGH-WOOLEY MULTIPLIER
d) VEDIC MULTIPLIER

These multipliers are designed using full adders and half adder's technique. Power and delay are the most important constituents for the performance of a multiplier. Power and delay are calculated and compared for these multipliers.

a) ARRAY MULTIPLIER

The structure of an Array multiplier employs an array of full adders and half adders. An n bit Array multiplier has n x n array of AND gates to generate partial products, n x (n-2) full adders and n half adders to the reference number, as in [13]. Each partial product bit is given to a full adder which sums the partial product bit with the sum from the previous adder and a carry from the less significant previous adder. The length of the multiplier in an array multiplier is denoted by no of rows and width of each row denotes width of the multiplicand. The 16 * 16-bit array multiplier is designed

using Cadence tool. The Multiplier circuit is designed using Full Adders and Half Adders. The block diagram of an 8-bit Array multiplier is shown in figure 1.

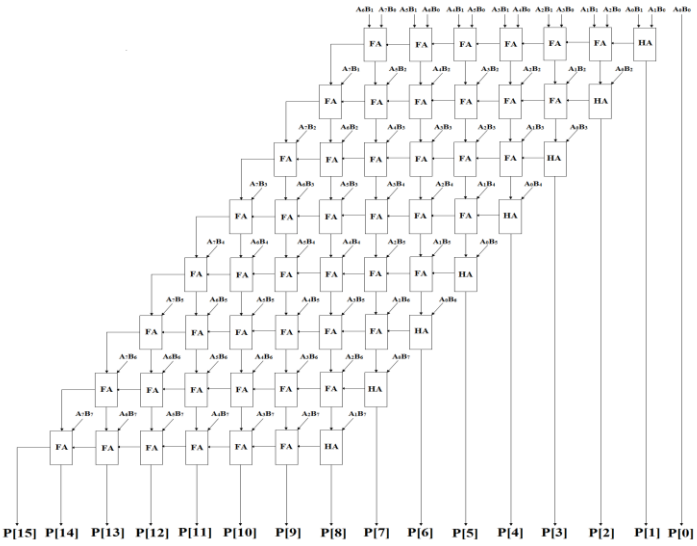

Figure 1: Block Diagram of Array Multiplier

b) WALLACE TREE MULTIPLIER

An efficient hardware implementation of a digital circuit that multiplies two integers is Wallace tree. But still, it is an efficient implementation of adding partial products in parallel to the reference number, as in [11]. The Wallace tree multiplier is faster than an array multiplier because its height is logarithmic in word size, not linear. Wallace Tree Multiplier using only full and Half Adders is employed in this. Wallace tree method is to reduce the number of adders by minimizing the number of the half adder in any multiplier. The first partial product is the least significant bit in the output of the multiplier result. After that, moving to the next column of the partial product if there are any adders from the previous product, the full Adder is used otherwise a half adder is used and so on. The block diagram of an 8- bit Wallace tree multiplier is shown in the below figure 2.

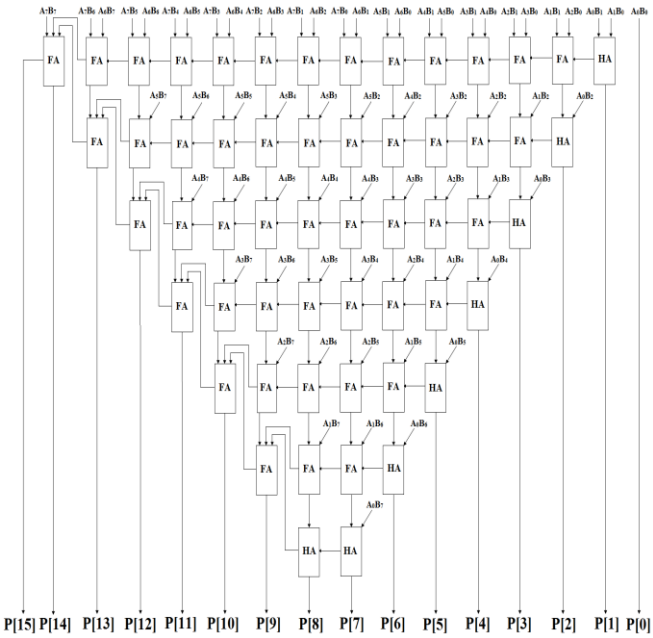

Figure 2: Block Diagram of Wallace Tree Multiplier

c) BAUGH-WOOLEY MULTIPLIER

Baugh-Wooley multiplier is designed and developed for the multiplication of signed numbers. It will multiply two's complement numbers.Baugh-Wooley two's complement Signed multipliers is the best-known algorithm for signed multiplication because it maximizes the regularity of the multiplier and allows all the partial products to have positive sign bits to the reference number, as in [1],[2]. Multiplying two's complement numbers directly, then each of the partial products to be added is a signed numbers. Thus each partial product has to be sign extended to the width of the final product in order to form a correct sum by the Carry Save Adder (CSA) tree. According to Baugh-Wooley approach, an

efficient method of adding extra entries to the bit matrix suggested avoiding having a deal with the negatively weighted bits in the partial product matrix. The block diagram of an 8-bit Baugh-Wooley multiplier is shown in the below figure 3.

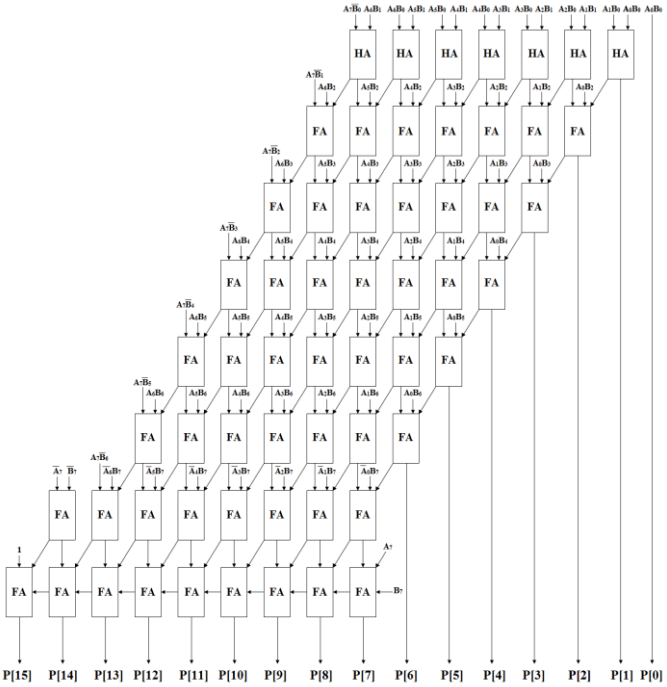

Figure 3: Block Diagram of Baugh Wooley Multiplier

d) VEDIC MULTIPLIER

Vedic Mathematics to the reference number, as in [9] is the ancient system of mathematics .contains techniques of calculations based on 16 Sutras. Using these techniques in the computation algorithms of the coprocessor will reduce the complexity, execution time, area, power etc. The main advantage of the Vedic multiplier is that it reduces delay as well as power when compared with the existing multipliers. This work has proved the efficiency of Urdhva Tiryakbhyam–Vedic method for multiplication. The meaning of UT is "Vertically and Crosswise" and the multiplication happens in this fashion. UT introduces a parallel execution of partial products and sums. The block diagram of an 8-bit Vedic multiplier is shown in the below figure 4.

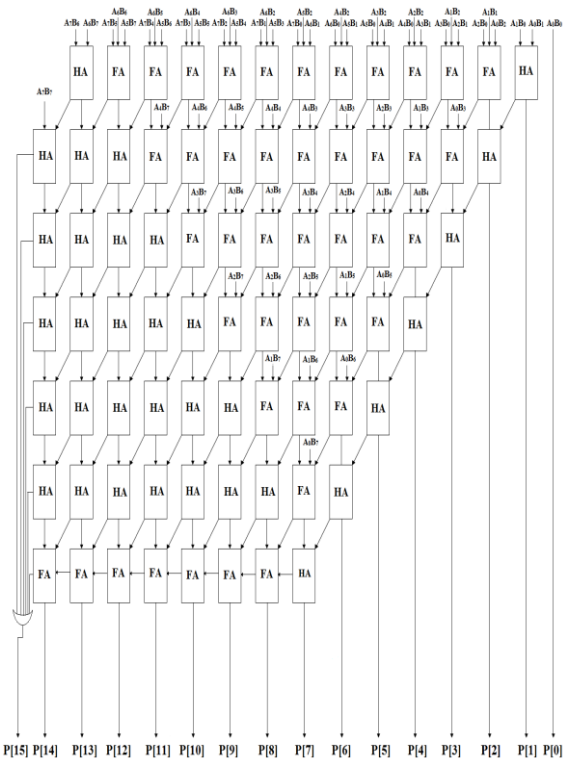

Figure 4: Block Diagram of Vedic Multiplier

B. ADD/SUBTRACT BLOCK

A parallel adder circuit is designed using a cascaded combination of full adders in the Parallel Adder . Likewise, bit parallel subtract or can be designed. For the purpose of optimization, we prefer using a single circuit to accomplish addition and subtraction operations. These two operations are performed using a single digital circuit i.e. a parallel adder or subtract or circuit. The subtraction process of binary numbers is nothing but their 2's complement addition. An n bit parallel Adder/Subtract or circuit using full adders is shown below figure 5.

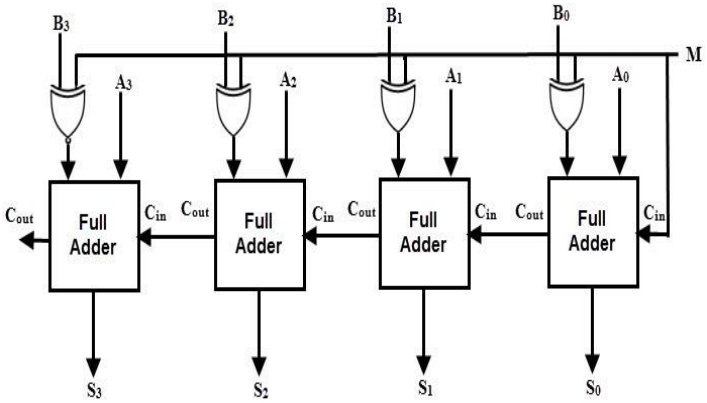

Figure 5:Parallel Adder/Subtractor Circuit

In the above circuit When M= 1, the circuit is a subtractor and when M=0, the circuit becomes adder. An addition operation is performed when the Ex-OR gate consists of two inputs to which one is connected to the B and other to input M. When M = 0, B XOR of 0 produce B. Then full adders add the B with A with carry input zero.The subtraction operation is performed when M = 1, B XOR of 0 produce B complement and also carry input is 1 to the reference number, as in[4],[3]. Then the complemented B inputs are added to A and 1 is added through the input carry nothing but a 2's complement operation.

C.Multiplexer

A multiplexer (mux) is a common digital circuit used to mix a lot of signals into just one. A multiplexer is the most important element in an AU. It selects any one output among two outputs generated from an AU depending upon the select line value and then reproduces it at the output terminal. Multiplexers are made out of logic gates.Every multiplexer has at least one select line, which is used to select which input signal gets relayed to the output. In a 2-to-1 multiplexer, there's just one select line. (2n inputs requires n select lines).a 16 bit 2:1 multiplexer is designed in the proposed Arithmetic Unit. a 2:1 multiplexer is shown in figure 6.

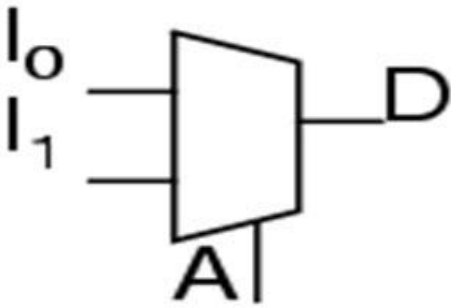

Figure 6.2:1 Multiplexer

III. PROPOSED ARITHMETIC UNIT

The proposed 16-bit Arithmetic Unit using four different multipliers is designed in Cadence Virtuoso in 45 nm technology.Arithmetic Unit's are replaced with four different multipliers in order to find the low power Arithmetic Unit. The schematics and results of the Arithmetic Unit are implemented.

Arithmetic Unit designed here is a 16 bit using different multiplier in each AU. They are

A) AU Using ARRAY Multiplier
B) AU Using WALLACE TREE Multiplier
C) AU Using BAUGH-WOOLEY Multiplier
D) AU Using VEDIC Multiplier

The Arithmetic Unit consists of three blocks, they are Addition, subtraction and Multiplication. The Outputs from these blocks are given to the multiplexer which mixes many signals to one. The multiplier block is replaced with the above multipliers in each Arithmetic Unit .power and delay are compared in order to choose a low power high-speed ALU.The block diagram of proposed Arithmetic Unit is shown in figure 7.

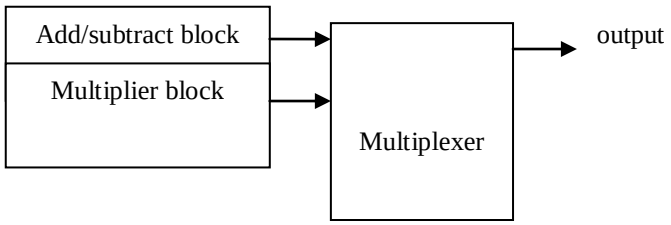

Figure 7.Proposed Arithmetic Unit Block

IV. RESULTS

The Arithmetic Unit using different multipliers are designed among those the Arithmetic Unit using Wallace multiplier is discussed below.

A.Schematic of AU using Wallace Tree multiplier

The Arithmetic Unit using WallaceTree multiplier shown in figure 8 consists of 16-bit Adder/Subtractor block and a 16-bit WallaceTree multiplier and these outputs are given to a 16-bit 2:1 Multiplexer.The Wallace Tree Multiplier is replaced with other multipliers in other Arithmetic Units.

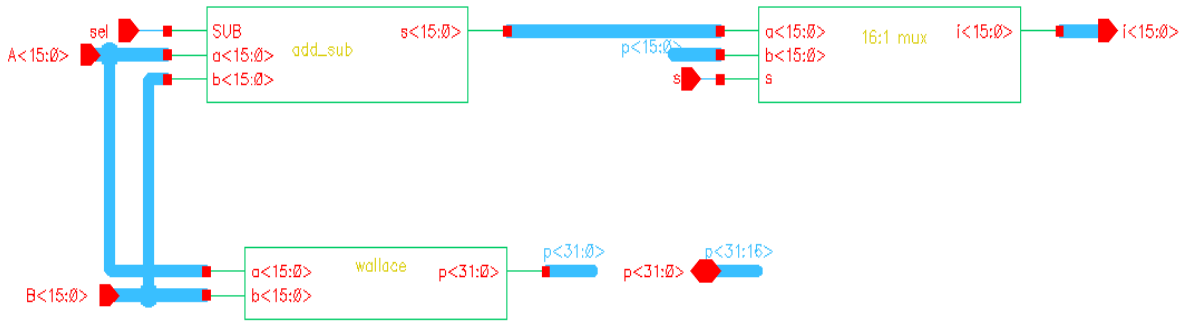

Figure 8. Schematic of AU using Wallace Tree multiplier

B.Output of AU using Wallace Tree multiplier

Arithmetic Unit using Wallace Multiplier consists of two 16- bit Inputs(a and b) and a selection line and one 16- bit Output shown in figure 9. The output is represented as (i).

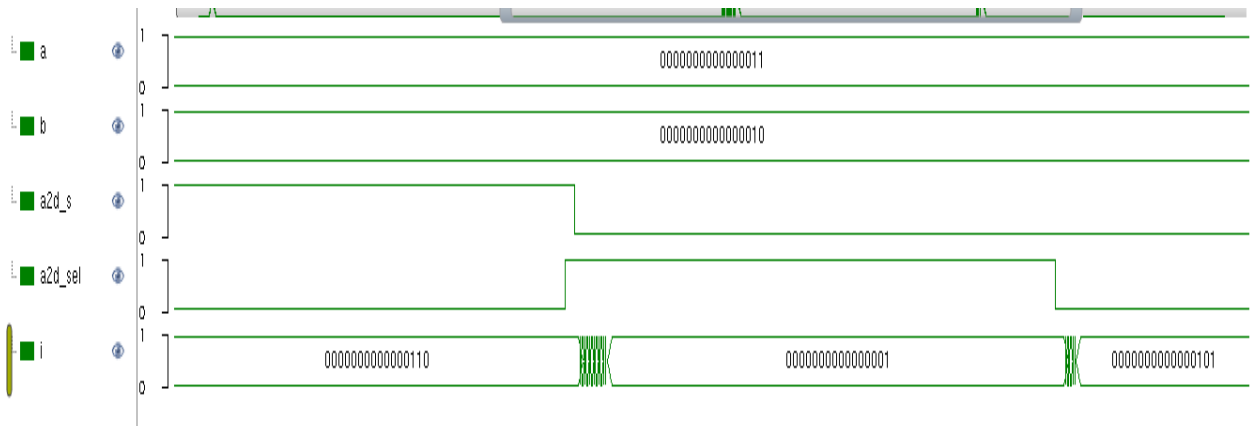

Figure 9. Waveform of AU using Wallace Tree multiplier

C.Power and Delay Calculations

Power and delay calculations of Multipliers and Arithmetic Unit using different multipliers are tabulated below in table I and II. In Table I power and delay of multipliers are compared.

Table I Power and Delay Calculation of Multipliers

Parameter	Array	Wallace	Baugh-Wooley	Vedic
Delay	292.8psec	169psec	291.8psec	291.5psec
Power	259.5nw	694.3nw	229.4nw	903.7nw

Table II Power and Delay Calculations of AU

Parameter	AU using Array multiplier	AU using Wallace Multiplier	AU using Baugh-Wooley multiplier	AU using Vedic multiplier
Delay	477.9psec	357.6psec	476.5psec	356.4psec
Power	44.67 µw	27.62 µw	27.93 µw	29.82µw

Power and Delay of Arithmetic units are tabulated in Table II. From Table II, it is evident that Arithmetic Unit using Vedic Multiplier has less delay and Arithmetic Unit using Wallace Multiplier has low power

CONCLUSIONS

The 16-bit AU using different multipliers has been proposed, designed, simulated and verified for their functionality using cadence virtuoso ADE spectre. Four 16-bit Arithmetic Units were designed, power consumption and delay are compared between the Arithmetic Units. These are designed using a power supply of 1V in 45nm Technology using cadence tools. The schematics are drawn using cadence virtuoso, schematic editor, symbol editor and while the simulations are done using Analog design environment (ADE L) Tools. By comparing the power consumption of each Arithmetic Unit and it helps us to choose a low power Arithmetic Unit in designing of different systems. The Arithmetic Unit using Wallace multiplier consumes power 27.62 µw and the Arithmetic Unit using Vedic Multiplier has 356.4psec delay. So this paper concludes that Arithmetic Unit using Vedic Multiplier is high- speed unit and the Arithmetic Unit using Wallace Multiplier is low power unit.

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