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Design and comparison of Low Power 64-Bit ALU using CMOS and Transmission Gate Logic

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Abstract —*Arithmetic and logical unit (ALU) is an important block of microprocessor. Now days for most of the applications of digital circuits the important attributes are minimizing power consumption and area whreas maximizing speed. The main aim of this project is to design 64 bit ALU with less number of transistors using fast complementary metal oxide semiconductor logic and Transmission gate logic. The Arithmetic and Logical Unit (ALU) is designed to perform all the Arithmetical and Logical operations, including bit shifting operation which is needed to be done for almost any data that is being processed by the Central Processing Unit (CPU). The proposed 64 bit ALU is designed and simulated in Cadence Virtuoso Tools in GPDK 45nm Technology.*

Keywords- *CMOS, ALU, Adders, Multiplexers, Subtractors, Transmission gate & all basic gates.*

I. INTRODUCTION

ALU Stands for Arithmetic and logical unit, an Arithmetic and logic unit is the heart of all the microprocessors. It is a combinational logic unit that performs logical or arithmetic operations.ALU is getting smaller and more complex nowadays to enable the development of a more powerfull but smaller computer. However there are few limiting factors that slow down the development of smaller and more comlex IC Chip. They are IC fabrication technology, Designer productivity and design cost. The ALU performs arithmetic operations (Addition,Subtraction,Mutiplication and Division) and logic operations. Logic operations test various conditions in countered during processing and allow for different actions to be taken based on the result. The data required to perform the arithmetic and logical functions are inputs from the designed Central Processing Unit (CPU) registers and operands. The ALU relies on basic items to perform its operations. These includes number systems, data routing circuits (adders/subtractors), timing, instructions, operands and registers figure. 1 shows ALU block diagram.

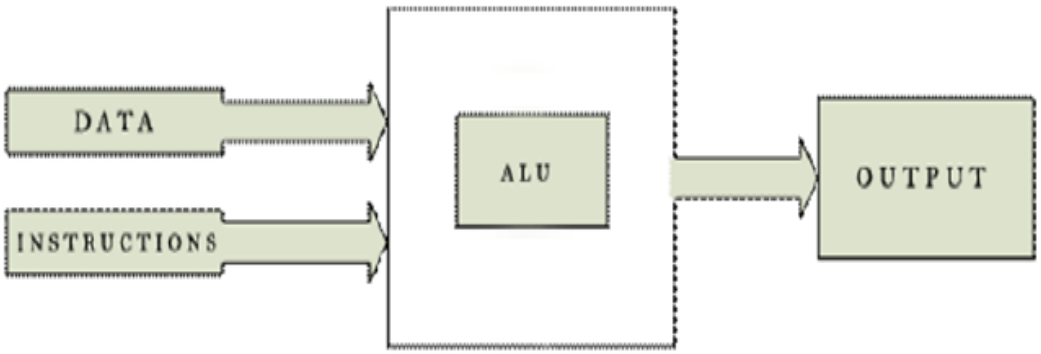


Figure 1: Block diagram of ALU

An ALU loads data from input registers, an external control unit then tells the ALU what operation to perform on the data and then the ALU stores its results into an output register. The control unit is responsible for moving the processed data between these registers, ALU and memory.

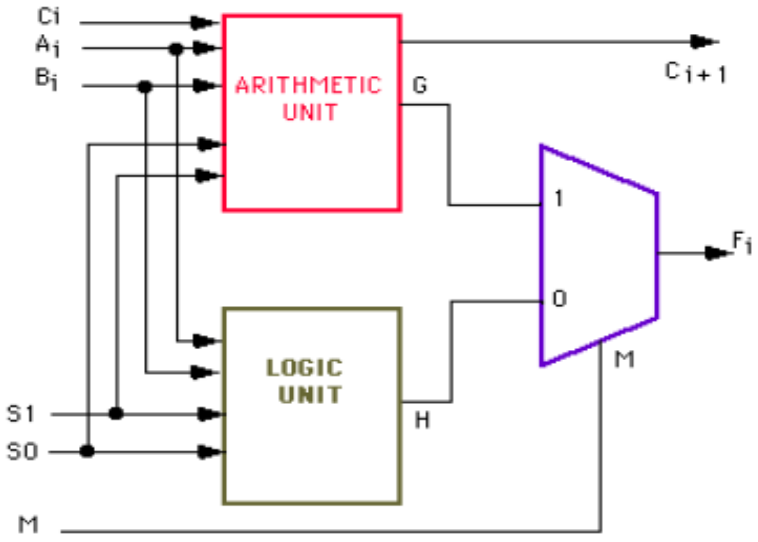


Figure 2. Architecture of ALU

The above ALU architecture shows its two sub blocks one is arithmetic unit and second one is logical unit the first block performs arithmetic operations and the second block will performs logical operations. Most of the ALUs can perform the following opertions:

Table 1. Arithmetic and logical operations

ARITHMETIC OPERATIONS	LOGICAL OPERATIONS
ADDITION	AND
SUBTRACTION	OR
MULTIPLICATION	NOT
DIVISION	NAND
REMAINDER	NOR
MODULUS	XOR
UNARY ADDITION	
UNARY SUBTRACTION	
EXPONENTIAL	

II. CMOS LOGIC

In CMOS technology while we design high speed 64 bit ALU, we have to take care about power dissipation. Power dissipation is the most critical parametre for portability & mobility and it is classified into dynamic and static power dissipation. Dynamic power dissipation occurs when the circuit is operational, while static power dissipation becomes an issue when the circuit is inactive or is in power down mode. There are three major sources of power dissipation in digital CMOS circuits, which are summarized as

$$P_{avg} = P_{switching} + P_{short\ circuit} + P_{leakage}$$

$$= (\alpha_0 \rightarrow 1 \times C_1 \times V_{dd}\, 2 \times F_{clk}) + (I_{sc} \times V_{dd}) + (I_{lekage} \times V_{dd})$$

The first term represents the switching component of power where C_1 is the load capacitance, F_{clk} is the clock frequency and α is the probability that a power consuming transaction occurs. The second term is due to the direct path short circuit current, Isc which arises when both the NMOS and PMOS transistors are simultaneously active conducting current directly from supply to ground. Finally leakage current, I_{lekage} which can arrives from substrate injection and sub-threshold effects is primaily determined by fabrication technology considerations [3]. The switching power in CMOS digital integrated circuits is a strong function of the power supply volage. Therefore reduction of Vdd emerges as very effective means of limiting the power consuption. However the saving in power consuption comes at a significant cost interms increased circuit delay. Since the exact analysis of propogation delay is quite complex, a simple first order derivative can be used to show the relation between power supply and delay time

$$T_d \alpha C_1 V_{dd} / k (V_{dd} - V_{th}) \alpha$$

K = Transistor aspect ratio (W/L)
Vth = Transistor threshold voltage
α = Velocity saturation index

III. TRANSMISSION GATE LOGIC

A transmission gate can conduct in both directions or block by a control signal with almost any voltage potential in analogous to that of relay. It is CMOS based switch in which PMOS passes a strong 1 but poor 0 and NMOS passes strong 0 and poor 1. Both PMOS and NMOS works simultaneously. In principle a transmission gate made up of two field effect transistors in which contrast to traditional discerete field effect transistors. The substrate terminal which not cnnected internally to the source terminal. The two transistors, an n-channel MOSFET and a p-channel MOSFET are connected in parallel with this, howevever, only the drain and source terminals of the two transistors are connected together. Their gate terminals are connected to each other via a NOT gate (inverter), to form the control terminal. As with the discrete transistors, the substrate terminal is connected to the source connection, so there is a transistor to the parallel diode, whereby the transistors passes backwards. However , since a transmission gate must block flow in either direction, the substrate terminals are connected to the respective supply voltage potential in order to ensure that the substrate diode is always operated in the reverse direction. The substrate terminal of the p-channel MOSFET is thus connected to the positive supply voltage potential and the substrate terminal of the n-channel MOSFET connected to the negative supply voltage potential.

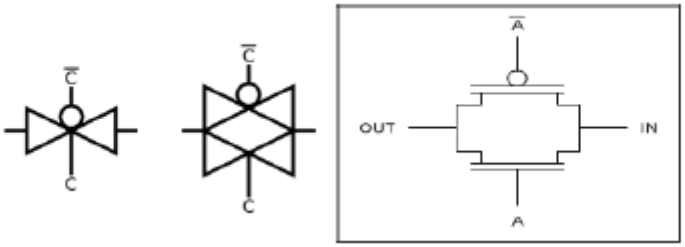


Figure 3: (A) Symbol of transmission gate (B) Schematic representation of transmission gate

In figure 3(A). When the control input is logic zero, the gate of the n-channel MOSFETs is also at a negative supply voltage potential. The gate terminal of the p-channel MOSFETs is caused by the inverter, to the positive supply voltage potential. Regardless of on which switcing terminal of the transmission gate (A or B) a voltage is applied, the gate source voltage of the n-channel MOSFETs is always negative, the p-channel MOSFETs is always positive. Accordingly, neither of the two transistors will conduct and the transmission gate will turns off. When the control input is a logic one, so the gate terminal of the n-channel MOSFETsis located at a positive supply voltage potential. By the inverter, the gate terminal of p-channel MOSFETs is now at a negative supply voltage potential. As the substrate terminal of the transistors is not connected to the source terminal, the drain and source terminals are almost equal and the transistors start a voltage difference between the gate terminal and one of these conducts.

IV. ARITHMETIC AND LOGICAL UNIT

In any system ALU is the most important part of a processor as it is required even for calculating the address of each memory location. It performs particular arithmetic and logic operations on each set of operands, based upon the instructions given by the processor. The system almost frequently, it contributes to one of the heighest power-density locations on the processor. Becouse of this reason, there exist thermal hotspots and sharp temparature gradients inside the execution core, thereby reducing the reliability as well as the battery life of the system therefore, there is a greate need for the development of a power optimized ALU design. This encourages powerfully for the design of a power optimized ALU that satisfies the superior needs along with the reduction of avarage powerconsuption. The rest of the paper is organized as follows. Discusses the fundamentals of ALU. Presents the methodology for developing a power optimized ALU. Includes the design and simulation details of ALU. Gives the results and analysis and concludes the paper. It consists of two separate units to carry out arithmetic and logic operations. The unit that is built specifically for performing arithmetic operations called as arithmetic unit and the unit handles the logic operations called the logic unit.

Working principle:

An ALU is combinational logic circuit, meaning that its outputs will change asynchronously in response to input changes. In normal operation , stable signals are applied to all of the ALU inputs and, when enough time(nothing but propagation delay) has passed for the signals to propagate through the ALU circuitry, the result of the ALU operation

appears at the ALU outputs. The external circuitry connected to the ALU is responsible for ensuring stability of ALUinput signals throughout the operation, and for following sufficient time for the signal to propagate through the ALU before sampling the ALU result.

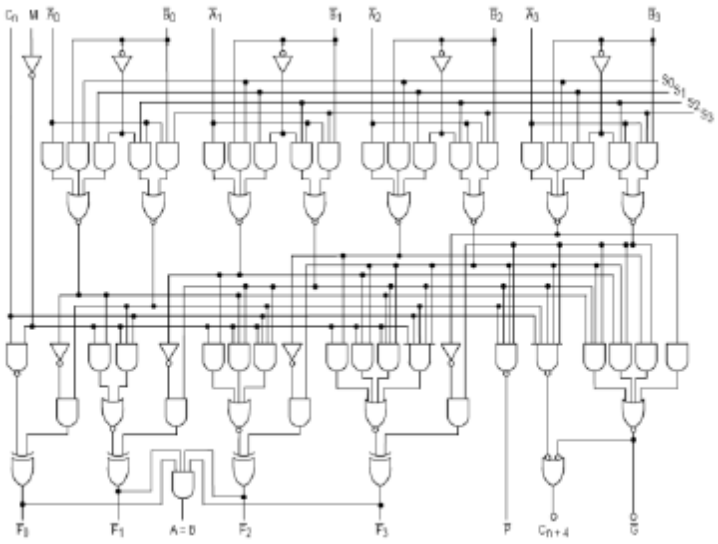


Figure 4. Block diagram of 4-bit ALU

ALU by applying signals to its inputs. Typically, the external circuitry employs to control the ALU operation which is paced by a sufficiently low frequency to ensure enough time for the ALU outputs to settle under worst case conditions. For example a cpu begins an ALU adition operation by routing operands from their sources (Which are usually registers) to the ALUs operand inputs, while the c simultaneously applies a value to the ALUs opcode input, configuring it to perform addition. At the same time the CPU also routes the ALU result output to the destination register that will receive the sum. The ALUs input signals which are held stable untill the next clock are allowed to propagate through the ALU and to the destination register while the CPU waits for the next clock. When the next clock arrives the destination register stroes the ALU result and since the ALU opertion has completed the ALU inputs may be setup for the next ALU operation. An ALU consists of three units :

1. **Arithmetic unit** : consist of addition,subtraction, addition with carry, subtracion with barrow, increament,decreament and Transfer.
2. **Logic unit** : consists of AND gate, OR gate, NOT gate and XOR gate.
3. **Shift unit** : consists of left shift,right shift.
4.

Table 2. 64 Bit Arithmetic and logic unit

S3	S2	S1	Cin	Result	Operation
0	0	0	0	A+B	Addition
0	0	1	0	A+$\bar{B}$+1	Subtraction
0	1	0	1	A−B+1	Addition with carry
0	1	1	1	A+$\bar{B}$	Subtraction With barrow
1	0	0	0	A+1	Increament
1	0	1	0	A−1	Decreament
1	1	0	0	A	Transfer
1	1	1	0	XX	No function

IV. SIMULATION RESULT

This paper presents a design and comparison of 64 Bit ALU using cmos and transmission gate logic and power differences is calculated. First we designed 1 bit alu and then we cascaded it, make it as 2 bit alu and then 4,8,64 bit ALUs. The below schematic diagrams shows the proposed ALUs.

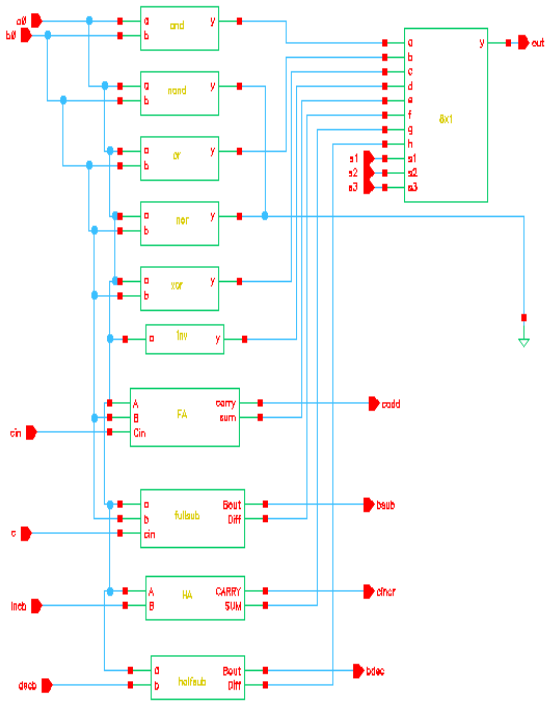


Figure 5. 1 Bit ALU Schematic diagram

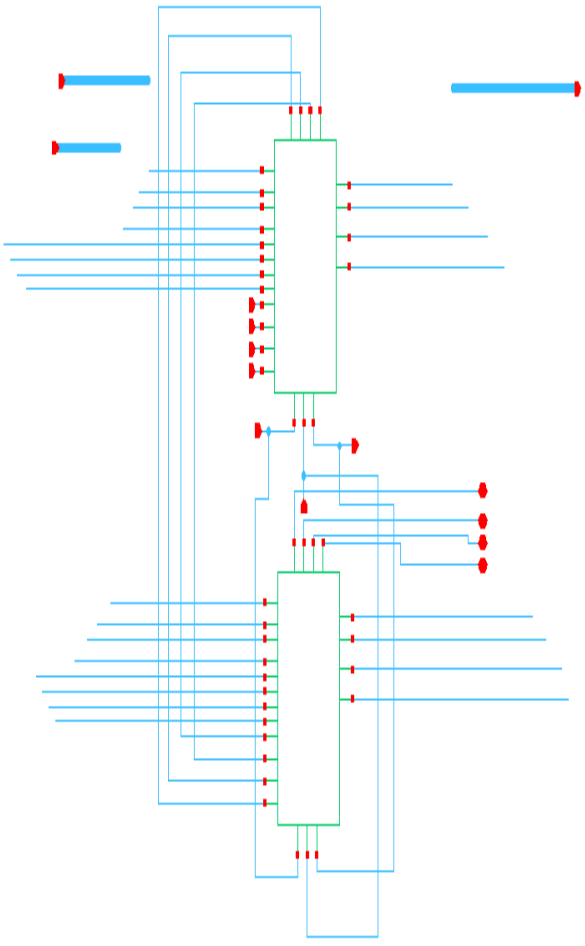
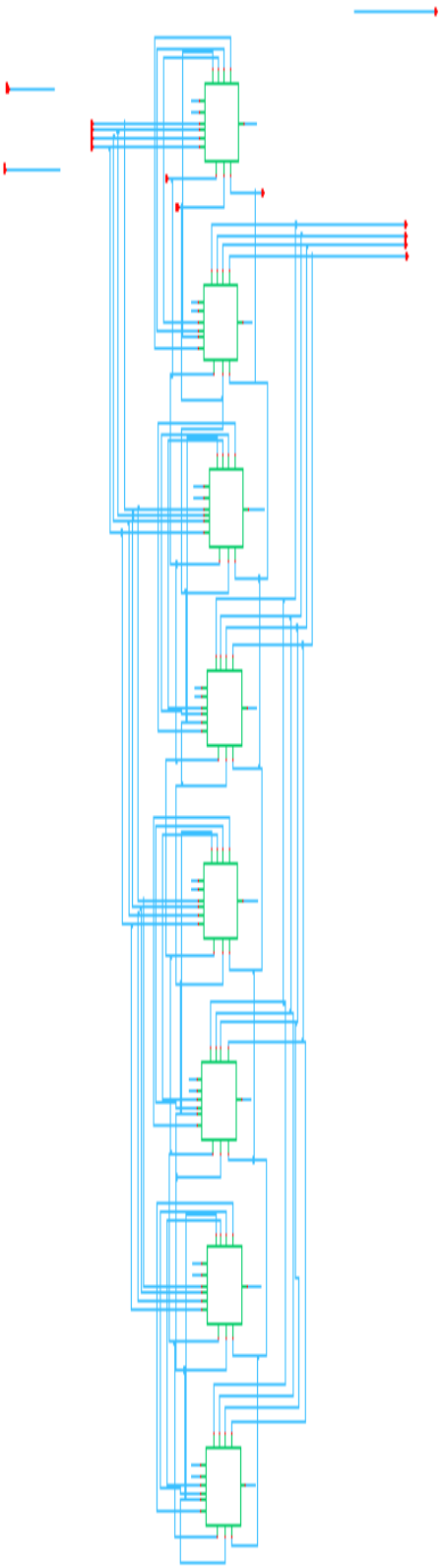


Figure 6. 8 Bit ALU Schematic diagram

4.1 Proposed design circits :



Fiigure 7. 64 Bit ALU in CMOS logic

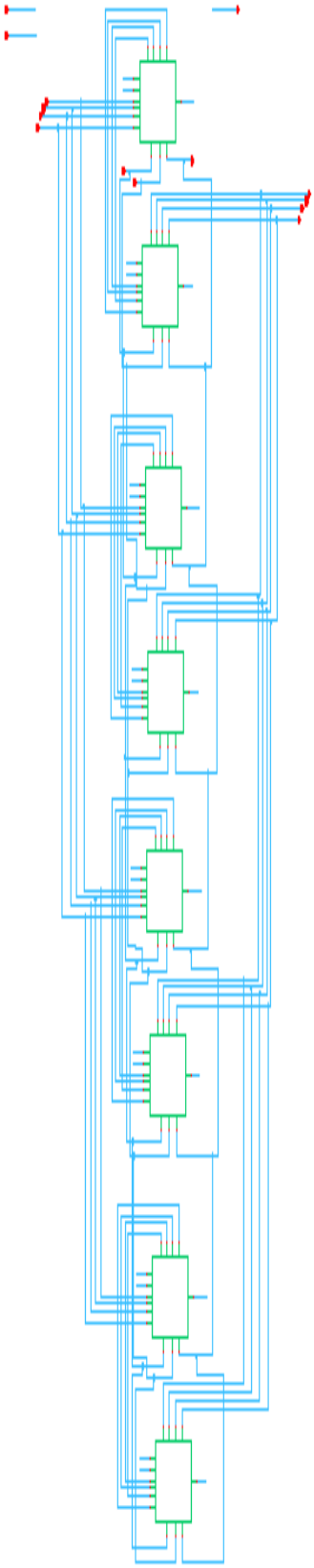


Figure 8 . 64 Bit ALU using transmission gate logic

4.2 Simulation Results :

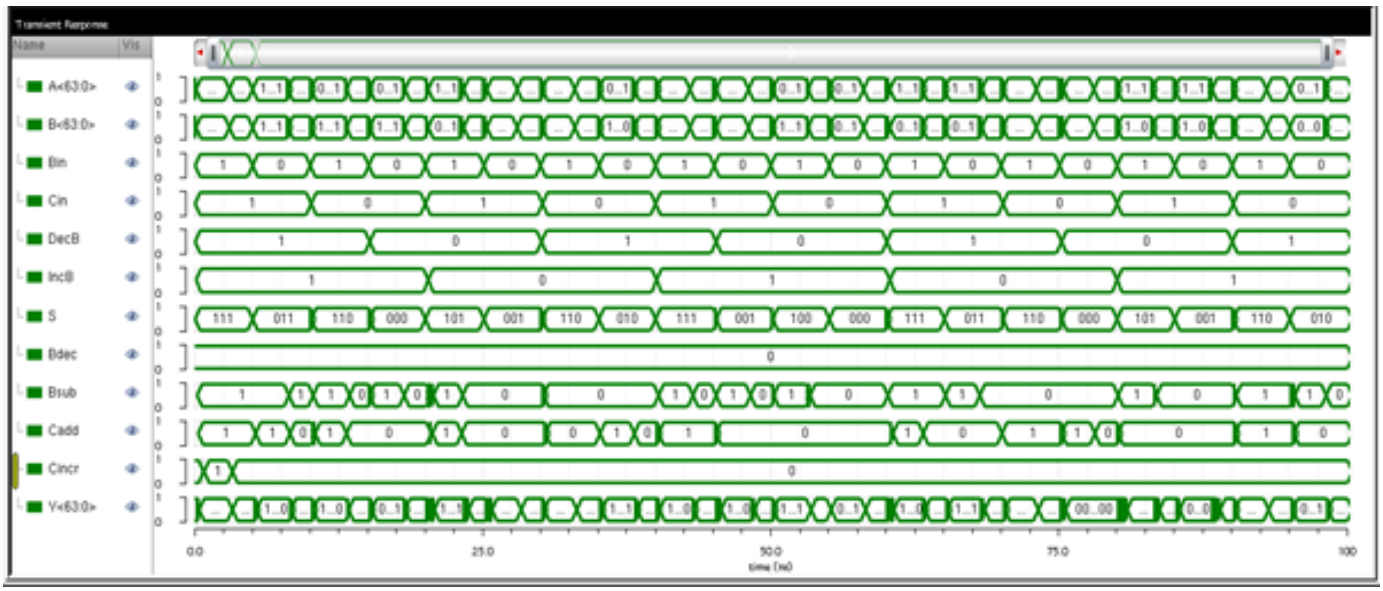


Figure 9. 64 Bit ALU using CMOS logic

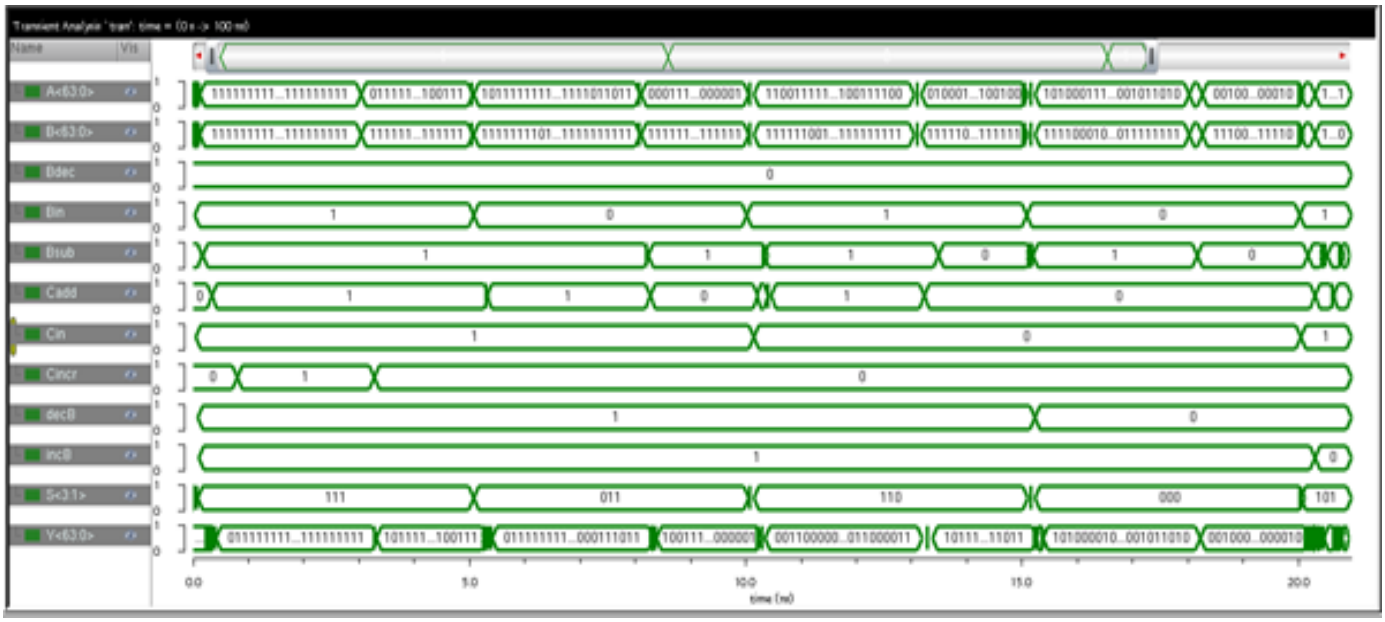


Figure 10. 64 Bit ALU using Transmission gate logic

4.3 Power calculations of different ALUs :

Table 3. Power Calculations

ALU	POWER(µW)	
	CMOS Logic	Transmission Gate Logic
1 Bit ALU	40.55E-6	40.35E-6
8 Bit ALU	173.6E-6	153.2E-6
64 Bit ALU	55.32E-6	26.11E-6

CONCLUSION

In this proect "Design and comparison of low power 64 Bit ALU using CMOS and Transmission gate logic" Arithmetic logic unit is the part of computer that perform all the arithmetic compution such as addition, subtraction, addition with carry,subtraction with barrow, increament, decreament and logic operations like AND, NOT, OR and XOR. ALU represents the fundamental building blocks of central processing unit of the computer. In this project 64 Bit Arithmetic and logic unit is designed using cmos and transmission gate logic which consumes less power and area, it is higly efficient for higher bit ALU and it enhance the system performance.

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