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High Speed and Low Power QPSK Modulator Design using Verilog and Cadence

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Abstract — *The Quadrature phase shift keying (QPSK) is one of the forms of phase shift keying (PSK) modulation scheme. The Convention QPSK method using Direct Digital Synthesizer (DDS) consumes more power. This proposed method eliminates the DDS and multiplier blocks of the modulator.*

Keywords- *QPSK modulation, VHDL, FGPA, DDS, Xilinx, Cadence,* NRZ

I. INTRODUCTION

The modulation is a process, used in communication system to transfer the data. This technique reduces the size of an Antenna and transfer the data without loss through the channel. Wireless communication system require high data rate for efficient transmission of information. . Many modulation techniques are used in digital communication system. The main modulation techniques are PSK, MSK, QAM, QPSK, etc. the digital methodology has advantages in terms of repeatability cost and simpler structure than analog solution. QPSK is one of the widely used communication technique. In QPSK modulation, the carrier phase acquires four discrete states that are used to represent a group of two input data bits as shown. Each group takes one form of QPSK states. Data transmission is QPSK is twice compared to BPSK. The bit error rate (BER) over (Signal-to-noise) SNR for both the modulation is same. The symbol period is QPSK is two times the bit period in QPSK. In the section2 general QPSK modulation method is discussed. Proposed methodology, completely eliminates DDS and multiplier blocks of the modulation system

II. CONVENTIONAL QPSK MODULATOR

The digital QPSK modulator is as shown in figure1. The input binary data sequence is divided in to two other sequences. These unipolar sequences are converted into bipolar by using NRZ encoding technique.

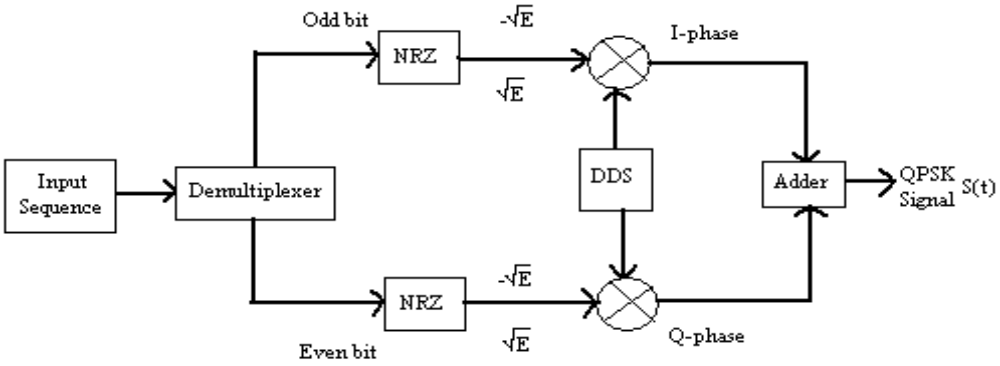


Figure 1. Conventional QPSK modulation.

The coded data will be mixed with carrier which is generated from DDS. The DDS produces the sine and cosine as separate carrier signal with same frequency. After multiplying the carrier with bipolar data. The coded data is nothing but the I-phase and even data as Q-phase. These two phases will be added together to produce a single QPSK signal. The QPSK produces a modulated wave is described as follows.

$$S(t) = m_I(t)\cos[2\pi fct] - m_Q(t)\sin[2\pi fct] \quad (1)$$

Where $m_I(t)$ is the in-phase component, $m_Q(t)$ is the quadrature-phase component of the modulated wave.

III. PROPOSED QPSK MODULATOR

In the proposed method data for each QPSK is collected and stored in different RAM blocks. Each RAM will store data for one QPSK phase. Since all the four possible phases for a QPSK is stored in four different RAM'S.

3.1. Block diagram and explanation

The digital QPSK modulator is stored in four different RAM'S the digital QPSK modulator is no longer required to produce a QPSK phase from I and Q phase as in first method QPSK modulator. For the simulation purposes a serial input sequence will be considered as input to the 1:2 demultiplexer. The 1:2 demultiplexer will separate the input sequence into odd and even bits. These odd and even bits will be the input for the 4:1 multiplexer. This will select one RAM for different combination of odd and even bits as shown in figure 2.

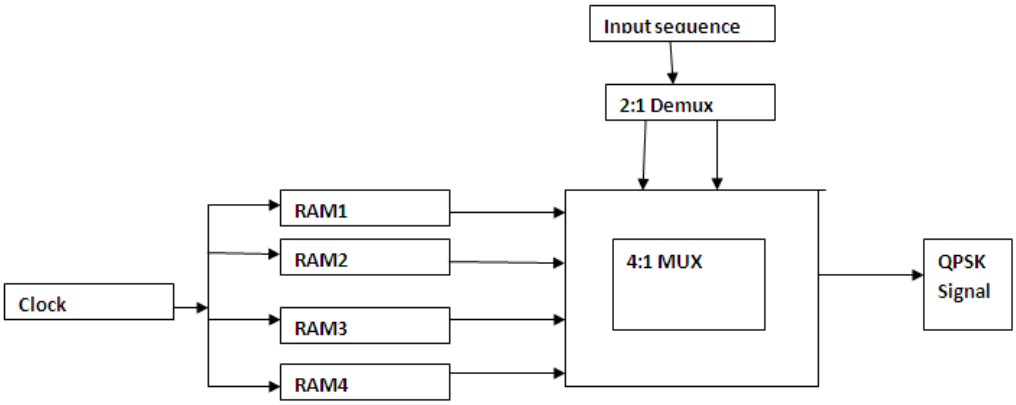


Figure 2. Block diagram of proposed QPSK modulation.

IV. SIMULATION RESULTS

The proposed design is modeled with VHDL and stimulated on Xilinx ISE 9.1i platform. The design is also executed using the cadence tool. The proposed design is compared in terms of area, throughput and power.

4.1. RTL for conventional QPSK modulator

The figure 3 shows the RTL obtained by synthesizing VHDL for conventional QPSK modulator.

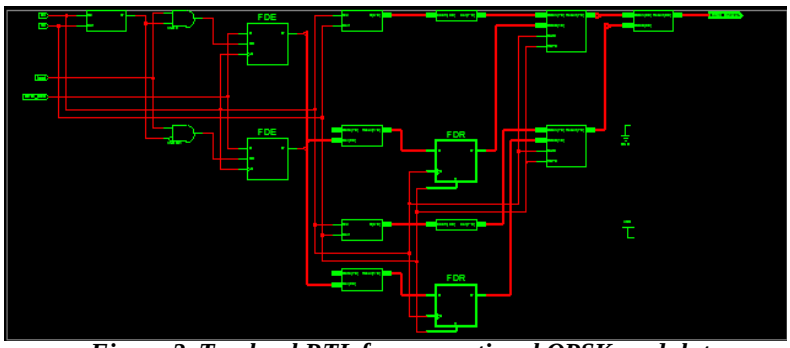


Figure 3. Top level RTL for conventional QPSK modulator.

4.2. Simulation results of conventional QPSK modulator

The figure 4 shows the simulator diagram. Where odd and even data change from 00 to 01 and 11 to 00

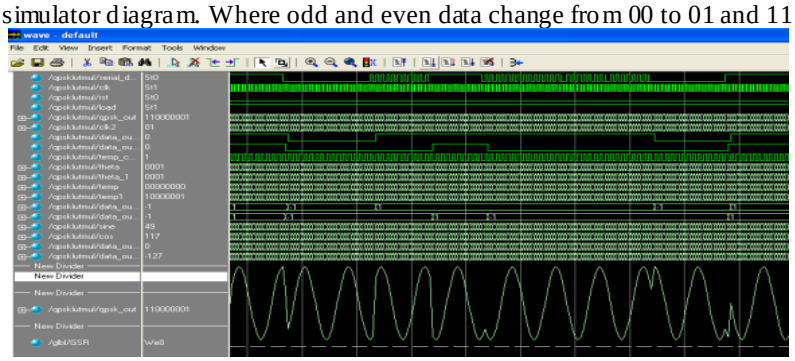


Figure 4. Simulation result of conventional QPSK modulator.

Then the data obtained is multiplied with carrier wave generator to produce me and Q phases and then added to both phases to generate QPSK signal.

4.3. RTL for proposed method

Figure 5. Shows the RTL schematic diagram and simulated results.

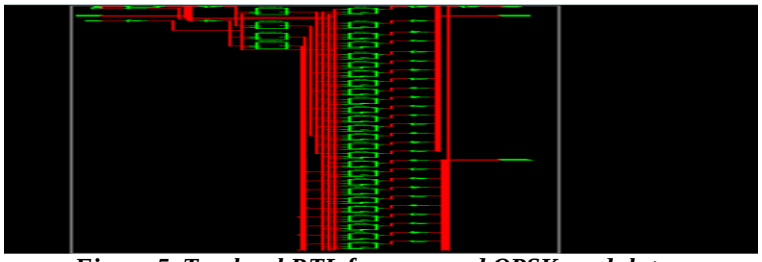


Figure 5. Top level RTL for proposed QPSK modulator.

4.4. Simulation results of the proposed QPSK modulator

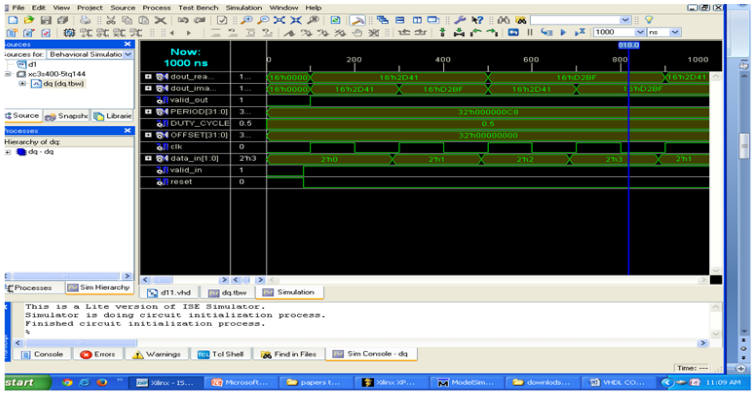


Figure 6. Simulation result of proposed QPSK modulator.

V. COMPARISION

The modulator was coded in VHDL and implemented on Spartan-3E FPGA kit and also executed using cadence incisive simulator. The parameter used by the entire implementation is described in table-1 and table-2. The performance and area constraints have been improved in method-2 compared to conventional QPSK modulator.

5.1. Results of XILINX ISE simulator

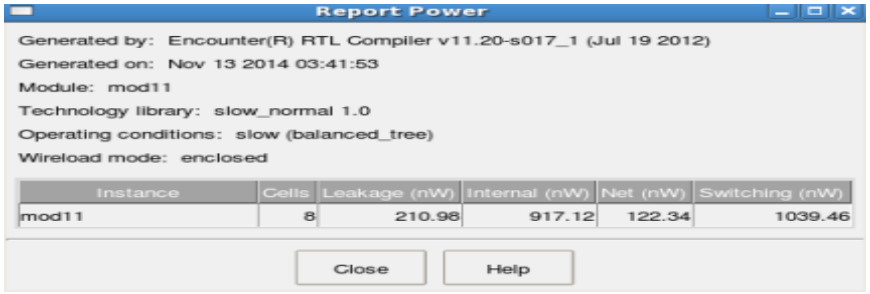
Table 1. Conventional QPSK modulator verses proposed modulator.

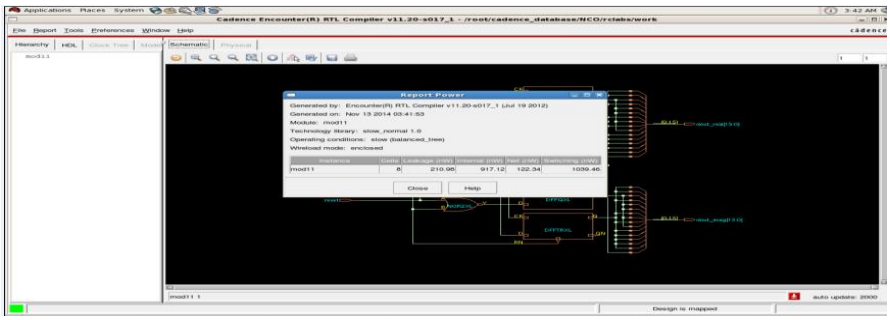
	Comparision		
		Conventional Method	***Proposed Method***
	Parameters	Total usage	Total usage
	No of slices	30	2
	No of slices	30	2
	No of 4 input LUTs	46	4
	No of slice flip-flops	28	25
Counters	4-bit up counter	2	2
Registers	Flip-flops	7	6
Cell usage:	LUT2	12	4
Clock buffers	BUFGP	1	1
IO Buffers	IBUF	3	2
	OBUF	9	4
Timing Summary	Speed grade	-5	-5
	Minimum period	5.272ms	2.571ms

5.2. Results of CADENCE INCISIVE simulator

rc:/> report power

Instance Cells	Leakage Power(nW)	Dynamic Power(nW)	Total Power(nW)
mod11 8	210.976	1039.462	1250.438

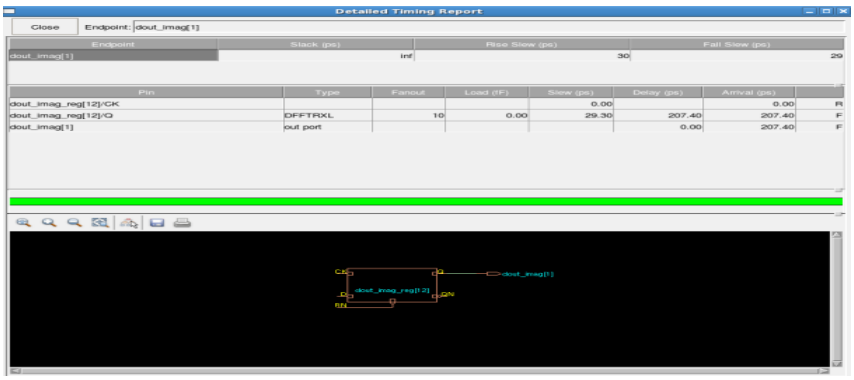




rc:/> report area

Instance Cells	Cell Area	Net Area	Total Area	Wireload
mod11 8	78	0	78	<none>(D)

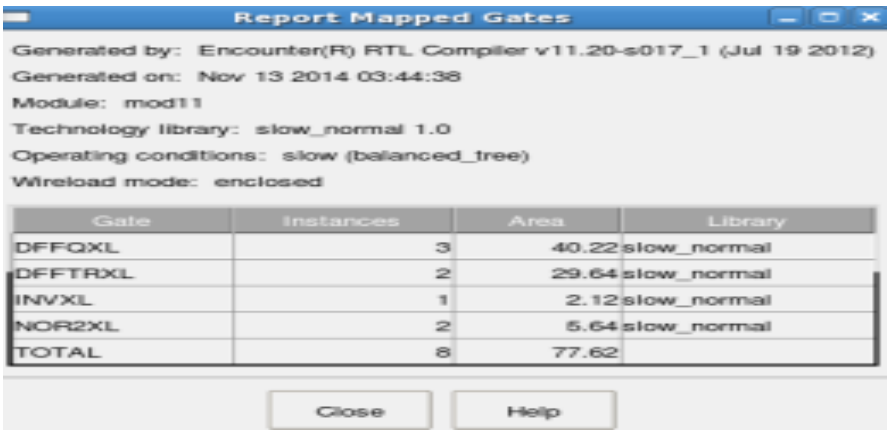
rc:/> report timing



Pin	Type	Fanout	Load (fF)	Slew (ps)	Delay (ps)	Arrival (ps)	
dout_imag_reg[12]/CK				0		0	R
dout_imag_reg[12]/Q	DFFTRXL	10	0.0	29	+207	207	F
dout_imag[1]	out port				+0	207	F

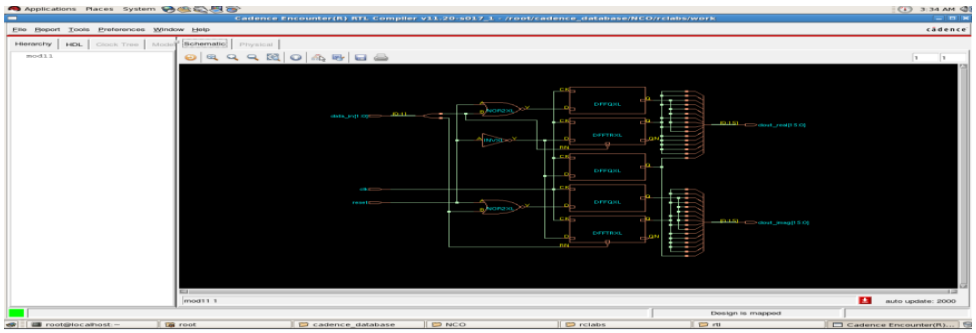
Timing slack : UNCONSTRAINED
Start-point : dout_imag_reg[12]/CK
End-point : dout_imag[1]

rc:/> report gates



Gate	Instances	Area	Library
DFFQXL	3	40.219	slow_normal
DFFTRXL	2	29.635	slow_normal
INVXL	1	2.117	slow_normal
NOR2XL	2	5.645	slow_normal
total	8	77.616	

Type	Instances	Area	Area %
sequential	5	69.854	90.0
inverter	1	2.117	2.7
logic	2	5.645	7.3
total	8	77.616	100.0



VI. CONCLUSION

The conventional QPSK modulator design uses multipliers, adders, subtractors, counters, flip-flops and DDS. In the proposed QPSK modulator these components are eliminated, hence high speed and low power are achieved. The work is simulated and synthesized using cadence incisive simulator.

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