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Design of low Power High Performance 32Bit ALU Using Different Adders in 45nm Technology

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Abstract — *A design for 1-bit full Adder cell using hybrid-CMOS logic style is proposed in this work. The Full Adder is based on a novel XOR-XNOR circuit that generates full-swing outputs simultaneously and outperforms its best counterpart which is showing improvement in power consumption, power delay product (PDP). The proposed full adder provides good driving capability and is a proper choice for low-voltage applications. The proposed work is to be done using cadence tools in 45nm technology with a power supply 1V to evaluate the performance of the circuit. It further describe simulation simulation results of that compare the surveyed full-adder cells. The work simulate all combinations of input transitions and consequently determine the delay and power consumption for the various full-adder cells. Moreover, the simulation results highlight the weaknesses and the strengths of the various full-adder cell designs. Adders are the basic building blocks of any processor or data path application. In adder design carry generation is the critical path. To reduce the power consumption of data path we need to reduce number of transistors of the adder. Hence different types of adder circuits are designed and which are used in ALU's. The circuits are Proposed full adder, 14T full adder, and normal Full Adder.*

Keywords- *Full Adder, high performance, high speed, hybrid-CMOS, low-power; low voltage, VLSI*

I. INTRODUCTION

Most of the VLSI applications, such as digital signal processing, image processing, and digital filter sign, widely use arithmetic operations. Addition, subtraction and multiplication are examples of the most commonly used operations. The 1-bit full adder cell is the building block of these units. Hence, improving its performance is critical for improving the overall unit performance. The most important performance parameters for a generic VLSI system are power consumption, speed, and chip area. Several logic styles have been used in the past to design full adder cells. Each logic style has its own advantages and disadvantages. Classical designs of full adders normally used only one logic style for the whole full adder design. Standard static CMOS, members of pass-transistor logic (PTL) family such as CPL, DPL, SRPL, and transmission gate are the most important logic styles in the conventional full adders. In the other full adder designs, more than one logic style have been used. These designs are called hybrid-CMOS logic style. These designs use the features of different logic styles to improve upon the performance of the designs using single logic style. New-Hybrid -CMOS adder, New-14T adder, and full adders proposed are the examples of adders designed with this logic style. In this paper, a novel 1 -bit full adder has been proposed with better performance in terms of power consumption, propagation delay and power-delay product (PDP) in comparison with these existing full adders. . The rest of this paper is organized as follow in power consumption issues in CMOS VLSI circuits will be discussed. In this content, the main structure of 1-bit full adder will be introduced. Then in this section , the new XOR-XNOR circuit and novel 1-bit full adder cell will be proposed. In simulation environment will be described simulation results will be expressed which show the supremacy of the proposed full adder. Based on these proposed full adder,14 t full adder, normal full adders are substituted in ALU as a application purpose.

As we know the major concern in VLSI is about area, speed and power. But actually there is no much importance given to the power when compared to the the speed and area in VLSI circuits. But as per the current growing technology, power has become placing a major role to reduce the power consumption of the electronic circuits. In these applications, average power consumption is a critical design concern. In the absence of low-power design techniques then, current and future portable devices will suffer from either very short battery life or very heavy battery pack. To reduces this power consumption and for good battery life we are proposing a Hybrid-CMOS logic design of the Full adder.

II. PROPOSED CIRCUITS

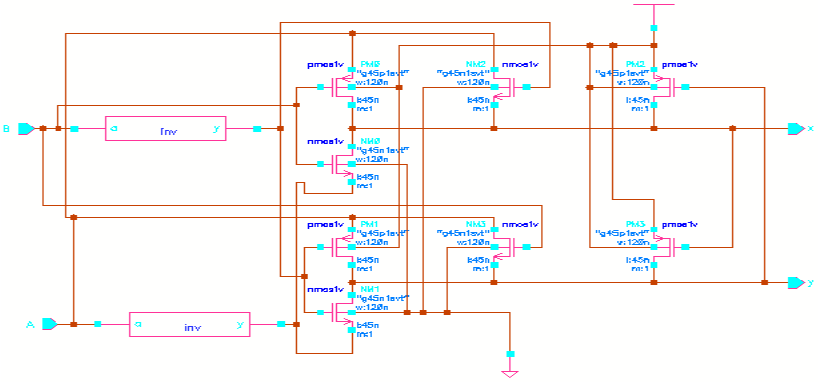


Fig 1 : Schematic diagram of proposed XOR-XNOR circuit

The proposed XOR-XNOR circuit is based on pass transistor logic with output signals restoration. This circuit is compared to circuits used in different applications. The simulation results in Hybrid CMOS technology at input 1V power supply. Simulation results show that the proposed circuit has less power consumption and propagation delay than other existing circuits. Owing to the less power and delay in proposed circuit, there is almost 43%-71% improvement in PDP. Since the proposed circuit has the lowest PDP compared to its counterparts, it can be used for implementation of the proposed full adder. Moreover, with the explosive growth, the demand, and the popularity of portable electronic products, the designers are driven to strive for smaller silicon area, higher speed, longer battery life, and enhanced reliability. The XOR-XNOR circuits are basic building blocks in various circuits especially arithmetic circuits (adders & multipliers), compressors, comparators, parity checkers, code converters, error-detecting or error-correcting codes and phase detector.

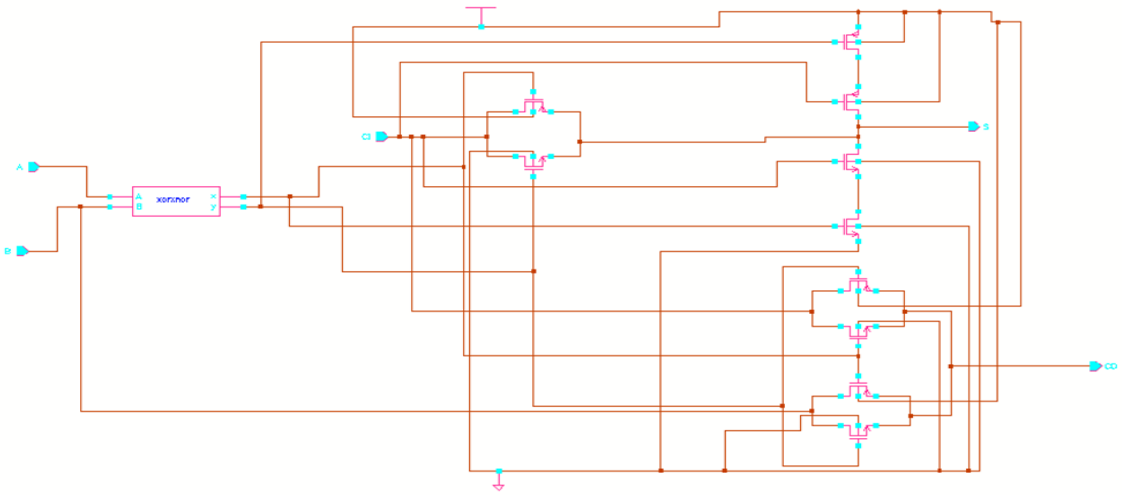


Fig 2 : Schematic diagram of Proposed Full adder

More than one logic style is used for implementation of the hybrid full adders. The hybrid adder cells may be classified into various categories depending upon their structure and logical expression of the Sum and Carry output signals. All hybrid designs use the best available modules implemented using different logic styles or enhance the available modules in an attempt to build a low power consuming full-adder cell. Most full adder topologies are based on two XOR circuits: one to generate (XOR) with (XNOR), and the other to generate the Sum output. The carry signal is obtained by using one MUX (multiplexer).The hybrid logic style uses completely different logic designs so as to make new full adders which gives good desired performance. The design utilizes several types of CMOS logic styles to generate a design of higher efficiency shown in Figure.

III. METHODOLOGY

Main Structure of 1-bit Full Adder

Generally, hybrid-CMOS full adders are categorized in three groups depending on their structure and logical expression of *sum* output. The first category of full adders is based on XOR gates (XOR-XOR based full adder) and second one is based on XNOR gates (XNOR-XNOR based full adder). In third category, the *Sum* and *Carry* outputs are generated by XOR-XNOR intermediate signal (centralized full adder). In this paper, the proposed full adder stands on third category. The *Sum* and *Carry* (C_{out}) outputs of a 1 -bit full adder generated from the binary inputs *A*, *B*, and C_{in} can be generally expressed as

$$SUM = A \oplus B \oplus C_{in}$$

$$C_{out} = A.B + C_{in} \quad (A \oplus B)$$

Generally, this category is divided by three modules. ModuleI1 is an XOR-XNOR circuit producing *X* and *y* signals respectively. These Modules are 2-to-1 multiplexers with *X* and *Y* as select lines. The simultaneous generation of *x* and *Y* signals is critical in these types of adders, because they drive the select lines of the multiplexers in the output stage. Otherwise, there may be glitches and unnecessary power dissipation may occur.

Table 1 : Truth table of 1 bit full adder

Input			Output	
A	B	Cin	Sum	Carry
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

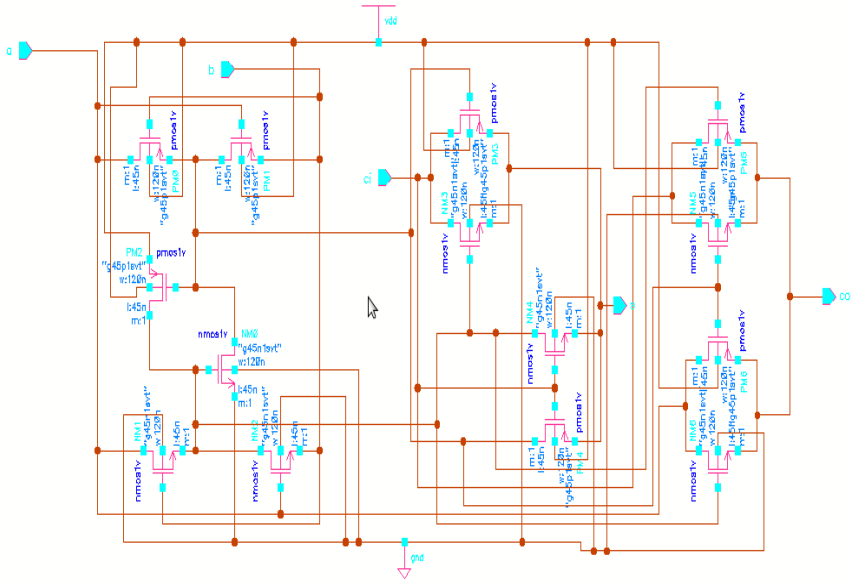


Fig 3 : Schematic diagram of 14T Full adder

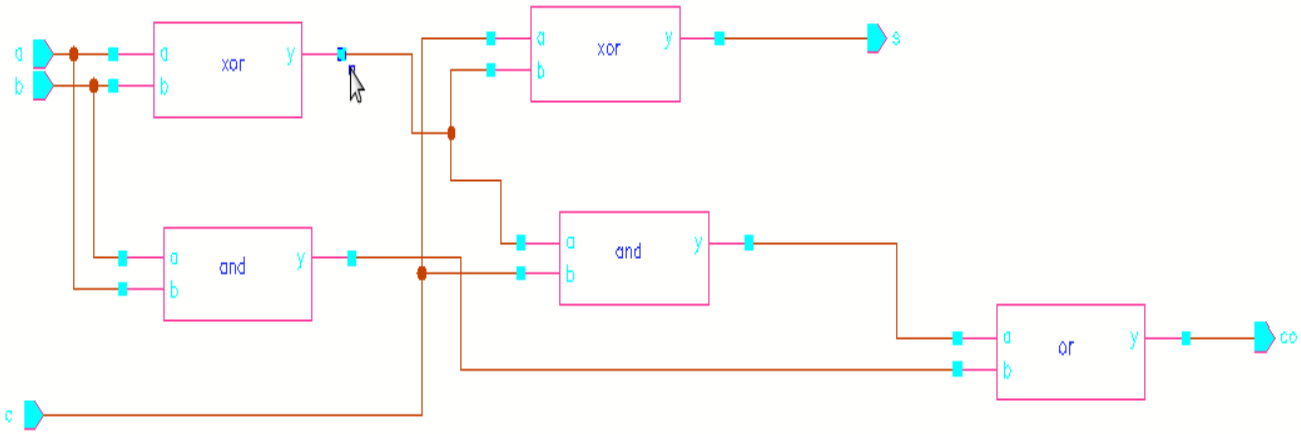


Fig 4 : Schematic diagram of Normal Full Adder

Arithmetic logic unit(ALU)

Most of the VLSI applications, such as digital signal processing, image processing, and digital filter design, widely use arithmetic operations. Addition, subtraction and multiplication are examples of the most commonly used operations. The

1-bit full adder cell is the building block of these units. Hence, improving its performance is critical for improving the overall unit performance. The most important performance parameters for a generic VLSI system are power consumption, speed, and chip area. Several logic styles have been used in the past to design full adder cells. E ach logic style has its own advantages and disadvantages. Classical designs of full adders normally used only one logic style for the whole full adder design. Based on these full adder circuit designs ,we have to implement a ALU. Different types of Full adder circuits are used in ALU's as a application. The ALU performs as addition, subtraction, division and multiplication and logical operations are shift left shift right, or, not and etc. Different types of full adders are used to calculate power delay in low power VLSI applications.

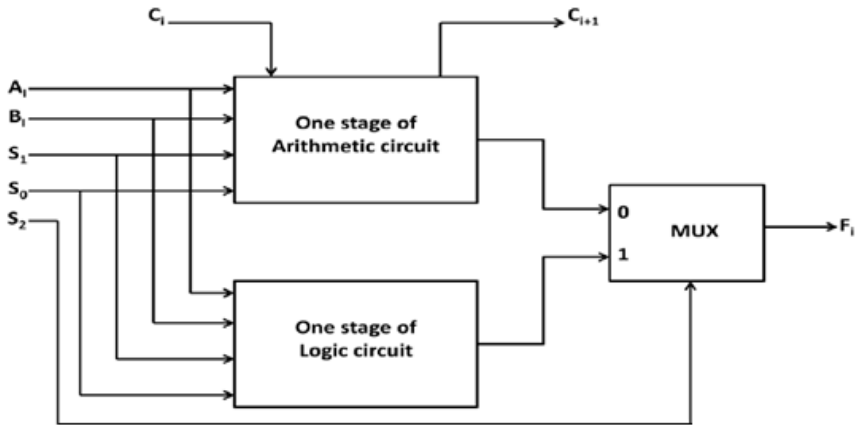


Fig 5 : Implementation of ALU

In this work 32 Bit ALU is implemented as a application purpose of Full adder of different logic styles. In this content for arithmetic operations as addition, subtraction. For logical operations AND,OR,NOR,XOR,XNOR etc operations are performed. All these functions are implemented as 32 Bit. As shown in above figure the architecture consist of multiplexer is also implemented. Hence a 32 Bit multiplexer is designed and it depends on the selection lines. The application of full adder purpose delay, power calculated.

The below figures shows 32 bit ALU using proposed Full ader a<31:0>,b<31:0>,c are inputs and y<31:0>,co<31;0>,b<31:0> is output and s1,s2,s3 are selection lines.

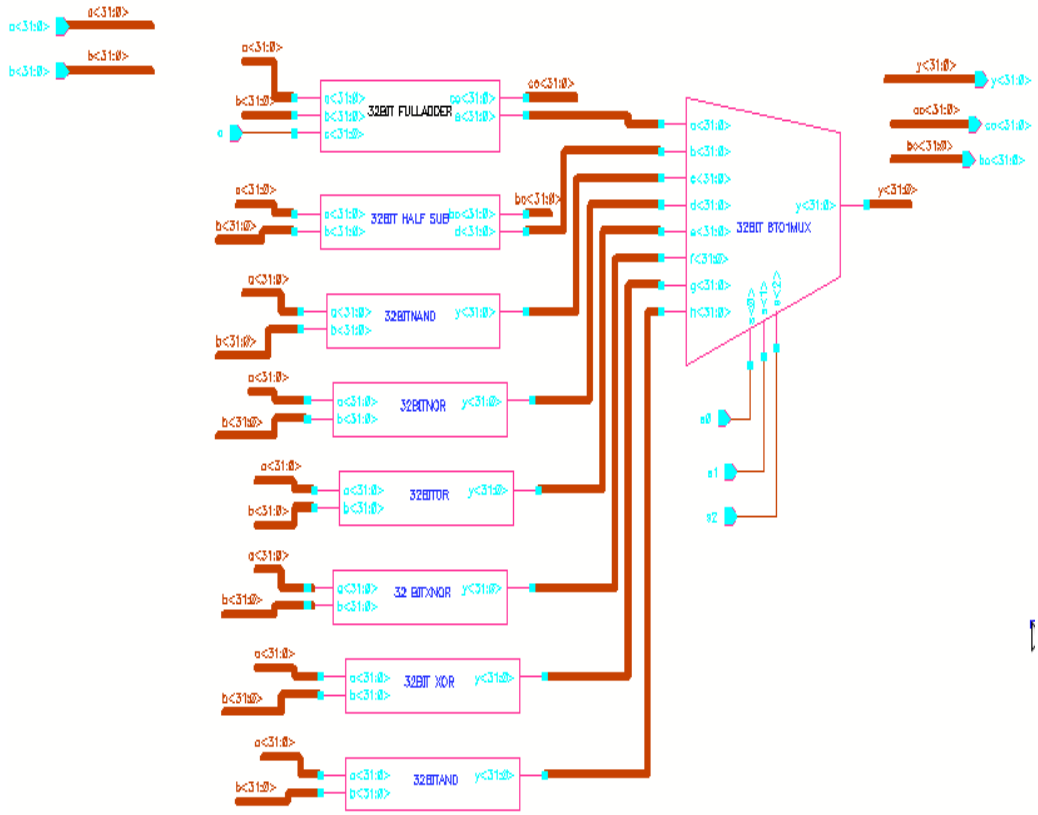


Fig 6 : Schematic diagram of 32 bit ALU using proposed Full adder

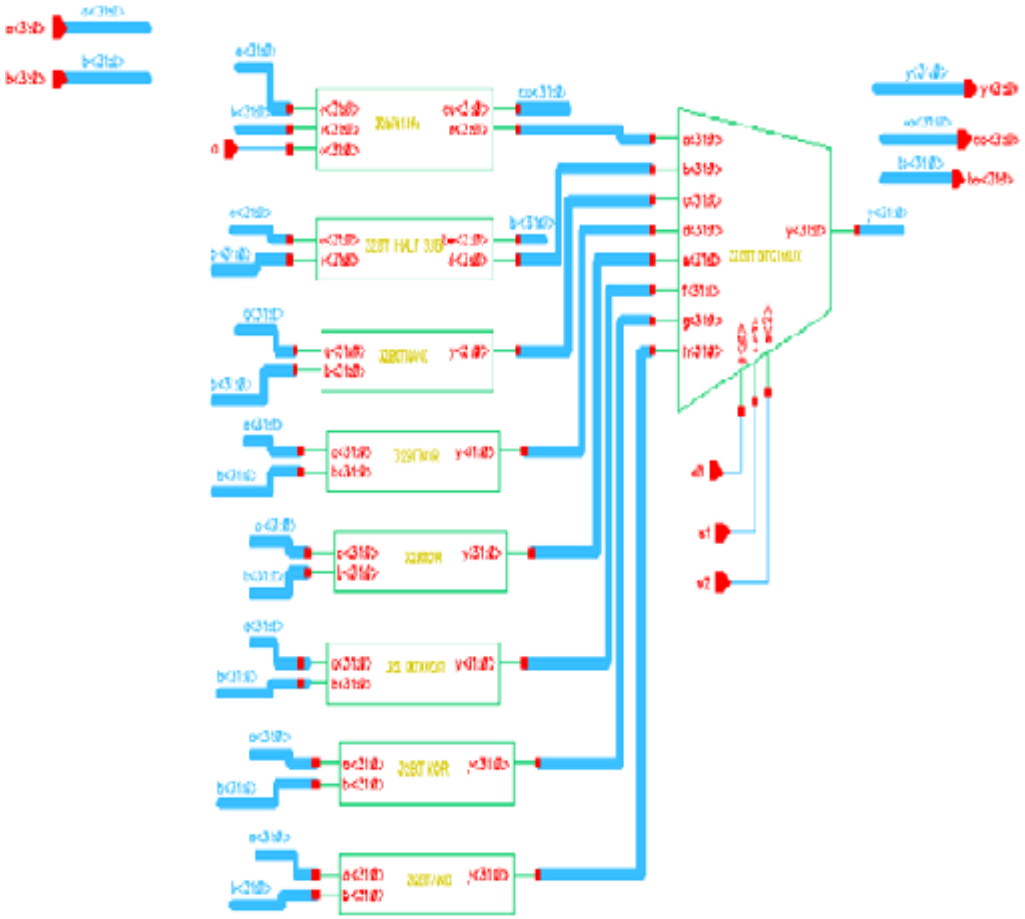


Fig 7 : Schematic diagram of 32 bit ALU using 14T Full Adder

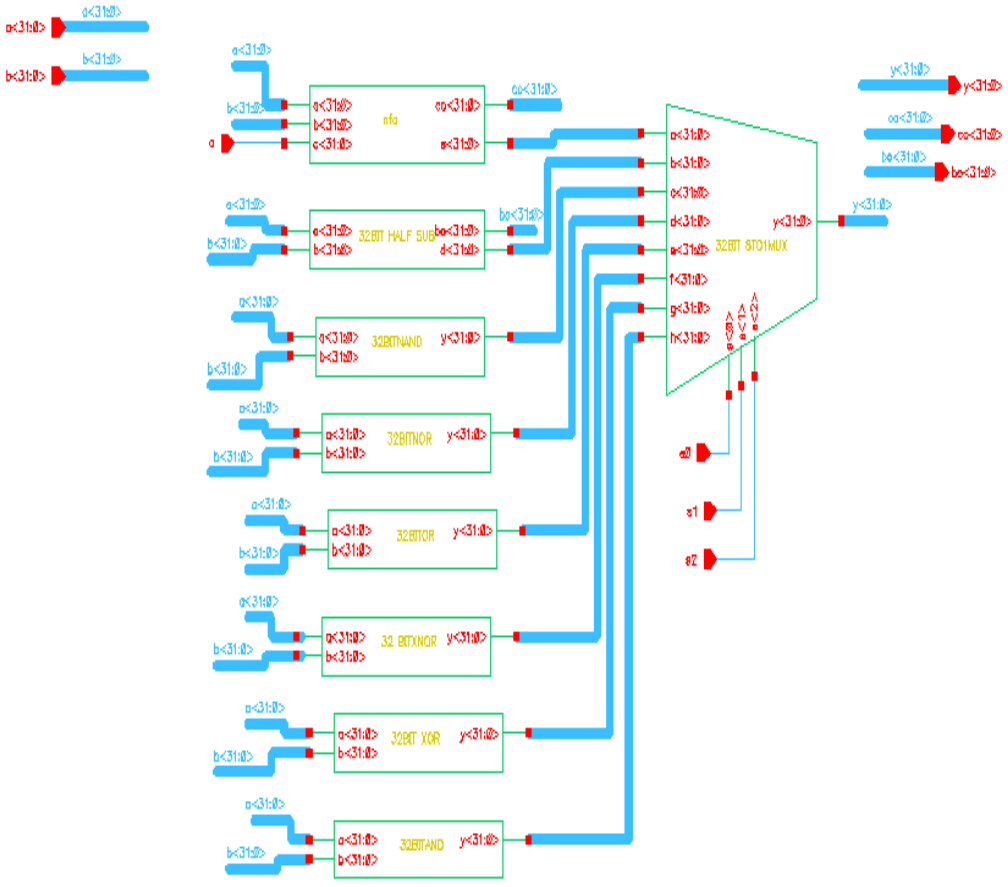


Fig 8 : Schematic diagram of ALU using general Full Adder

IV. SIMULATION RESULTS

Proposed XOR-XNOR Circuit

The below figure shows schematic diagram of proposed XOR-XNOR circuit and a,b are inputs and x,y are outputs.

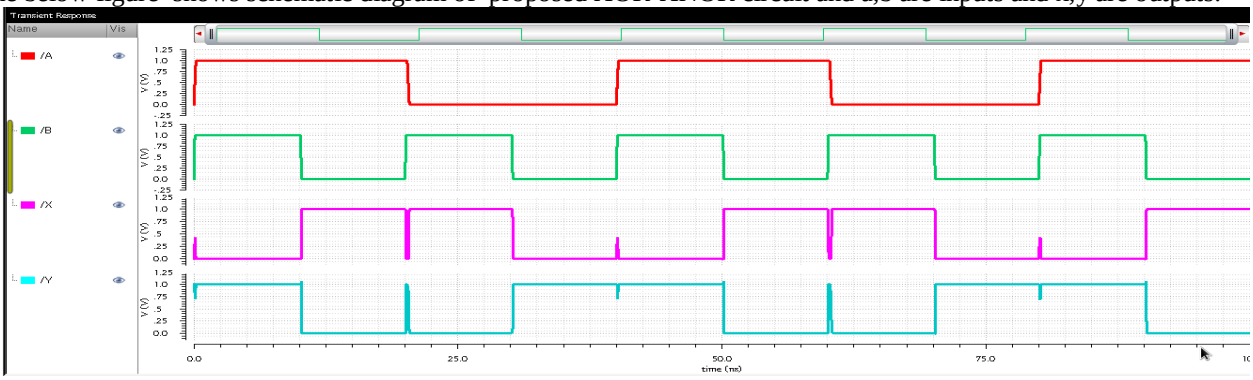


Fig 9 : Simulation results of Proposed XOR-XNOR gate

Proposed Full adder

The below figure shows schematic diagram of proposed full adder circuit and a,b,c are inputs and s,co are outputs.

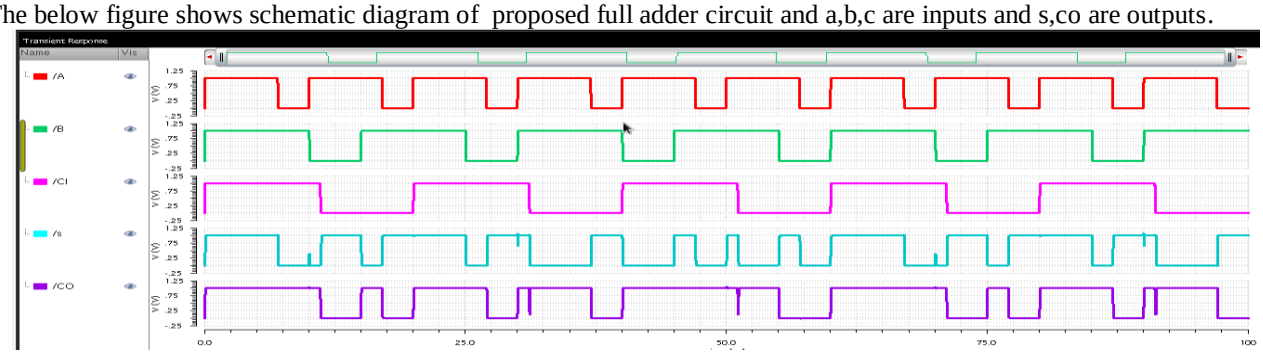
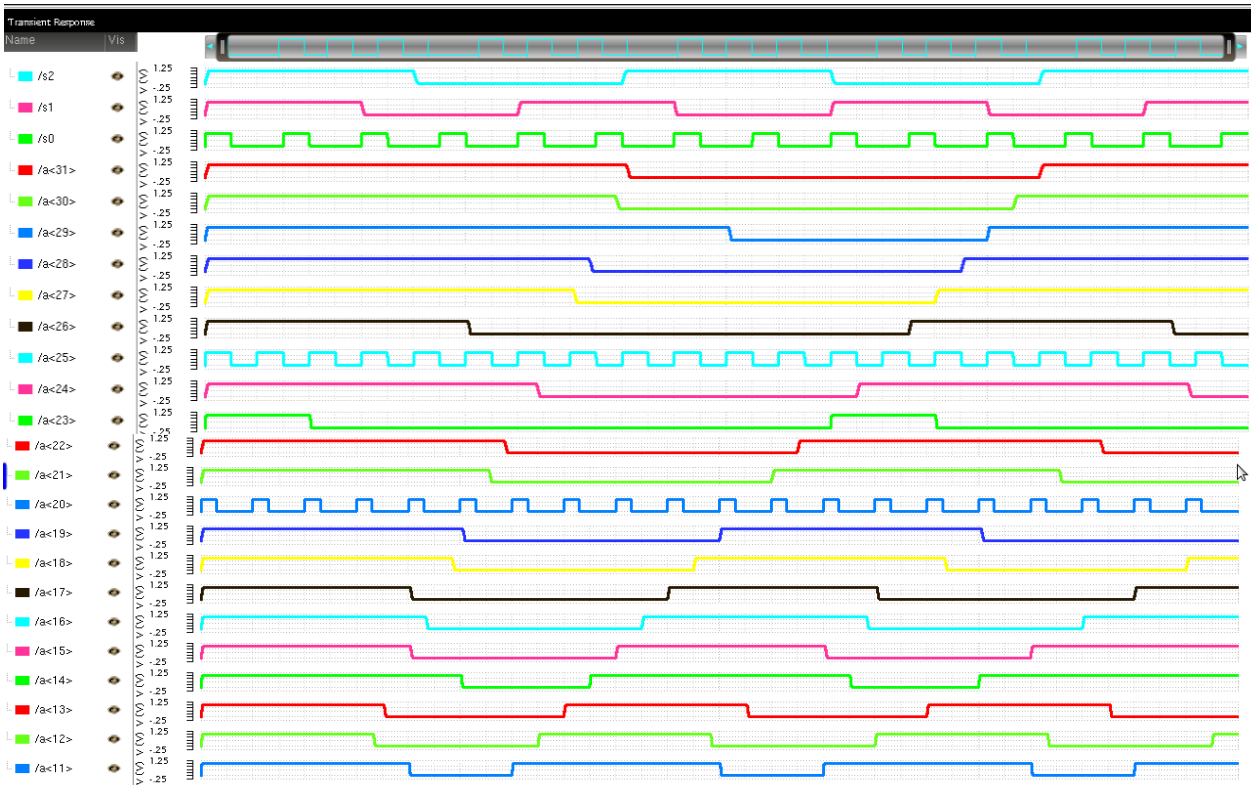
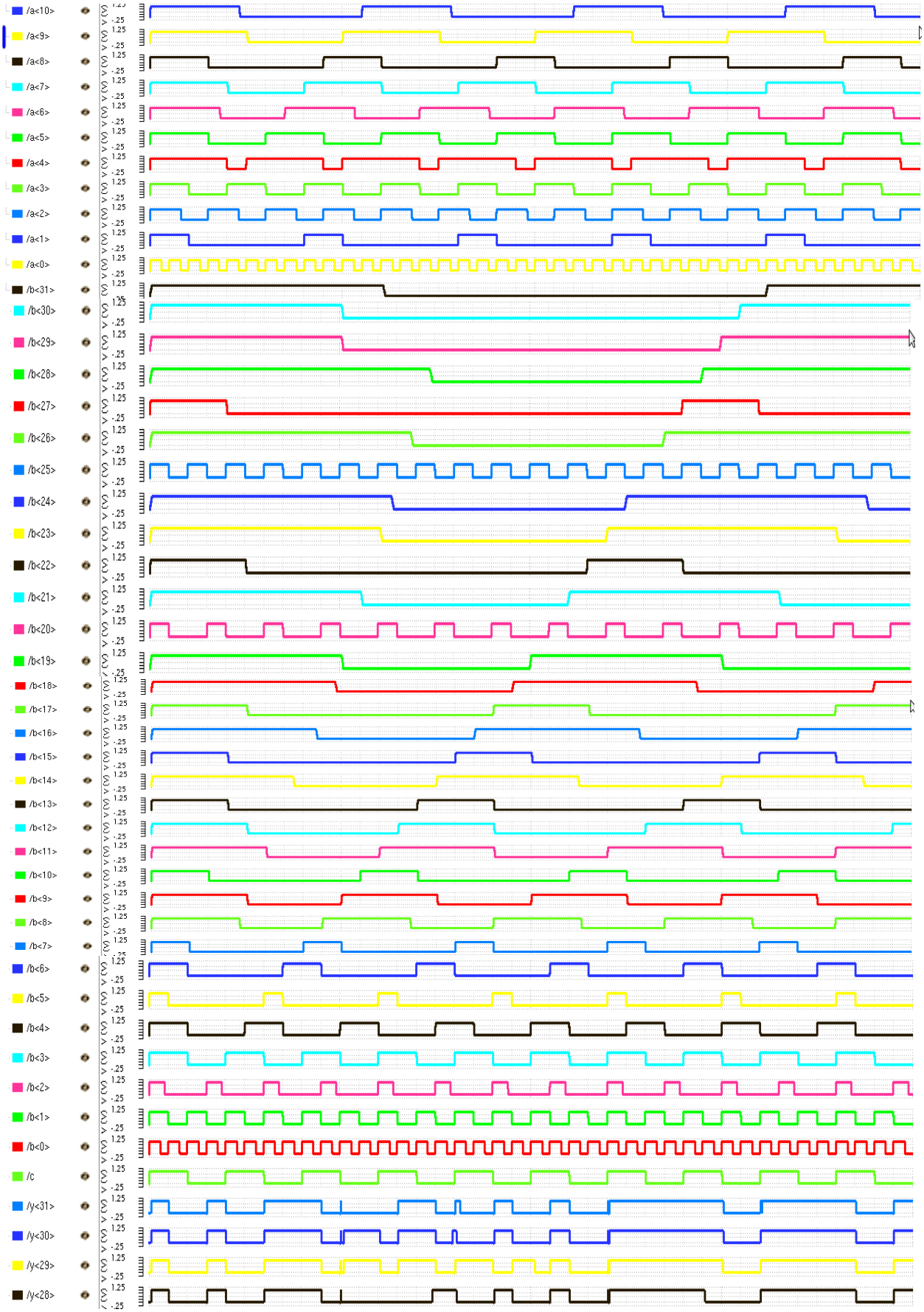


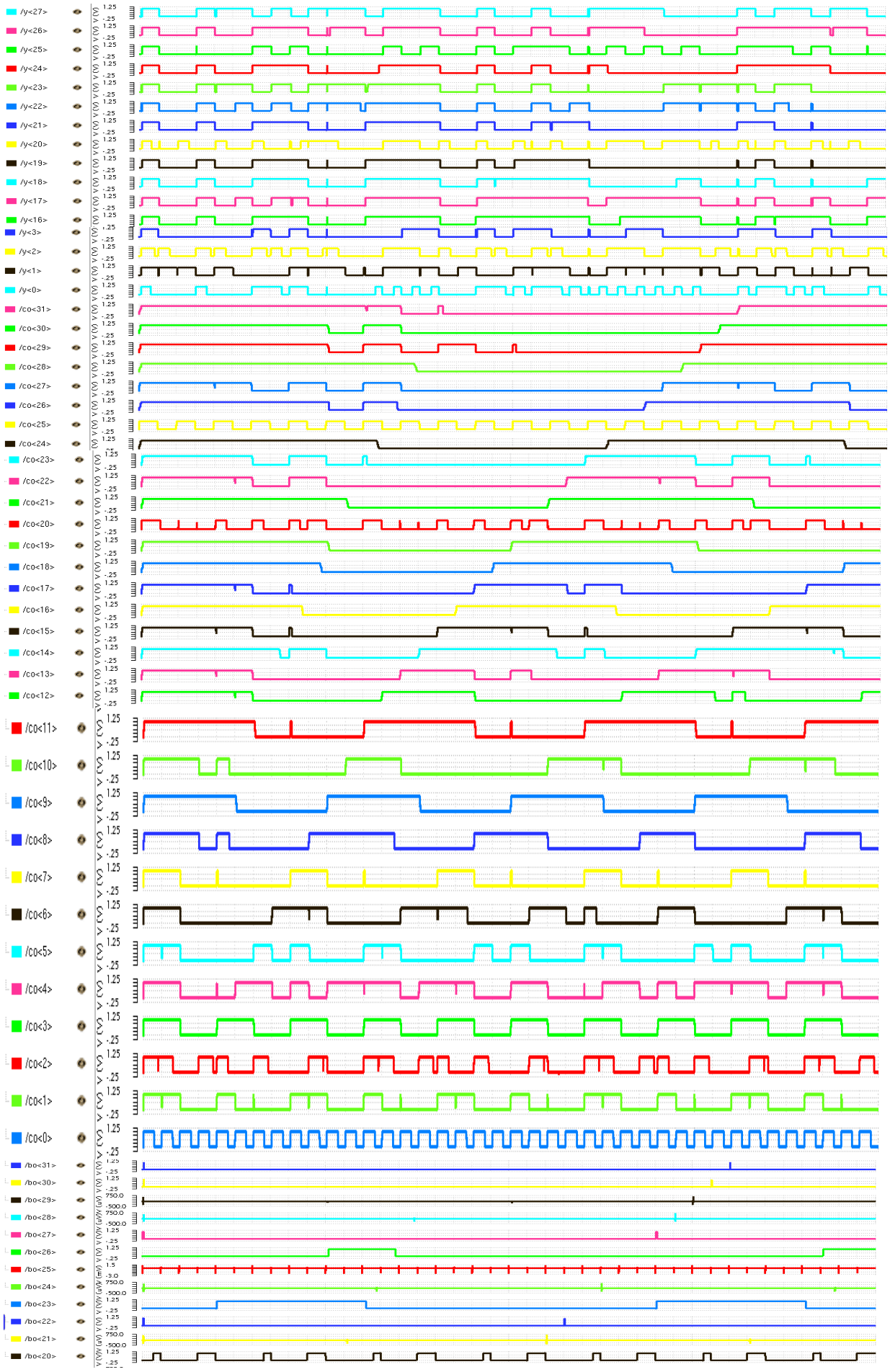
Fig 10 : Simulation results of Proposed Full Adder circuit

Simulation Results of ALU

The below figure 6.13 shows 32 bit ALU using Proposed Full ader a<31:0>,b<31:0>,c are inputs andy<31:0>, co<31;0>,b<31:0> is outputs and s1,s2,s3 are selection lines.







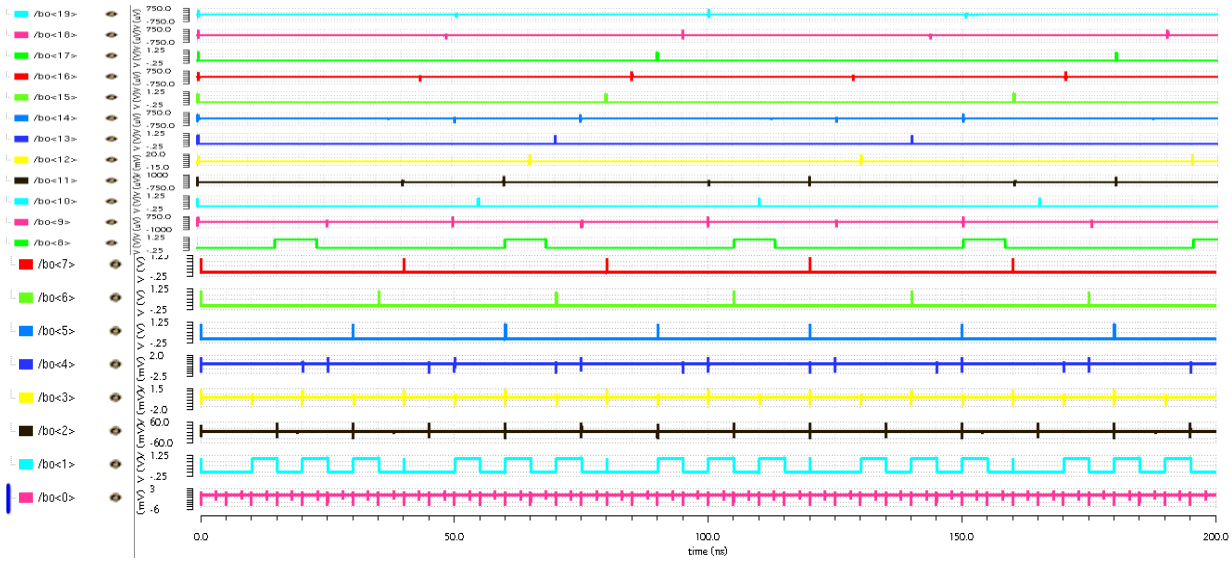


Table 2 : Comparison of power and delay of different designs in 45nm technology

Full Adder	Power(W)	Delay	Power delay Product(PDP)
Proposed Full adder	311.31ns	26.57ps	8.271E-19
14T Full adder	43.56µs	31.75ns	1.383E-12
Normal Full adder	85.59µs	59.12ns	5.060E-12

V. CONCLUSION

Various types of full adders with different logic styles have been implemented. These-CMOS Hybrid CMOS, 14T full adders are compared with new hybrid full adder and adder. These full adders consists of less number of transistors, because of less number of transistors results in less switching activity and area. A broad comparison of all the designs will shows the gradual improvement in power dissipation, delay and Power delay product (PDP). The considered reduction in power by minimizing static and dynamic power dissipation as well as some techniques to enhance the speed of the design leads to the best PDP. The proposed hybrid-CMOS full adder has better performance than most of the conventional full-adder cells owing to the novels design modules proposed in this paper. It performs well with supply voltage scaling and under different load conditions. We recommend the use of hybrid-CMOS design style for the design of high performance circuits. It has the best driving capability compared to existing full adder circuits. Based on these full adders as application purpose used in ALU and power, delay Values are calculated, and different digital applications are implanted by using this type of full adders.

REFERENCES

[1] R.Zimmermann and W.Fichtner, "Low-power logic styles: CMOS versus pass- transistor logic," Solid-State Circuits, IEEE Journal of, vol. 32, pp. 1079-1090, 1997.

[2] J. Zavarei, M.R.Baghbanmanesh, E.Kargaran ,H.Nabovati,and A.Golmakani,"Design of new full adder cell using hybrid-CMOS logic style," in Electronics, Circuits and System (ICECS), 2011 18th IEEE International Conference on, 2011, pp. 451-454.

[3] M. Zhang, J. Gu, and C.-H. Chang, "A novel hybrid pass logic with static CMOS output drive full-adder cell," in Circuits and Systems, 2003. ISCAS'03. Proceedings of the 2003 International Symposium on,2003, pp. V-317-V-320 vol.5.

[4] C.-H. Chang, J.Gu, and M. Zhang, "A review of 0.18-/spl mu/m full adder performances for tree structured arithmetic circuits," Very Large Scale Integration (VLSI) Systems, IEEE transactions on, vol. 13, pp. 686-695, 2005.

[5] S. Goel, A.Kumar, and M.Bayoumi,"Design of robust, energy-efficient full adders for deep-sub micrometer design using hybrid-CMOS logic style," Very Large Scale Integration (VLSI) Systems, IEEE Transactions on, vol.14,pp.1309-1321, 2006.

[6] D.R adhakrishnan, "Low-voltage low-power CMOS full adder," in Circuits, Devices and Systems, IEE Proceedings-, 2001, pp. 19-24.

[7] M. Agarwal, N. Agrawal, and M. A.Alam, "A new design of low power high speed hybrid CMOS full adder," in Signal Processing and Integrated Networks (SPIN), 2014 International Conference on, 2014,pp 448-552.

[8] S.Musala and B. R. Reddy, "Implementation of a full adder circuit with new full swing EX-OR/EX-NOR gate," in Microelectronics and Electronics (PrimeAsia), 2013 IEEE Asia Pacific Conference on Postgraduate Research in, 2013, pp. 29-33.

[9] A. M. Shams and M. Bayoumi, "A novel high-performance CMOS 1-bit full-adder cell, "Circuits and Systems II:Analog and Digital Signal Processing, IEEE Transactions on,vol. 47,pp.478-481,2000.

[10] H .T. Bui, A.K. Al-Sher-idah, and Y. Wang, "New 4-transistor XOR and XNOR designs," in Proc. 2nd IEEE Asia Pacific Con f. ASICs, 2000, pp. 25–28.

[11] S. Goel, M. Elgamel, M. A. Bayoumi, and Y.Hanafy, "Design methodologies for high-performance noise-TolerantXOR–XNOR circuits," IEEE Trans. Circuits SystemI, Reg. Paers, vol. 53, no. 4, pp. 867–878, Apr.2006.

[12] V. Tiwari, D. Singh, S. Rajogopal, G. Mehta, R. Patel and F. Baez, "Reducing power in high-performance microprocessors" in Proc. Conf. Des. Autom, 1998, pp, 732-737.

