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RESISTIVE TYPE SOLID STATE FAULT CURRENT LIMITER FOR IMPROVEMENT OF TRANSIENT STABILITY OF DFIG BASED WIND GENERATOR

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Abstract: *transient stability is one important parameter in case of inter connected power system. With the involvement doubly fed induction generator (DFIG) based wind generator (WG) system, transient oscillations in the system increases. To reduce these oscillations or to improve the transient stability of the system, this paper proposes resistive type solid state fault current limiter (R-type SSFCL) with simple controller. The proposed method applied on test system and compared with series dynamic breaking resistor (SDBR) and LR type solid state fault current limiter (SSFCL-LR) methods. The proposed method compared with these methods under different fault conditions, the results demonstrated that the proposed method effectively improves the transient stability.*

Keywords: *Doubly fed induction generator (DFIG), Resistive type solid state fault current limiter (R-type SSFCL).*

I.INTRODUCTION

In the beginning of 21st century, the world electricity demand is increasing very rapidly because of the advanced technology and industrial growth. The major part of these electricity demands is fulfilled through the conventional energy. In general, the conventional energy is dependent on the fossil fuels- coal, oil, and gas, which are very limited as well as air is also polluted by using of conventional energy sources. Therefore, due to the environmental concerns and inadequacy of fossil fuel resources, the electric power industries are placing more emphasis on the renewable energy resources or green energy sources with respect to economical and availability prospects. Among the various viable renewable energy sources including hydro, wind, solar, and geothermal resources, wind energy becoming the most prominent energy resources and fastest growing power generation technologies in comparison to others renewable energy sources due to its low maintenance cost, high production capability, no air pollution and availability in several parts of the world. Moreover, wind energy is endless energy resources in the power network. In [1], it is reported that throughout the world, total 760 GW of the wind power will generated by the end of year 2020.

The modern wind power extraction technology prefers variable wind speed generators instead of fixed speed due to its ability to capture more wind energy. The applications of DFIGs are currently most popular among all of the variable generators because of its flexibility in operation, large scale production, and fault ride through capability with lower converter losses [2]. However, in the event of grid fault or any kind of disturbance on the transmission line, the transient stability of DFIG is more vulnerable to the system as the stator windings of the DFIG is directly connected with the power system network as well as during fault, DFIGs terminal voltage goes very low from the nominal value, generator speed goes very high and high fault current flow through the converters of DFIG, and finally system becomes unstable [3]. According to the grid code, DFIG should be kept connected with the network even during fault. For this reason, to accomplish the requirements of the new grid codes and to ensure continue operation on the grid side, it is necessary to find a suitable solution to improve the transient stability of the DFIG based wind power systems and low voltage ride through (LVRT) capability during fault [3].

In literatures, it was found that to enhance the transient stability of the DFIG based WG, some energy storage systems (flywheel energy storage (FES) [4], superconducting magnetic energy storage (SMES) [5]), reactive var compensators (Static Synchronous Compensator (STATCOM) [6]), unified power flow controller (UPFC) in [7]. These devices basically provide a large amount of reactive power after the fault occurrence to recover the flux of the air gap. The above mentioned shunt compensators can improve the transient stability of the DFIG based WG, but the energy storage systems and reactive power compensators (RPC) required a large capital investment. Sophisticated power electronics based converter makes the power network more complex and more costly. For instance, in STATCOM additional converter, complex control strategy and coupling transformer is required. On the other hand, although the SMES and UPFC is very efficient to control the active power and the voltage during the fault, but both SMES and UPFC devices are most complex devices in terms of device structure, controller structure and the cost. According to recent literature, to improve the transient stability of DFIG some series compensators have been investigated as well, such as the bridge-type fault current limiter (BFCL) [8], inductive–resistive-type solid-state fault current limiter (SSFCL-LR) [9], superconducting fault current limiter (SFCL) [10], series dynamic braking resistor (SDBR) [11], non-superconducting fault current limiter (NSFCL) [12]. In [13], it is reported that to improve the voltage profile at the point of common coupling (PCC), the series compensating devices are more effective than the shunt compensating devices for a given MVA size.

Based on the above background, this paper proposes a simple effective controllable structure, using an R-type SSFCL and applied on a DFIG based variable speed WG to improve the transient stability. The proposed circuit operation both in normal and fault conditions are simulated and observed the transient stability performance. In this work, a 2MW DFIG based variable speed WG system has been considered.

II. MODELING OF DFIG

The Doubly-Fed Induction generator (DFIG) is an induction machine, where its stator is directly connected with the grid, but the rotor winding is connected to the grid through AC-DC- AC converter. The converter is divided into two components: Rotor-side converter (RSC) and Grid side converter (GSC). A dc-link capacitor is connected between these two converters, in order to keep variation of the voltage in a small range. In this research, to control the RSC and GSC converters of the DFIG, the vector control method is used [10].

The basic diagram of DFIG is shown in Fig. 1 and power converters of RSC, GSC are shown in Fig. 2a and 2b respectively. In DFIG, the rotor side converter (RSC) is connected with the generator rotor side as shown in Fig. 2(a). The main purpose of the RSC is control to the real and reactive power of the DFIGs stator terminal [10]. The RSC is a power electronic full bridge 2-level, 6-pulse converter. Converter. Therefore, it is possible to control the rotor speed of the generator, hence the speed of the wind turbine. The RSC controller takes the terminal active power, the reactive power, and terminal voltage as inputs and controls the output active and the reactive power with the help of the controller. The main purpose of the GSC controller is to keep the fixed dc-link voltage and helps to keep a constant power method is used. In this scheme, the d-axis current component is used to keep the dc-link voltage constant, and a q-axis current component is used to control the reactive power of the DFIG [16]. In DFIG, the GSC ensures balanced power energy on the both sides of the dc-link capacitor by maintaining the dc-link voltage. In order to design the GSC, two series PI controllers are used in this work. The gain parameter values of the GSC controller are shown in Fig. 2(b). The GSC controller also contains a 2- level, 6-pulse based full bridge power electronic converter. It uses the dc-link voltage and the reactive power from the rotor line as inputs and sends the desired signal with the processing of the PI controller and carrier frequency of the GSC controller. In this paper, a 16000 µF power capacitor is used to smooth the dc voltage ripple of and maintain constant 1200 Volts.

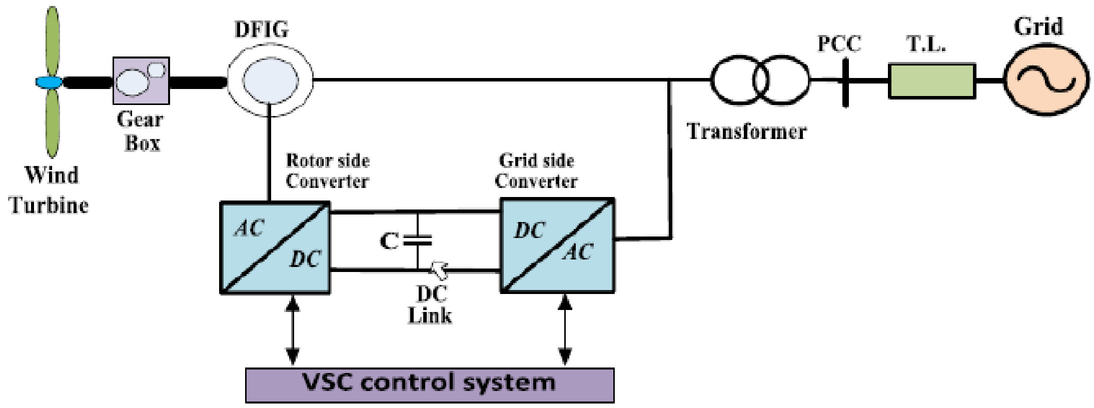


Fig.1 Configuration of DFIG.

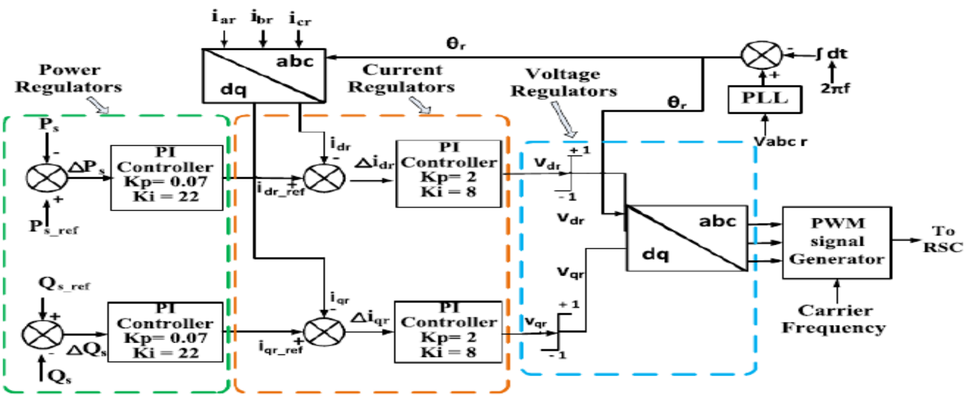


Fig.2a Configuration of RSC.

III .PROPOSED RESISTIVE TYPE SOLID STATE FAULT CURRENT LIMITER

Fig. 3a shows the configuration of the proposed single phase R-type SSFCL. The proposed structure is composed of three main parts that are briefly explained as follows.

1. The R-type SSFCL is based on diode bridge rectifier, which consists of four diodes D1-D4
2. A high impedance of shunt resistor R_{sh} is placed in parallel with the bridge part of the circuit.
3. An ZnO arrester is used in the proposed R-type SSFCL, which is connected in parallel with the shunt resistor.

In the steady state condition the self-turn-off IGBT switch remains closed and the rectifier diode bridges of the R-type SSFCL carries the line current. For one half cycle, the line current is carried through the path D1-L_{DC}-D4 and other half in D2- L_{DC} – D3 carry line current. Thus, the combination of the four diodes of the proposed method operates in near dc condition in each phase and the inductor of L_{DC} acts as a short circuit. Therefore, the total line current will flow through the rectifier diodes bridge part minimizing the devices impact under normal conditions. In the event of fault, the line current rises abruptly. The reactance of $L_{DC\ =0.1}$ limits this rate of increase in the line current, protecting the semiconductor IGBT switch from large $\frac{di}{dt}$ value at the beginning of fault. At the event of fault, the dc current crosses over than the present maximum permissible reference current, and the controller of the R-type SSFCL is turned off the IGBT switch. After that, high current through the line is bypassed to the shunted path of the circuit, which helps limit the fault current and consumes the excess energy from the DFIG to ensure the transient stability of the system.

Fault current and consumes the excess energy from the DFIG to ensure the transient stability of the system. In this present work, ZnO arrester is used to minimize over voltage conditions. During the fault, high current will Bow through the circuit. The sudden interruption of high current results peak volt-ages impressed onto the circuit, which can damage internal com-ponents of the circuit [14]. The ZnO device has high impedance during the normal operating condition and does not conduct, when the voltage across the ZnO device is smaller than conduction threshold and this state is considered in this work as the OFF mode of the ZnO device. On the other hand the ZnO device has low impedance, when the voltage across ZnO device is higher than the threshold value, the device is considered as the ON mode [19]. Therefore the ZnO device is used as a switching device in this work and it protects the circuit from the over voltage. The fault is isolated by opening the circuit breaker, and the system begins to recover. As the PCC voltage reaches its predefined reference voltage. Viet the R-type SSFCL control system will be forced to turn on the IGBT switch and the system will return to normal operation.

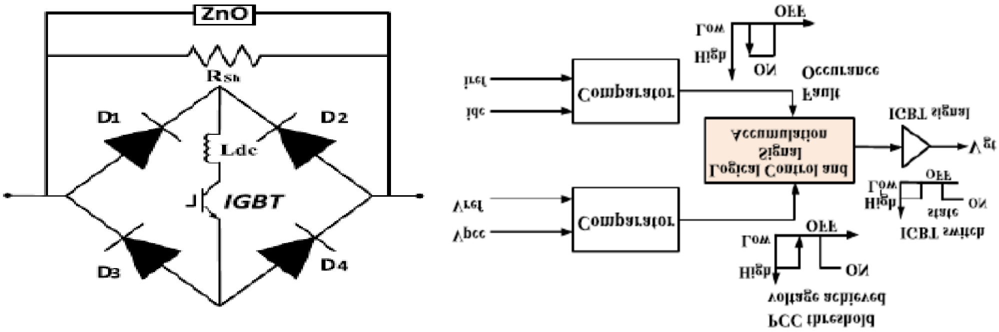


Fig. 3 a & b Construction of proposed R-type SSFCL and its controller respectively.

IV . TEST SYSTEM & RESULTS

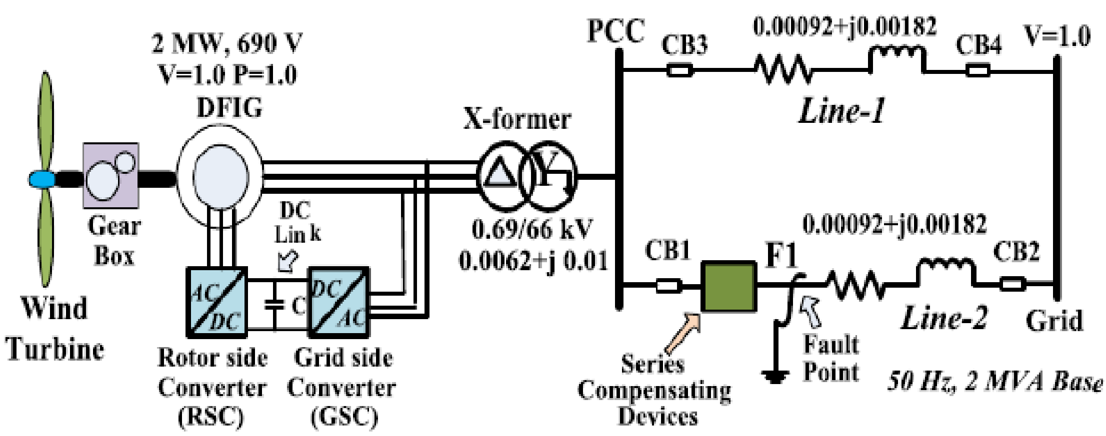


Fig.4 Tested model system with DFIG.

In this section, all simulation results and graphs are discussed for three-line-to-ground (3W) faults only. Fig. 6a shows the DFIG terminal voltage response after applying a temporary 3LG fault. Without auxiliary device, the DFIG terminal voltage goes almost zero right after fault, and continues at a sustained lower voltage range until the circuit breakers open. When the series devices are connected to the system, the voltage profile improves. However the improvement of the DFIG terminal voltage profile varies with each device. Although the SDBR and SSFCL-LR can improve the terminal voltage and maintain the ±0.1 p.u. of nominal value, but the simulation graphs clearly indicate that the performance of the proposed R-type SSFCL is superior to all devices in terms of voltage stability. By using the R-type SSFCL. The DFIG terminal voltage returns to 0.925 p.u. of its nominal value very quickly when compared to the SDBR and SSFCL-LR.

The speed response curves of the DFIG for four cases are shown in Fig. 6(b) and it is observed that by using the proposed R-type SSFCL, the machine speed of DFIG has lower oscillation compared to using the SDBR and SSFCL-LR for 3W fault. Fig. 6(c) represents the simulation response curve of active power for all the four cases. Without any controller, the DFIG active power goes to zero right after the 3W fault. The R-type SSFCL. SDBR and SSFCL-LR has the ability to maintain the steady state power, however the performance of the R-type SSFCL is better than the SDBR, and SSFCL-LR in terms of active power stability. The active power consumption by the series compensators during the 3LG fault is shown in Fig. 6(d). It can be seen that the R-type SSFCL consumes more active power than the SDBR and SSFCL-LR during the fault occurrence. This helps the R-type SSFCL provide better transient stability, performance. Moreover, we can *see* from Fig. 6(d), the R-type SSFCL SDBR and the SSFCL-LR does not consume any active power under normal condition.

In Fig. 6(e), shows the DC link voltage responses for 3LG fault. Without controller, the DC link voltage increases promptly from 1.0 p.u. to 1.58 pu during the fault. The R-type SSFCL maintains the DC link voltage with less fluctuation and more stability than the SDBR and SSFCL-LR. Fig. 6(f) shows the line current increases to 4.5 p.u. during the 3LG fault if the DFIG has no auxiliary controller. From the simulation curves, it can be seen that the R-type SSFCL suppresses the fault current from 4.5 p.u to 1.2 p.u. The SSFCL-LR and the SDBR can limit the line current from 4.5 p.u. to 1.35 and 1.4 p.u respectively. Therefore, the R-type SSFCL has the ability to better limit the fault current during the fault as compared to the SDBR, and SSFCL-LR. Fig. 7(a) shows the DFIG terminal voltage responses for 3LL fault. From this figure, it can be stated that the proposed R-type SSFCL can retain the DFIG terminal voltage faster than the SDBR and SSFCL-LR This simulation indicates the performance of R- type SSFCL is better than the SSFCL-LR and SDBR. The machine speed, active power. DC link voltage, and current response curves for all devices are shown in Fig. 7(b) to (e) respectively. From the graphs, it can be seen that the proposed R-type SSFCL performs better than the SSFCL-LR and SDBR with respect to transient stability. Fig. 7(I) shows the active power consumption curves in the event of 3LL fault and it is clear visualized that the R-type SSFCL improves the transient stability of the DFIG based WG and per-formed well in comparison to SSFCL-LR and SDBR by consuming more active power than the SSFCL-LR and SDBR. In this paper 2LG fault is considered to analyze the transient stability performance among the series compensators. The DFIG terminal voltage responses for all cases in the event of 2LG fault is shown in Fig. 8(a). In Fig. 8(a). it is seen that the DFIG terminal voltage sag goes to 0.47 p.u. without any auxiliary devices. The voltage profile improves over 0.90 p.u and enhances the transient stability through the all series device. However, the R-type SSFCL outperforms the SDBR and SSFCL-LR by keeping the voltage level over 0.948 p.u.

Fig. 8(b), represents the active power responses of the DFIG during 2LG fault. It is seen from the simulation curves that the output active power dip goes to 0.65 p.u. without controller. But by employing the series devices, the DFIG active power fluctuation becomes less and improves the transient stability performance in the 2LG fault. However the performance of R-type SSFCL is better than the SDBR and SSFCL-LR. The speed response of the DFIG for all cases is shown in Fig. 8(c). From Fig. 8(c), it can be stated that. The speed response of R-type SSFCL is much better when compared to SDBR and SSFCIA.R. The DC link voltage under the 2LG fault is shown in Fig. 8(d). The R-type SSFCL aids to keep maintains the variations of the dc-link voltage and more stable when compared to SDBR and SSFCL-LR. Fig. 8(e) and (f), represents the simulation response curve of current and active power consumption respectively for 2W fault. From Fig. 8(e), it can be seen that the proposed R-type SSFCL can mitigate the fault current compared to the SSFCL-LR and SDBR. On the other hand, the proposed R-type SSFCL consumes more active power than the others, which indicates that the R-type SSFCL performed well in comparison to the SSFCL-LR and SDBR.

The terminal voltage, active power, the machine speed and DC link voltages responses for 2LL fault is depicted in Fig. 9(a)-(d). It may be seen, from the simulation curves that the proposed R. type SSFCL can improve the transient stability by restoring the KC voltage level faster than the SSFCL-LR and SDBR, as well as yielding superior performance, maintaining a small variations of output power, machine speed and DC link voltages than the SSFCL-LR and SDBR during the 2LL fault. In addition, this paper considers a 1W fault due to the 1LG fault being the least severe and the most common fault compared to 3W and 2W fault. Fig. 10(a) shows that without controller, the DFIG terminal voltage sag goes to 0.68 p.u. during the 1LG fault. It is evident that the all series device improves the voltage profile and enhances the transient stability by maintaining the voltage level over 0.96 p.u. But the performance of R-type SSFCL is better than others in terms of voltage profile.

Fig. 10(b) shows all series improves the DFIG active power under 11.G fault. *However*, the II-type SSFCL have less oscillation compared to others. The speed variation of the DFIG under 1LG fault is shown in Fig. 8(c). The effect of the series devices on DF1G during 1LG fault is not significant. All series devices can control the speed during the ILG fault. The DC link voltage shows in Fig. 10(d). The variation of the DC link voltage is minimal for all series devices, but from the Fig. 10(d), it is clearly visualized that the 12- type SSFCL has lower oscillation compared to SDBR and SSFCIAR, which indicates that the proposed R-type SSFCL can enhance the transient stability of DFIG based WG and works better than the SDBR and SSFCL-LR.

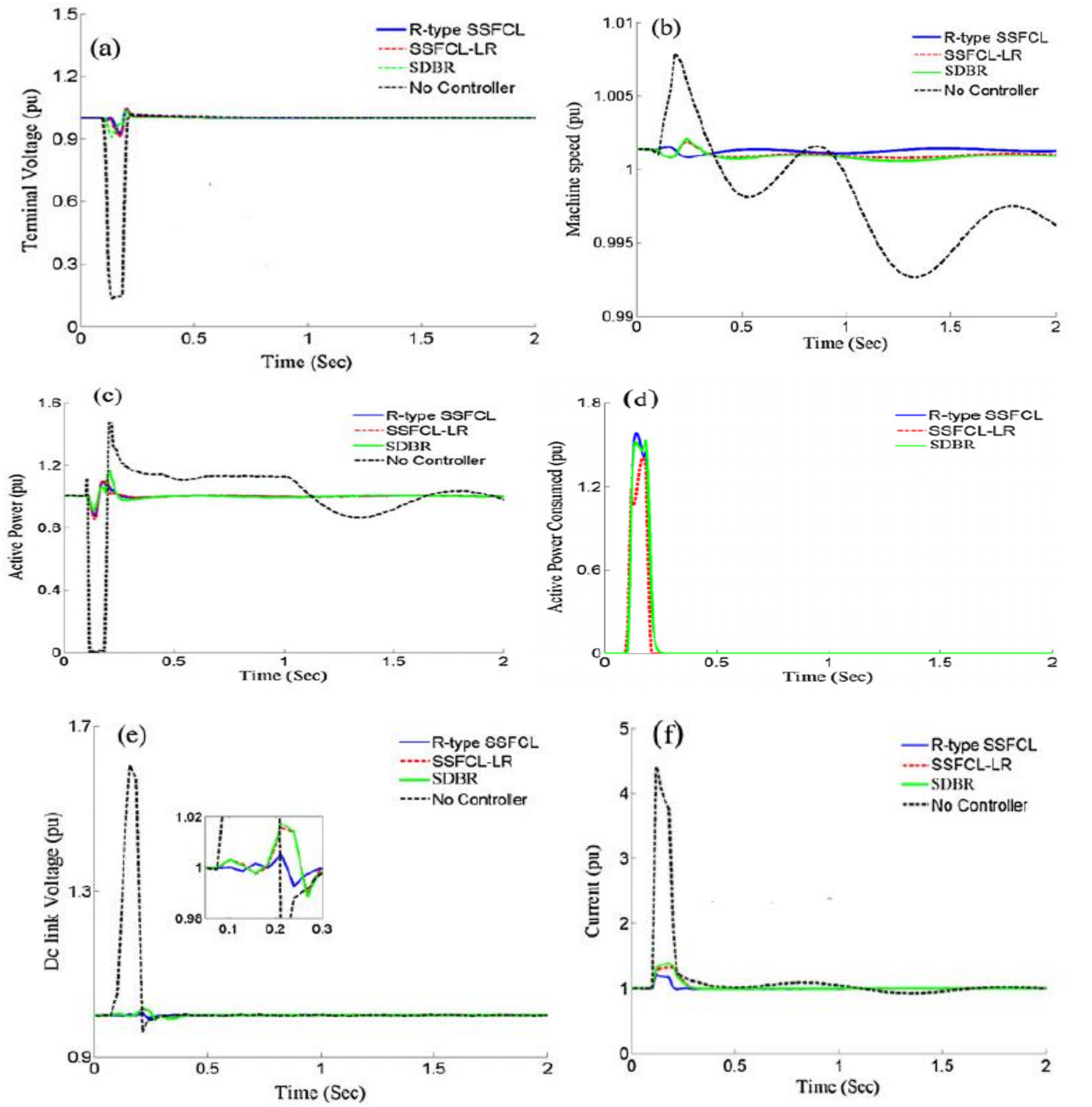
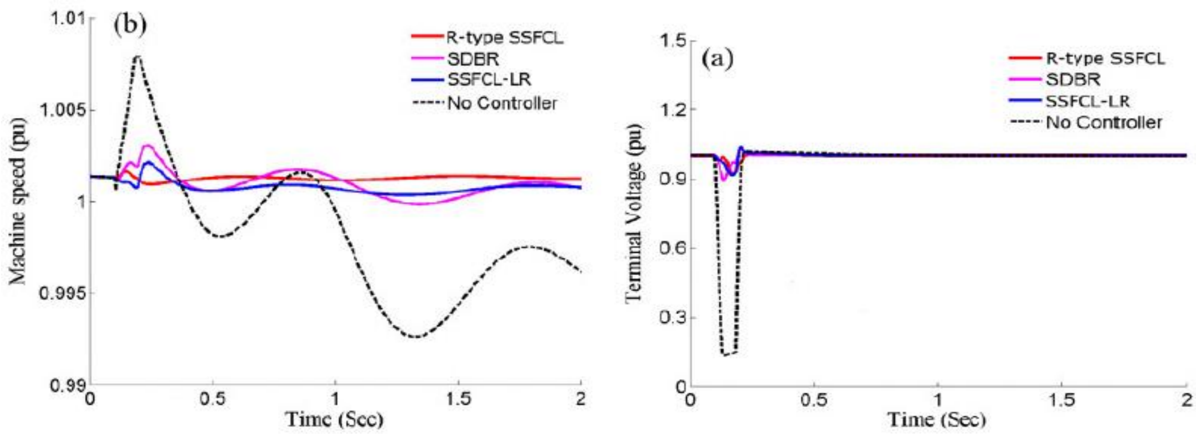


Fig.6 Simulation results of DFIG for 3LG fault: (a) Terminal voltage; (b)Speed: (c) Output active power: (d) Active power consumed by the series devices; (e) DC link voltage; (0 Stator current of DFIG.



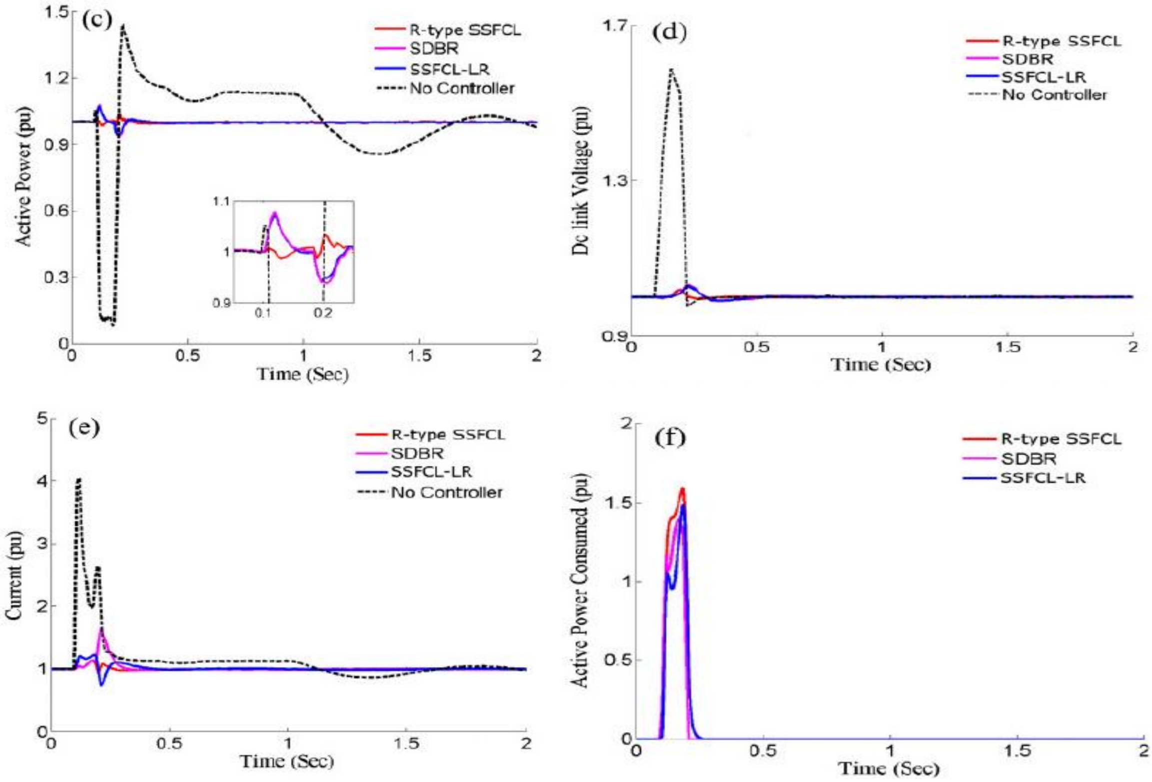
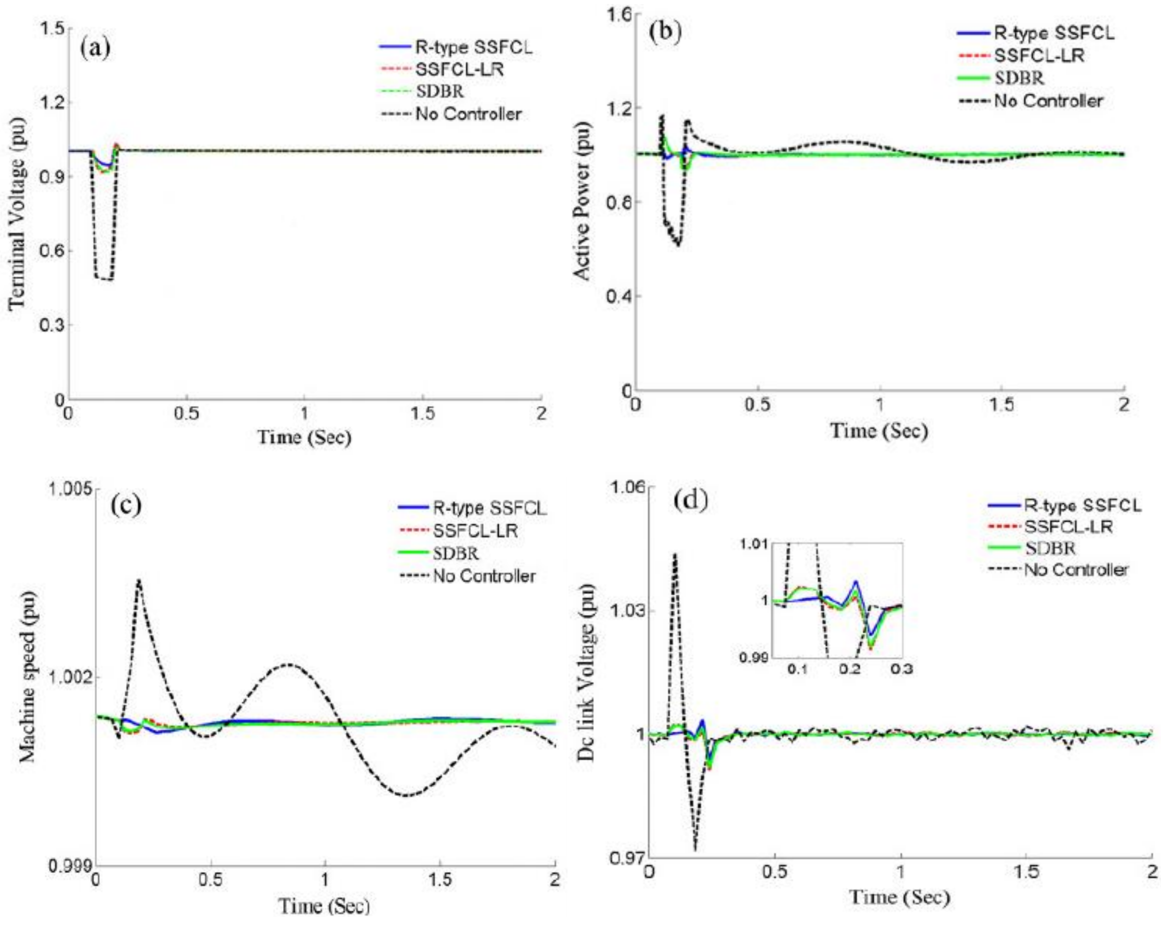


Fig. 7 Simulation results of DFIG for 3LL fault: (a)Terminal voltage: (b)Speed: (c)Output active power. (d) DC link voltage: (e)Stator current of DFIG: (f)Absorbed power by the series devices.



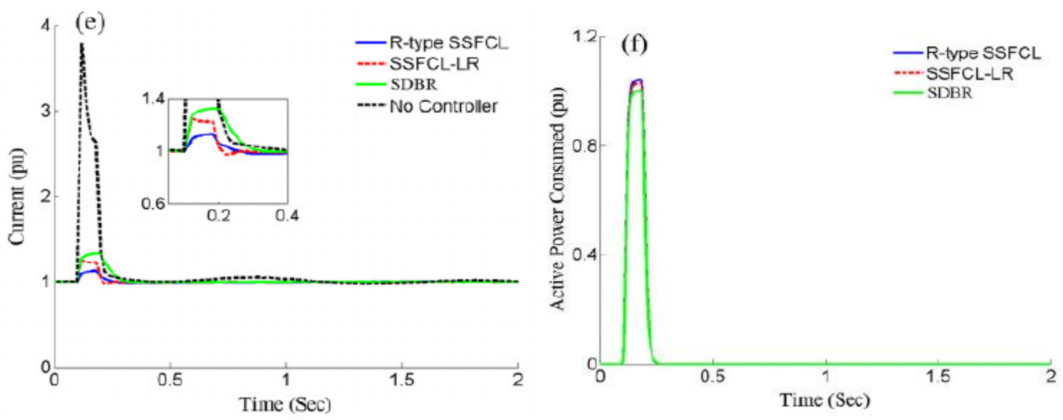


Fig. 8 Simulation results of DFIG for 2LG fault: (a)Terminal voltage: (b)Speed: (c)Output active power. (d) DC link voltage: (e)Stator current of DFIG: (f)Absorbed power by the series devices.

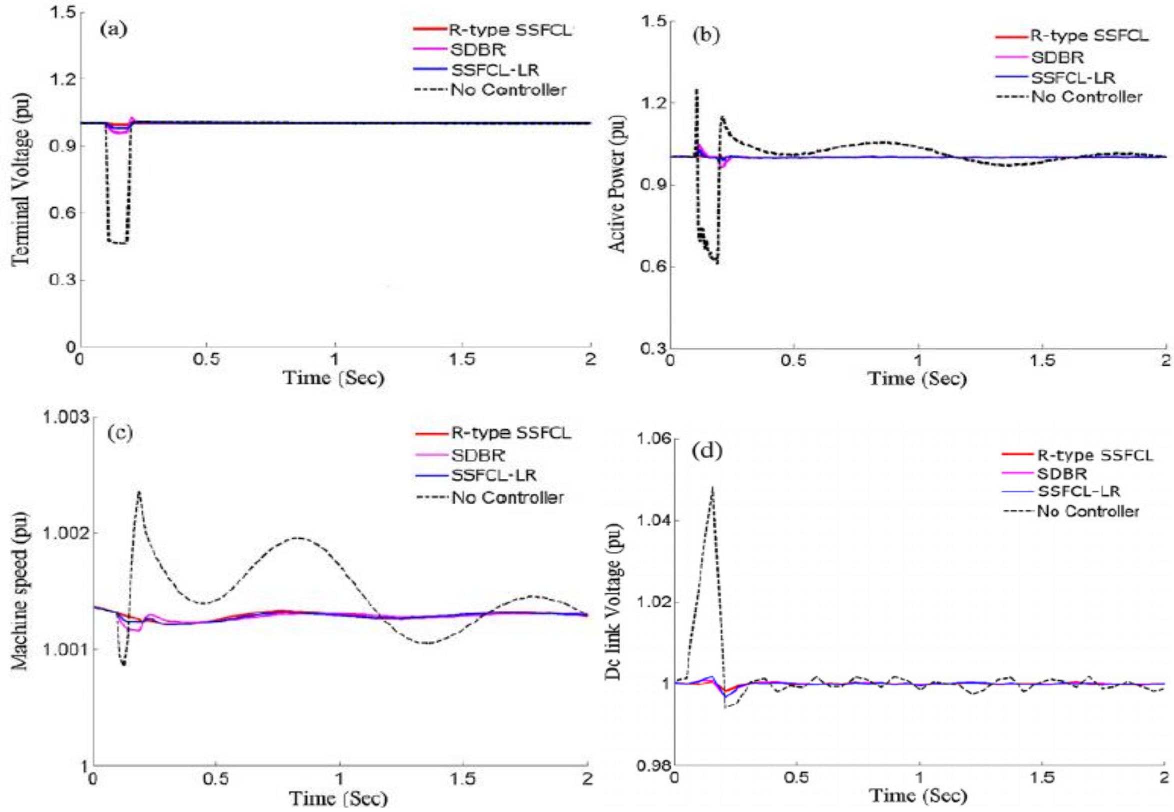
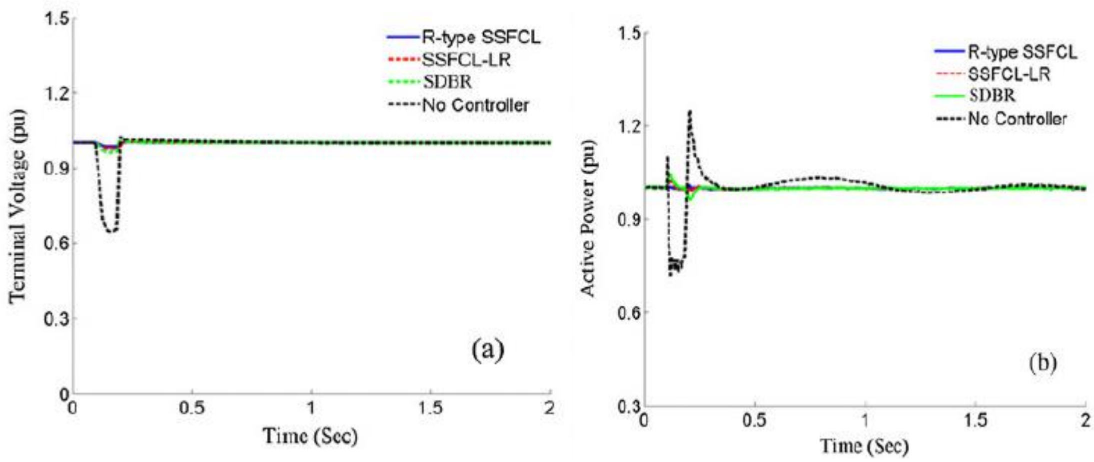


Fig. 9. Simulation results of DFIG for 2LL fault: (a) Terminal voltage: (b) Output active power: (c) Speed response: (d) DC link voltage.



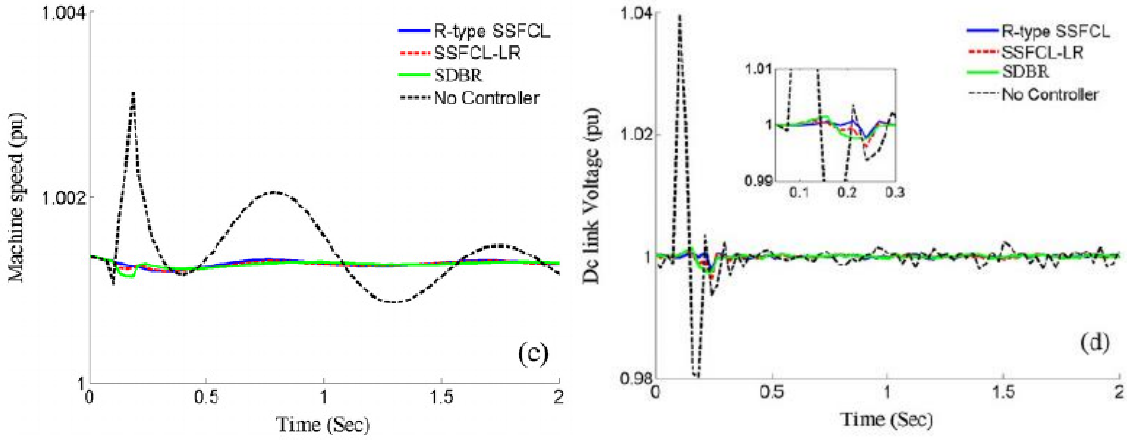


Fig. 10. Simulation results of DFIG for 1LG fault: (a) Terminal voltage: (b) Output active power: (c) Speed response: (d) DC link voltage.

V . CONCLUSIONS

In this work, the proposed R-type SSFCL structure, operation, and simulation results with a details explanation is presents. The proposed R-type SSFCL and SSFCL both series devices performed well in DFIG based WG, however at the conclusion, from all explanations with proper evidence, the proposed device (R-type SSFCL) appears to be very effective in enhancing the transient stability of the DFIG based WG and it performed better than the SSFCL-LR and SDBR. Lastly the following points can be summarized from this work -

i. The proposed R-type SSFCL is performed well and has the capability to improve the transient stability of the DFIG based variable speed WG system both for balanced and unbalanced faults.
ii. The R-type SSFCL has the ability to maintain the voltage level 0.1 p.u. of the nominal value at PCC point and can mitigate the high current significantly during the fault time compared to SSFCL-LR and SDBR.
iii. The R-type SSFCL stabilizes the machine speed during a fault, thus DFIG faces low stress and improves the transient stability.
iv. The R-type SSFCL can maintain the output power very smoothly and effectively by consuming more active power than the SDBR and SSFCL-LR during fault time.
v. The R-type SSFCL controller is very simple and easy to implement in the power networks.

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