Scientific Journal of Impact Factor (SJIF): 4.72

e-ISSN (O): 2348-4470
p-ISSN (P): 2348-6406

International Journal of Advance Engineering and Research Development

Volume 4, Issue 11, November -2017

Design of DPLL and Implementation of BIST to Evaluate its Characteristics

[1]PANCHETI HAREESH, [2]SIMHADRI VENKATA ABHISHEK

[1]Asst. Professor, Sir CR REDDY college of engineering, Eluru, A.P.
[2]M.tech, Sir CR REDDY college of engineering, Eluru, A.P.

Abstract — *All digital systems need to synchronize between Integrated Circuits and functional blocks, mainly to progress digital systems operations for excellence in performance. Future processors need to work with different ICs and IPs, whose operating speed is different; there is requirement for high speed clocks. This has to be done by just using the low frequency on board clock. To generate the on-chip clocks to have well-timed, Phase locked-loops (PLLs) are used. But designing a fully digital PLL is needed because all the designs are digital and analog component will need more power and will reduce efficiency. Most of the traditional PLL are monolithic design with other circuits. The proposed DPLL is just based on counters, dividers and digital phase lock detectors which are easy to fabricate when compared to analog component and can be integrated in any system easily. It can generate wide range of frequencies and has in built BIST to test the operation of PLL and to determine characteristics like lock time, jitter and duty cycle. The experimental results of DPLL with waveforms are shown for 50 MHz reference clock signal to generate 200 MHz clock DPLL. BIST for the PLL is implemented using TESSENT TOOL.*

Keywords *- DPLL, BIST, TESSENT, PLL, DCO, JTAG, TAP, DTAB.*

I. INTRODUCTION

Basically, PLL has three blocks as shown in the Fig.1. Phase error detector detects the phase difference between the two input signals i.e. it generates error signal between them. Digital filter is mainly used to suppress the lower frequency signals, so in analog model LPF is mainly used, but in digital circuits the functionality of LPF can be achieved by using counters. Digital controlled oscillator generates pulses depending on the output of digital filter, this will continue until the phase error becomes zero and then the PLL is locked.

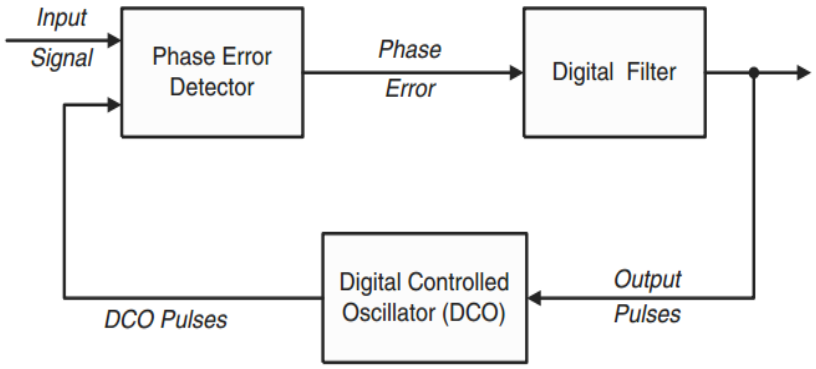

Fig. 1: Block Diagram of DPLL

II. PROPOSED TECHNIQUE

In the proposed technique, fully digital PLL is designed by using counters, dividers, and multipliers. The frequency of the output signal depends up on the values of dividers. The relation is expressed in Equation 1.

$$Op_{fr} = \frac{F_{ref} * Fb_{en}}{In_{en} * Op_{en}} \quad (1)$$

Where,

Op_{fr} = Output frequency,
In_{en} = Input divider value,
Op_{en}=Output divider value,
F_{ref}=Input frequency.

The proposed Architecture is shown in the Figure 2.
The features of DPLL includes power, area, range of operating frequency,are shown below.

Features of the DPLL:

- Power Supply of 0.8V.
- Low power – typically 1.6mW.
- Frequency range of DCO 800 – 3200 MHz
- Area 80x160µm2.
- Low output jitter.
- Bypass mode.
- Programmable input, feedback and output dividers provide frequency agility.
- Function for PLL lock detection.
- Power-down capability.
- ESD protection and power supply bypass are fully integrated in PLL.
- Locktime=(4xLOCK_DETECT_COUNT)*(REF_CLK period * Encoded REFDIV value).

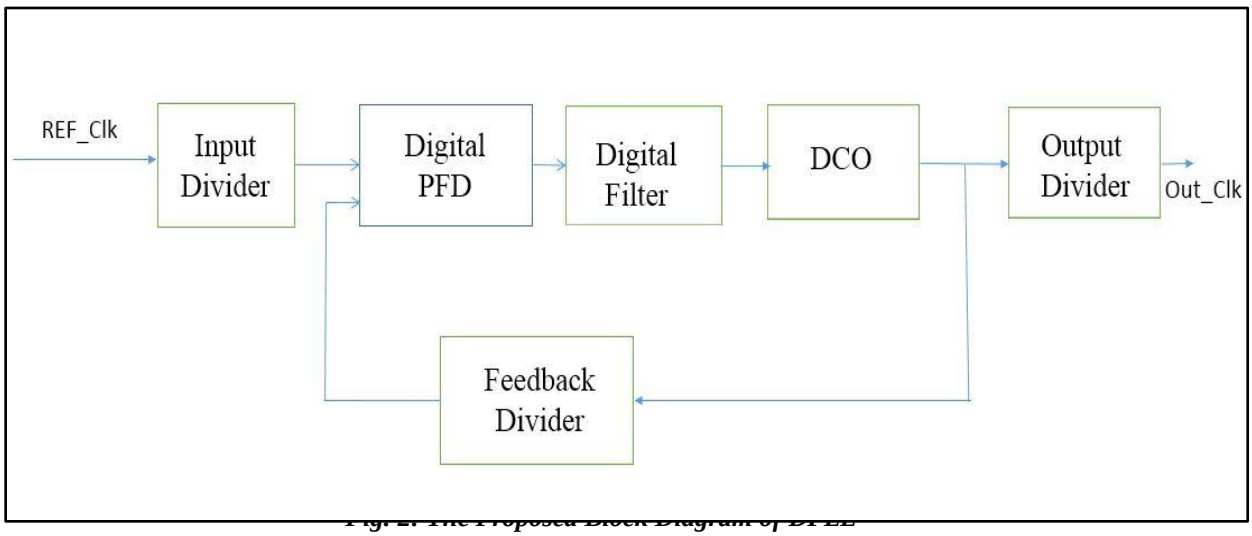

Fig. 2: The Proposed Block Diagram of DPLL

The waveforms for generating of signal frequency of 200 MHz are shown in Figures 3-5.The input reference clock frequency is shown in Figure 3 by observing the time period of the REFCLK which is 20,000ns i.e.,the lock state of the DPLL is observed from the Figure 4, the clock is generated when lock state is achieved by PLL.

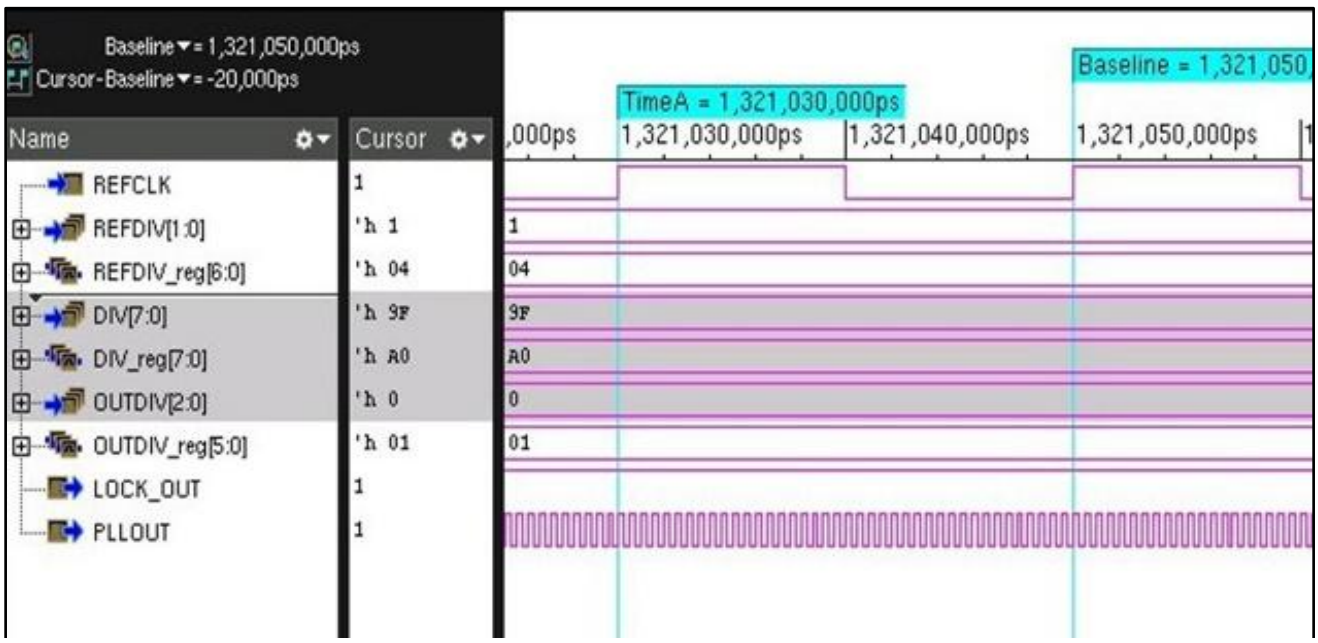

Fig. 3: Observation of input REFCLK frequency

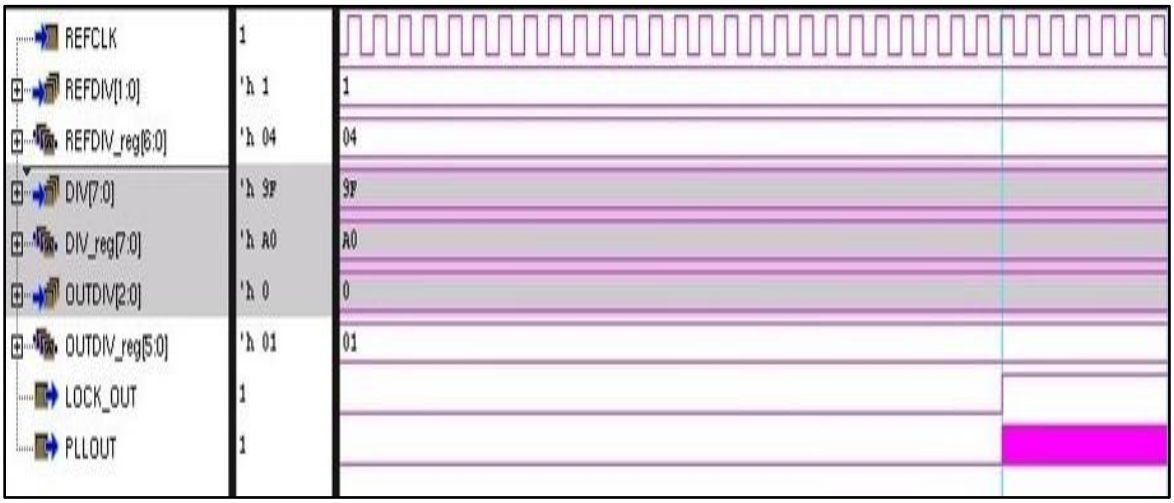

Fig. 4: Observation of lock state indicated by the signal, LOCK_OUT.

The frequency of the output waveform generated is 200MHz which can be observed in Figure 5.

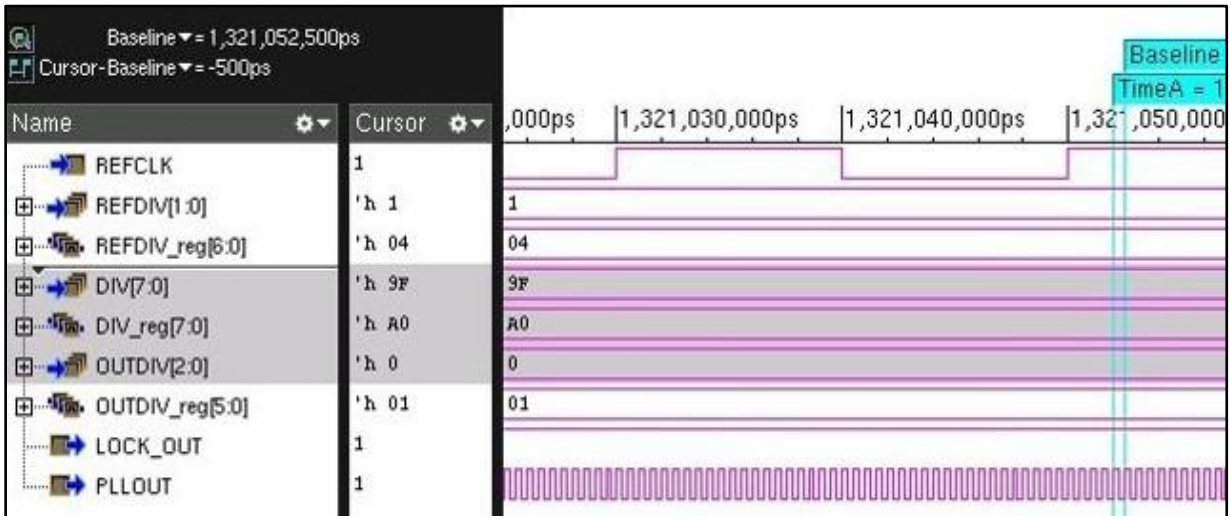

Fig. 5: Observation of the output signal PLLOUT frequency.

The reset sequence operation is demonstrated in the figure 6 given below.

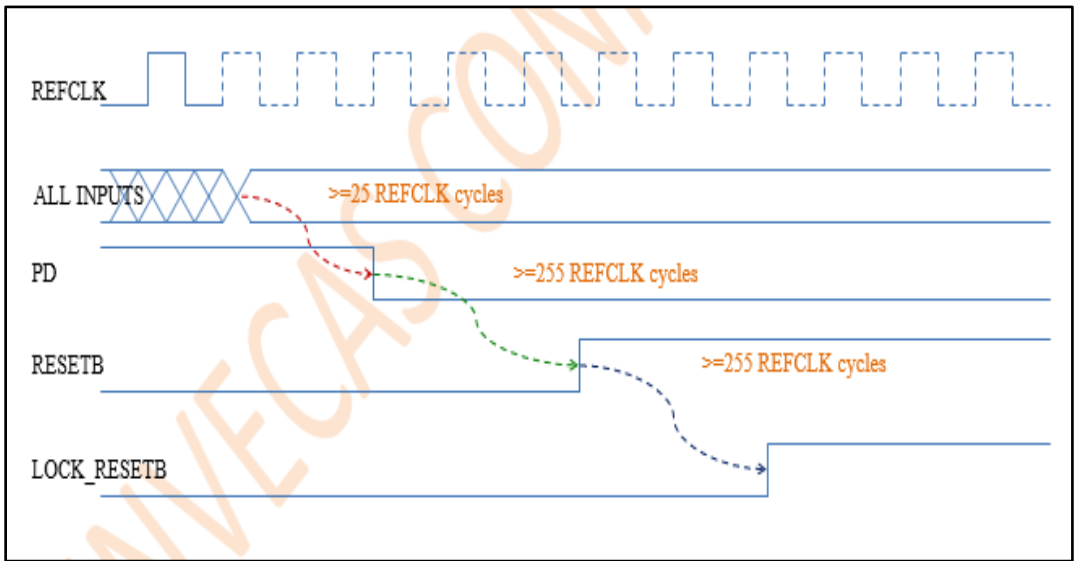

Fig 6: Reset sequence of proposed DPLL.

The default values of some of the signals is shown in the Table 1 given below.

- **TIMEOUT_COUNT_VAL**: should be greater than 4 times the lock_detect_count value. The internal fsm in pll model is designed such that the lock is achieved after 4 internal states with each state's time limit set to lock_detect_count value.
- **LOCK_PHASE_ERROR, UNLOCK_PHASE_ERROR** are set to 'h004.
- The maximum tolerance imposed on phase detector is the **LOCK_PHASE_ERROR** i.e. the phase error between refclk and the internal fb clock is 4.

Signal	Value
LOCK_DETECT_COUNT	'H1000
TIMEOUT_COUNT_VAL	'H8000
UNLOCK_PHASE_ERROR	'H0004
LOCK_PHASE_ERROR	'H0004

Table 1: Default values of the signals

REFDIV[1:0]	ENCODING
00	1
01	2
10	4
11	NA

Table 2: Encoding of input divider

The encoding of DPLL input and output dividers depends upon the way of requirement which is completely based designer. The values provided by the dividers are always the powers of 2. The encoded values of the input and output dividers can be shown in the tables 2 and 3 respectively. REF_DIV indicates the input divider which is a two-bit signal. Since it is a 2-bit signal, it has four combinations such as 00, 01, 10 and 11. Encoding values completely depends upon the requirement of the clients such that the values can be taken as either 1, 2 or 4 as shown in the Table 2. OUT_DIV indicates the output divider which is a three-bit signal. Since it is a 3-bit signal, it has eight combinations such as 000, 001, 010, 011, 100, 101, 110 and 111. Encoding values completely depends upon the requirement of the clients such that the values can be taken as either 1, 2, 4, 16, 32 as shown in the Table 3.

The DC characteristics of the DPLL such as Power Supply, Operating Junction Temperature and Supply Current are shown in the Table 4.

- The power supply should be in the range of 0.72-0.92V (volts).
- The temperature should be in the range of 0-125°C.
- Supply noise is 1 GHz square wave with 20ps tr/tf on VDD.
- Deterministic jitter measured with eye diagram over 250 VCO cycles, with output divider=1.

III. BUILT-IN SELF-TEST FOR DPLL

JTAG is the name used for the IEEE 1149.1 standard entitled *Standard Test Access Port and Boundary Scan Architecture* for test access ports (TAP) used for testing printed circuit boards (PCB) using boundary scan. JTAG is the acronym for *Joint Test Action Group*, the name of the group of people that developed the IEEE 1149.1 standard. The functionality usually offered by JTAG is *Debug Access* and *Boundary Scan*.

- **Debug Access** is used by debugger tools to access the internals of a chip making its resources and functionality available and modifiable, e.g. registers, memories and the system state.
- **Boundary Scan** is used by hardware test tools to test the physical connection of a device, e.g. on a PCB. Although this is usually not the task of a debugger tool the TRACE32 debugger offers mechanisms to access the JTAG TAP in a generic way, e.g. to perform boundary scan using a PRACTICE script or a custom application.

Although the TAP (Test Access Port) access itself is generic for all architectures, the functionality implemented behind JTAG is different for each device. JTAG is defined as a serial communication protocol and a state machine accessible via a TAP.

OUT_DIV[2:0]	Encoding
000,110,111	1
001	2
010	4
011	8
100	16
101	32

Table 3: Encoding of output divider

Parameter	Min. Value	Max. Value	Units	Description
VPLL	0.72	0.92	V	Power Supply
Temp	0	125	°C	Operating Junction Temp
IDD	-	-	mA	Supply Current

Table 4: DC Characteristics of DPLL

Interface Signals:

The main block for this BIST is TAP Controller and the concept behind this is Boundary Scan. The concept, Boundary Scan can be simply demonstrated by using the Figure 5.2. The scan path which is serially connected between the pins & device core is known as the Boundary-Scan Register (BSR). This register have plenty of cells known as BSCs (Boundary-Scan Cells). These BSCs are not observable in standard operation. The schematic which represents the way of connection between all the signals with the DTAB block and the selection of the Data Register depending on the content of the Instruction Register shown in the Figure 7.TCK – The signal called as Test-Clock used for state-machine operations.

- TMS – The signal called as Test-Mode Select, changes at the rising edge of TCK. This signal is used to find the next state.
- TDI – The signal called as Test Data-input which portrays the data shifted into the device's logic either for testing or programming. It is also changes at the positive edge of TCK.
- TDO – The signal called as Test-Data output which portrays the data shifted out of the device's logic either for testing or programming and operates at the negative edge of TCK.
- TRST – The signal called as Test-Reset which can be used to reset the state-machine of the TAP. This pin is optional.

TAP Controller:

It consists of a state-machine of 16-states. The movement in the states is commanded by TMS signal. The state alone decides the position of the JTAG device. Data can be write or read whether from DR or IR.The TAP state-machine is shown in the Figure 8 given below.

The debug tool communicates with the DTAB by reading and/or writing IRs and DRs. The debug tool first drives the TAP Controller to the Shift-IR state to write the appropriate instruction to IR. Then it drives to the Shift-DR state where the DR can be read or written. Once the Update-DR state is reached, the processing of DR is started, e.g. the data contained in DR is forwarded to the on-chip debug system.

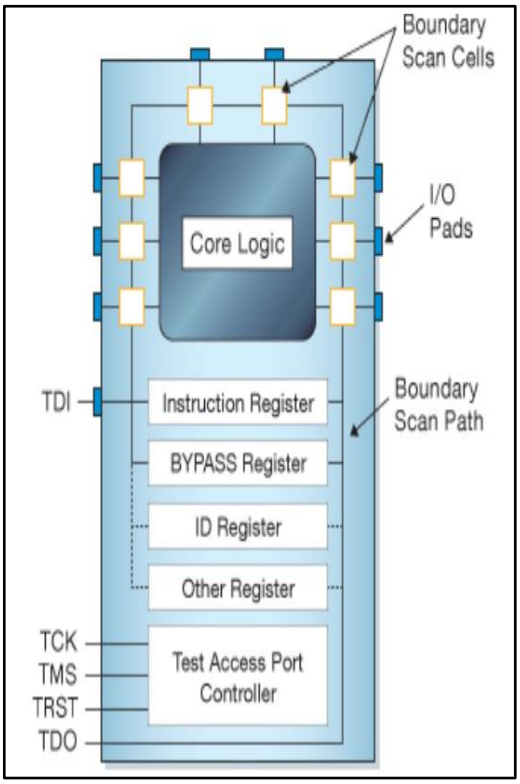

Fig. 7: Schematic Diagram of the JTAG

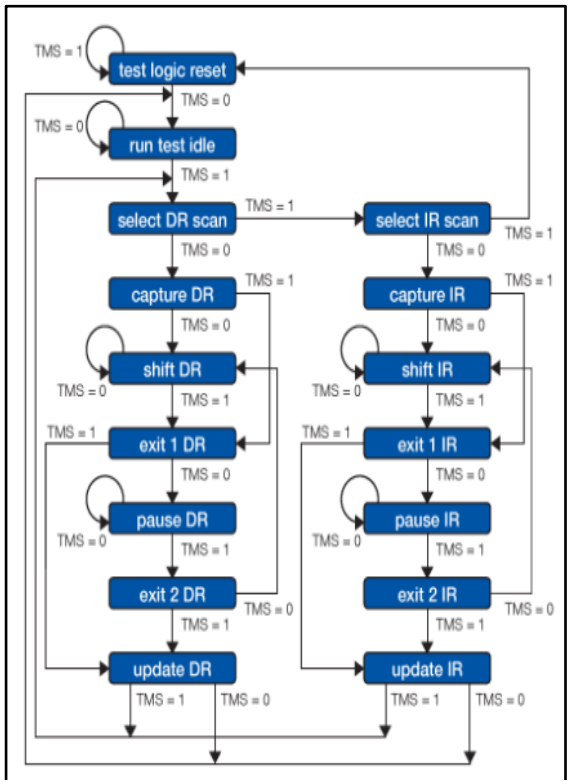

Fig. 8: TAP Controller State-machine

The following example shown in Figure 10 represents how the chip ID code is read on a Tri-Core processor (IR: 8 bits, IDCODE DR: 32 bits). Reading or writing the IR or DR is performed bitwise from LSB to MSB. With every bit shifted into the TAP controller via TDI, the contents of DR is right shifted one bit, providing the LSB on TDO that can be observed in the Figure 9.

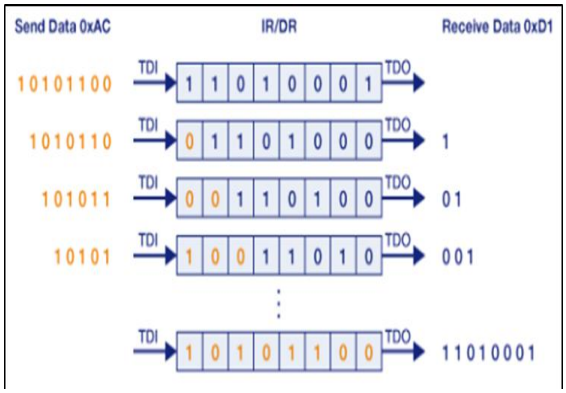

Fig.9: Loading of Contents into IR/DR

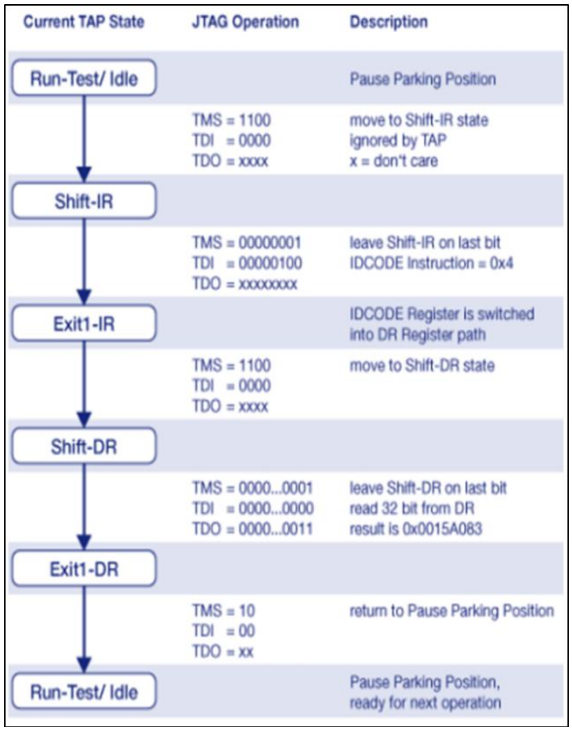

Fig. 10: Chip ID read on a Tri-Core Processor

RMS jitter is determined by implementing the BIST for PLL, is shown in Figure 13. Lock Time measurement for the PLL is shown in figure 14.

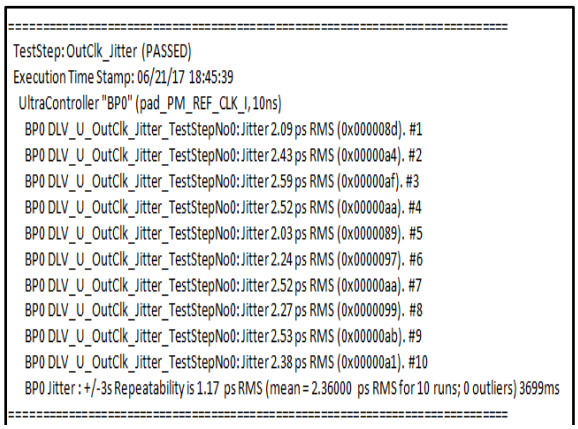

Fig. 13: RMS Jitter Measurement Log.

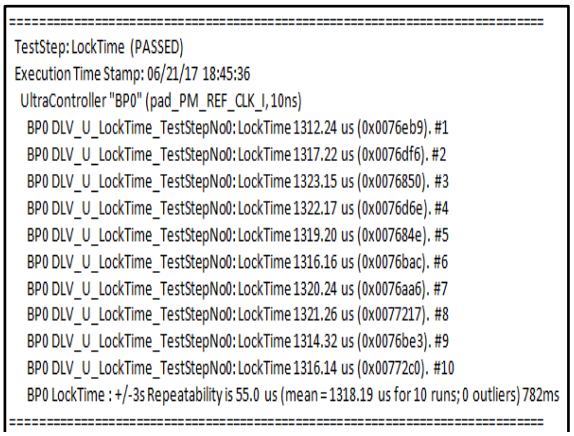

Fig. 14: Lock Time measurement log.

IV. RESULTS

DPLL is designed for the input frequency range of 25MHz-200MHz. The simulation results for the output of frequency 200MHz are presented here. By implementing JTAG and implementing the BIST for the PLL using TESSENT tool the lock time, output clock jitter and duty cycle of the clock can be determined.

V. CONCLUSION

The designed DPLL can be used for generating clock of high frequencies. It can also be used for DDR2/3. For same low frequency input reference clock we can generate same low frequency signal as well as high frequency signal by programming the input, output and feedback dividers. In this paper, a complete digital technique is signified for designing and testing of DPLLs in the operating frequency range of 25MHz-200MHz.

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