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IMPROVED DESIGN OF ALL-OPTICA HALF SUBTRACTOR BASED 2 - DIMENSIONAL PHOTONIC CRYSTAL

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Abstract- *Forthcoming Optical computers and Optical Signal Processors need all-optical devices in order to get rid of from Optical-Electrical-Optical conversions; Optical gates play a vital role in Optical networks. Photonic crystals (PhC) are periodic dielectric structures that have a band gap that forbids the propagation of a certain frequency range of light. This property enables one to control light with amazing facility and produce effects that are impossible with conventional optics and its dielectric constant can be varied occasionally. In this paper, Photonic crystal based Optical Half Subtractor on hexagonal lattice pattern with circle shaped rods is proposed. The Half Subtractor enactment can be upgraded by providing proper distinct space in output power between '0' and '1' logical states and operate well even in the reduced input power level. Errors during the identification of logical states (Logic '0' and Logic '1') can be condensed by establishing a threshold for output power. If the output power level is more than 0.7μW or less than 0.35μW, then it is regarded as logic '1' and logic '0' respectively. Another advantage is found with its contrast ratio which is about 17.24 dB and 25.88 dB for Difference and Borrow respectively. Compactness and ease of design are the characteristics which makes suitable for Photonic Integrated Circuit (PIC) applications.*

Keywords— *All-Optical Half Subtractor, Photonic Crystal (PhC), Electric Field, Polarization.*

I.INTRODUCTION

All-optical logic gates have a high potential for all-optical signal processing such as addressing, optical calculations, pulse retrieval, and signal reproduction. The presence of these gates has led to the rapid growth of ultrafast all-optical telecommunication networks and optical computers, the main constituent of which is photonic crystal (Phc).Photonic crystals (PC) are dielectric material in which the refractive index is periodically varied in space. In PC for some frequency ranges the light waves are not propagating through the structure, such frequency range is called forbidden gap of photons. The doping of impurity or creating defects produce strong localization of a resonant photon. This phenomenon will allow a perfect control of light propagation and radiation. Introducing line defects in PC results in a photonic crystal waveguide. All optic logic gates are key elements in different signal processing techniques.

Recently, photonic crystals (PCs) have received a lot of attention from fundamental and practical points of view. Due to their unique optical properties and their potential use in optical devices, much research has been done on their ability to control light emission. Photonic crystals are periodic dielectric structures with a refractive index in the wavelength scale of light. Considering this rotation, the photonic band gap (PBG) allows the emission of electromagnetic fields in a specific frequency band [1]. Using the defects in photonic crystals, light can be directed in a particular direction and can be used in photonic crystal structures [2]. Some significant applications of defective photonic crystals include ultra-narrow-band filter [1], multiplexer [2], ring resonators [3], filters [4], optical fiber [5], solar cells [6], power divider [7], waveguides [8], etc. The filter is realized by a coupled-resonator waveguide. With the development of optical telecommunication networks, narrow-band optical filters will be required in optical integrated circuits. Works done on this topic include: tunable narrow-band filter using voltage-controlled wavelength selection [8]. In future world, the fabrication of photonic integrated circuits finds a lot of applications in which the optical logic circuits and logic gates acts as the base. Among these logic circuits, not only the gates and adders play a key role in PIC but also other devices play a vital role. In this paper, an all-Optical Half Subtractor is proposed with a good split-up capability to classify logic "0" and logic "1" in output port. The minimum tolerable electric field that can be used as logic "1" is increased in our proposed PhCs based all-optical Half Subtractor which also increases the contrast ratio. In the design of the PhCs based optical logic gates, logic „1" is considered as ON and logic „0" as OFF. The important operation of logic gates is to control the interval variation between the maximum electric field in "0" state, and minimum in "1" state which is defined as the undefined region, thereby the probability of error in sensing logic "1" and logic "0" will be diminished. This gate forms the basis for all upcoming

optical components. The wavelength for the simulation should be in PBG range in order to limit and conduct the light in defect lines. Thus, the 1550 nm wavelength is chosen for simulating the proposed structure.
In the proposed paper, proper waveguide structures have been used in the presence of nonlinear effects in the structure that resulted in a reduction in power consumption and an increase in logic gate resolution. The proposed logical gate switching time is low compared to the above-mentioned articles**.**

I. NUMERICAL MODELING TECHNIQUES

FDTD Method

Several computational methods have been employed for analysis of photonic crystal structure, including plane wave expansion (PWE) method, transfer matrix method, Green's function method and finite difference time domain method. But we have employed the FDTD method based on Yee's algorithm, to study the 2D-PCS, because the computational time and memory requirements are reduced [9-10]. The propagation of electromagnetic waves through photonic crystal structure is governed by Maxwell's four equations in a linear medium with the sources and are

$$\vec{\nabla}\times\vec{E} = -\mu\frac{\partial\vec{H}}{\partial t}$$
$$\vec{\nabla}\times\vec{H} = -\varepsilon\frac{\partial\vec{E}}{\partial t}$$
$$\vec{\nabla}\times\vec{E} = \vec{\nabla}\times\vec{H} = 0 \qquad (1)$$

Using these equations, magnetic field components can be expressed in form of Helmholtz equation, which is given by

$$\frac{\partial}{\partial X}\frac{1}{\varepsilon(x)}\frac{\partial}{\partial x}H(x) + \frac{\omega^2}{c^2}H(x) = 0 \qquad (2)$$

Equations (1) and (2) are discritised so that the E and H fields are solved from the E and H field at a precise time step. The 2-D TE mode FDTD used in this paper is

$$\frac{\partial H_X}{\partial X}\frac{1}{\mu}\left[\frac{\partial E_Z}{\partial y}\right]$$
$$\frac{\partial H_y}{\partial t}\frac{1}{\mu}\left[\frac{\partial E_Z}{\partial x}\right]$$
$$\frac{\partial H_Z}{\partial t}\frac{1}{\varepsilon}\left[\frac{\partial H_y}{\partial x} - \frac{\partial H_x}{\partial y}\right] \qquad (3)$$

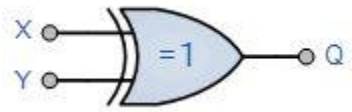
Each filed component is updated from the data at the previous time step. The Gaussian beam is initiated in the grid, travels through, reflects from, refracts in and resonates inside the photonic crystal. Where ε(r), μ (r), σ (r) are permittivity, permeability and conductivity of the material and all are in the function of position. For our simulation,

we have used PML boundary condition. Further time step is so chosen that stability criteria is satisfied and the output power normalization can be calculated as follows.

III. CONVENTIONAL HALF SUBTRACTOR DESIGN

1- input Exclusive-OR Gate

Symbol



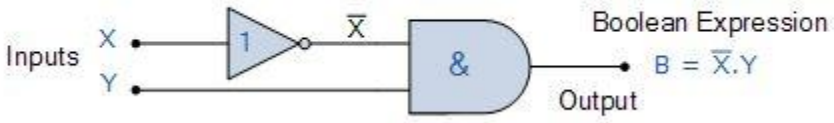
2-input Ex-OR Gate

Truth Table

Y	X	Q
0	0	0
0	1	1
1	0	1
1	1	0

As with the Binary Adder, the difference between the two digits is only a "1" when these two inputs are not equal as given by the Ex-OR expression. However, we need an additional output to produce the borrow bit when input X = 0 and Y = 1. Unfortunately there are no standard logic gates that will produce an output for this particular combination of X and Y inputs.

But we know that an AND Gate produces an output "1" when both of its inputs X and Y are "1" (HIGH) so if we use an inverter or NOT Gate to complement the input X before it is fed to the AND gate, we can produce the required borrow output when X = 0 and Y = 1 as shown below.

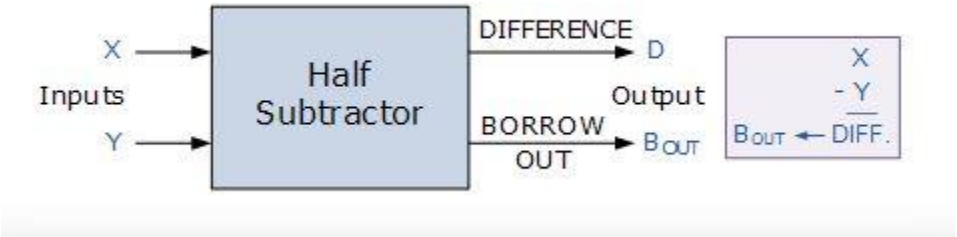


Then by combining the Exclusive-OR gate with the NOT-AND combination results in a simple digital binary subtractor circuit known commonly as the Half Subtractor as shown.

2- A Half Subtractor Circuit

A half subtractor is a logical circuit that performs a subtraction operation on two binary digits. The half subtractor produces a sum and a borrow bit for the next stage.

3- Half Subtractor with Borrow-out



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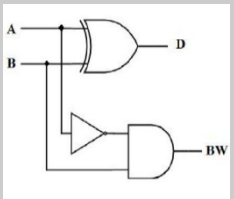


B	A	DIFFERENCE(D)	BORROW()
0	0	0	0
0	1	1	0
1	0	1	1
1	1	0	0

From the truth table of the half subtractor we can see that the DIFFERENCE (D) output is the result of the Exclusive-OR gate and the Borrow-out (Bout) is the result of the NOT-AND combination. Then the Boolean expression for a half subtractor is as follows.

For the DIFFERENCE bit:

D = A XOR B = A ⊕ B

For the BORROW bit

BW = not-A AND B = A.B

If we compare the Boolean expressions of the half subtractor with a half adder, we can see that the two expressions for the SUM (adder) and DIFFERENCE (subtractor) are exactly the same and so they should be because of the Exclusive-OR gate function. The two Boolean expressions for the binary subtractor BORROW is also very similar to that for the adders CARRY. Then all that is needed to convert a half adder to a half subtractor is the inversion of the minuend input A.
One major disadvantage of the *Half Subtractor* circuit when used as a binary subtractor, is that there is no provision for a "Borrow-in" from the previous circuit when subtracting multiple data bits from each other. Then we need to produce what is called a "full binary subtractor" circuit to take into account this borrow-in input from a previous circuit.

IV.SIMULATION AND RESULTS

A.Numerical Analysis Methods:

Analysis of the components with structure-based photonic crystals is done in two ways. 1. Determination of the diagram of a photonic crystal network to specify the logic gateway frequency range performed by the PWM waveform expansion method. 2. Determination of the transmission range and reflection of optical power in the photonic network structure of all-optical logic gates, which is done by the Finite-Difference Time-Domain (FDTD) method. The simulation process of the proposed optical photonic crystal logic gate is performed with Rsoft software. The calculation method of the listed tools is PWE. Transmission curve and reflection of optical power in the logical gate output are simulated using the Rsoft FULLWAVE tool. The calculation method of the above-mentioned tool is FDTD.

B.LAYOUT NARRATION :

The proposed design has 15 x 15 arrays of 2-D PhC silica dielectric rods embedded in air substrate of refractive index (n=1) in hexagonal lattice which analogous to fused coupler with waveguides. In this structure, the defects are created by removing the corresponding PhC dielectric rods in the structure that forms the waveguide. The refractive index of chosen Silica rods is about 3.46 and the dielectric constant „εr" is about 11.56 [21]. The radius „r" of the rods in this work is considered to be 0.18a; where „a" is known as the lattice constant which is the distance between two dielectric rods. In this design, several junction rods and reflection rods are used. The radius for each junction/reflection rods are chosen as 0.08a so that the Half Subtractor can produce the anticipated output and it is noticed that the maximum power is transmitted at the output ports (Difference and Borrow output Port). Figure 1 shows the layout of all-optical half Subtractor design and it is simulated using finite difference time domain (FDTD) method.

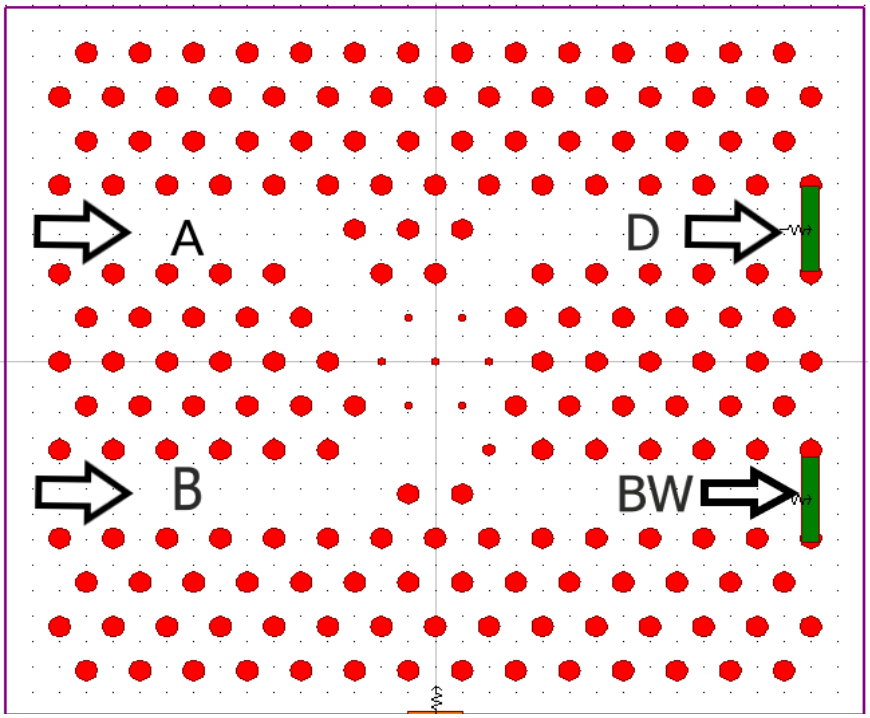


Figure 1: Design for half-Subtractor

C. BANDGAP CONFIGURATION

The Plane Wave Expansion (PWE) method is used for obtaining the band structure Figure 2 shows the normalized band structure for proposed structure. The band structure is obtained for the TE mode. The calculated band structure depicts that the main Photonic Band Gap (PBG) is situated in the range of $a/\lambda = 0.29$ to 0.479, such that the wavelength equivalent of this range is 1.29 to 2.13 μm. Then the selected wavelength sources should be in this PBG range and therefore $\lambda = 1550$ nm is used for this simulation.

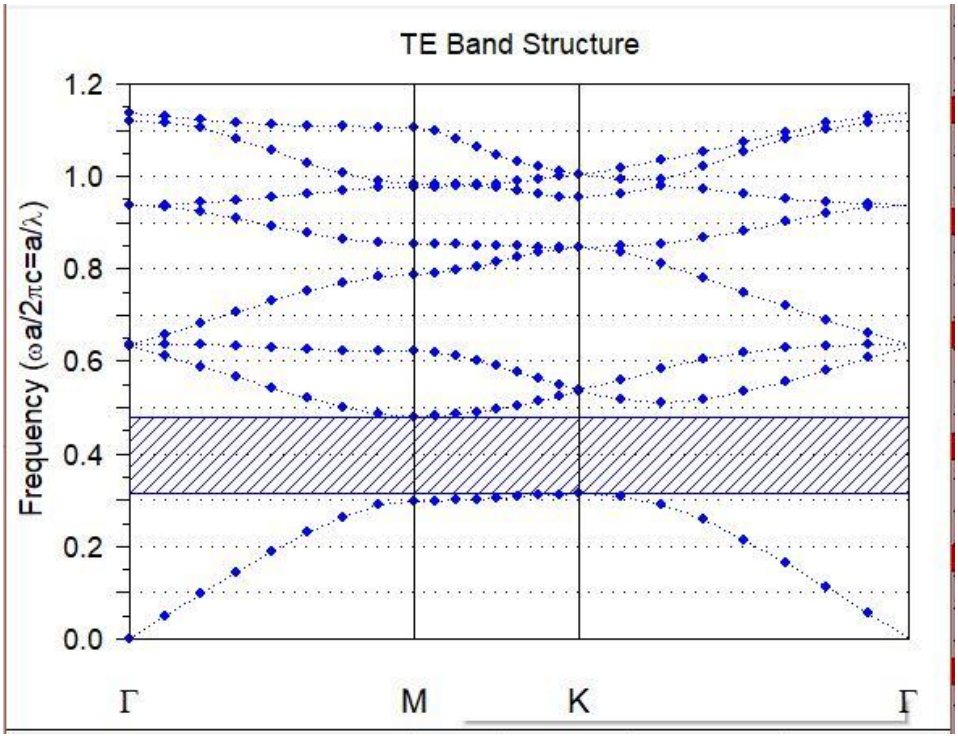


Figure 2: Calculated bandgap for proposed Structure

The refractive index diagram of the proposed crystal photonic structure is depicted in Figure3.

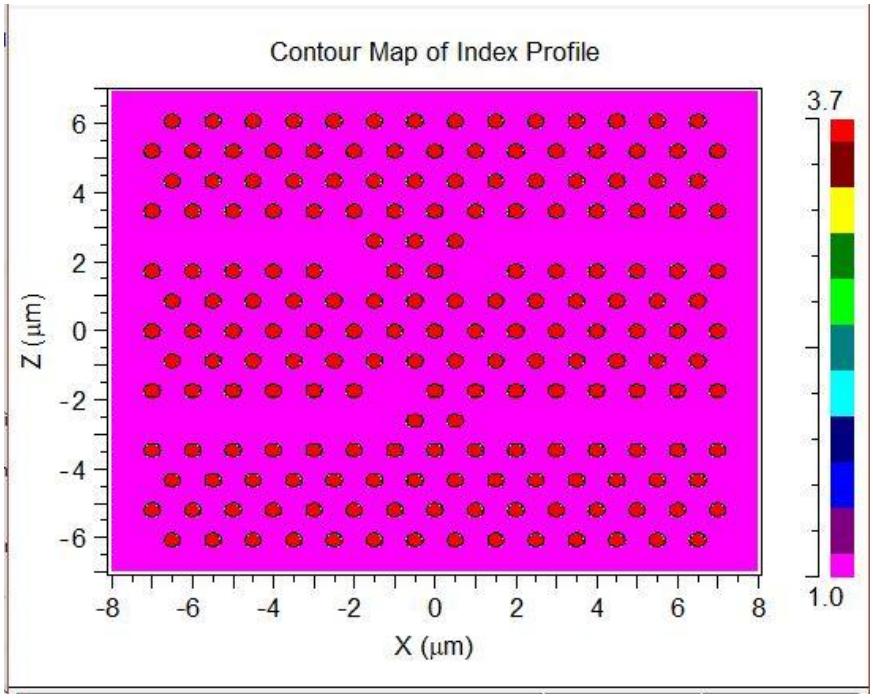
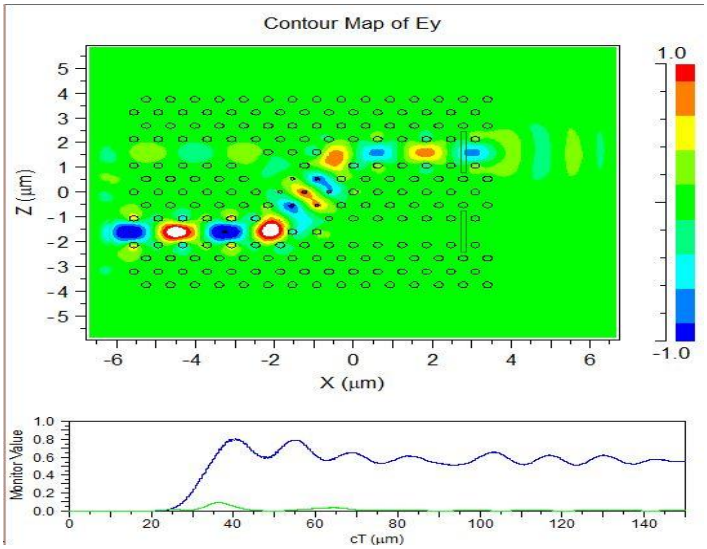


Fig. 3. Graph of the refractive index of the proposed crystal photonic structure

The proposed Optical Half-Subtractor has two inputs (A and B) and two outputs (D and BW), where D is the Difference of two inputs and BW is the Borrow output bit. Two optical sources with 1550 nm wavelength are used as inputs. The defect lines of the inputs and outputs of the proposed half-Subtractor are shown in the layout (Figure 4).The defect lines are selected to intercross each other. The radius of five (blue colored) rods is reduced to 0.5r in their crossing, where r is the radius of base (red colored) rods. These rods act as scatterers which will control and conduct electric field in their output ports.



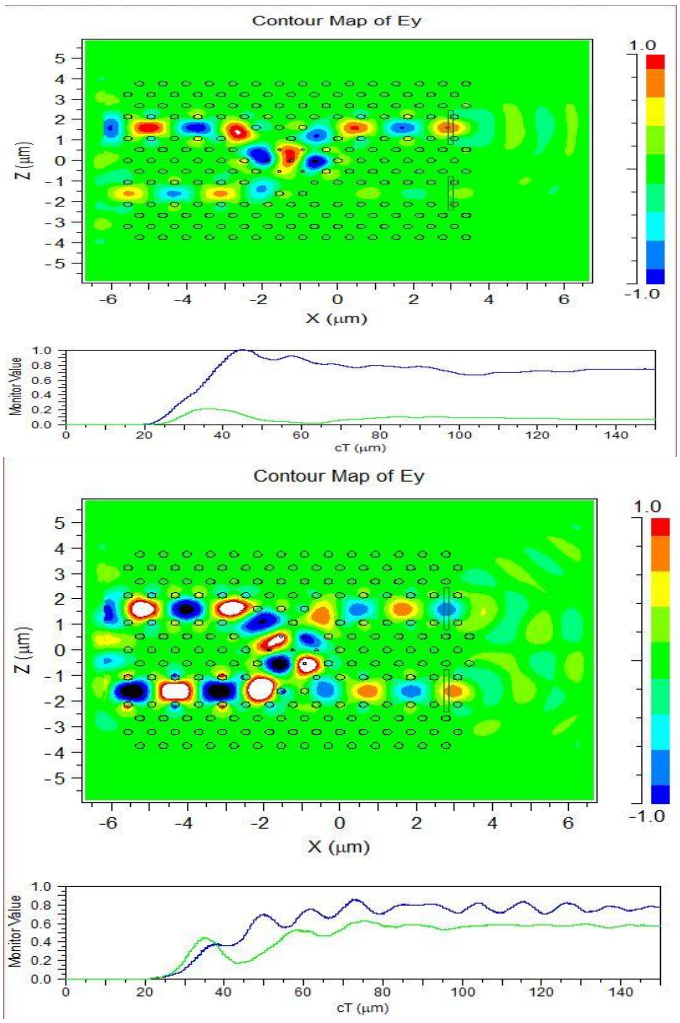


Figure 4: Electric field distribution of inputs a) A = 0, B = 1 b) A = 1, B = 0 c) A = B = 1

When the two input sources are in off state (A = B = 0) there is no possible for electric field distributions in the outputs, then D and BW will be in logic„0" state. For a special case of A = 0 and B = 1, the output is HIGH at both the outputs. When the inputs A = 1, B = 0, the output at D is significant than the BW output. If both of the inputs are HIGH then both of the outputs are LOW. All those cases are clearly shown in Figures 4 (a) (b) and (c). Table 1 presents the results of the proposed structure to verify half-subtractor operations.

Table 1. Input and output values for 1550 nm half-subtractor

Input power=1.0 µW

INPUT				OUTPUT			
A		B		D		BW	
VALUE	LOGIC	VALUE	LOGIC	VALUE	LOGIC	VALUE	LOGIC
0	0	0	0	0	0	0	0
0	0	1	1	0.85	1	0.58	1
1.0	1	0	0	0.82	1	0.1	0
1.0	1	1	1	0.22	0	0.1	0

In this simulation, electric field variations in the bandwidth range C (1530-1610 nm) are shown in Figures 5, 6 and 7. Here, there is a decrease in the path created by reflection and light emission to the unwanted output path and it should be in logic 0 mode.

Due to the fact that the designed subtractor cannot be ideal and any equipment has an ideal error value, the error value must be measured. In photonic crystal structures, due to lack of an ideal refractive index, and problems such as errors in the fixed distance of the grid, and the intervals between the holes, there is always some leakage from the input wave into the structure or the presence of electromagnetic power in undesirable outputs. This amount of leakage power should not exceed the threshold limit defined for the proper functioning of the subtractor. In this part, the amount of power in desirable outputs and the amount of leakage power to unwanted outputs are shown in the figures. The difference between these powers in the wavelengths of the design should be less than the threshold limit defined for proper functioning of the equipment.

In the case that both inputs are zero (A = 0, B = 0), both outputs show zero power, which is ideal and desirable. In the case where A = 1, B = 0, the desirable and ideal value of D output is 1 μm to indicate logic 1 value in this output. However, this power value is ideal, and in practical operation, this power value is less than 1 as shown in the figure below. In addition, the leakage power value to the BW output should be 0 μW, whose value in the normal operation of the equipment is not zero, and its value for the wavelengths of the design is shown in the figure5.

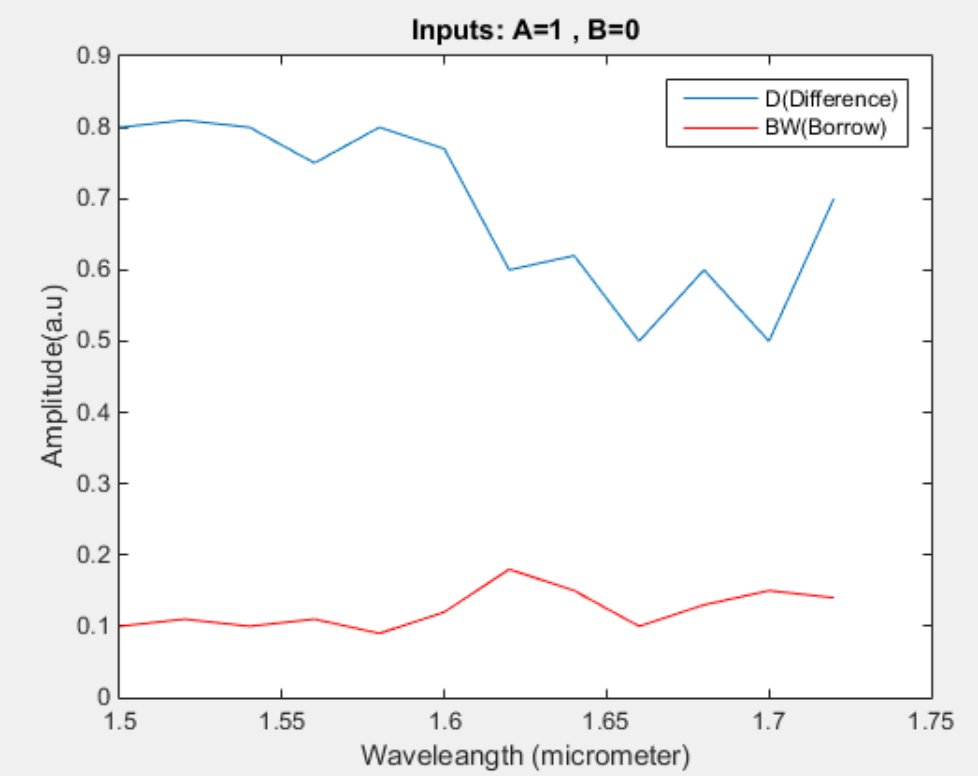


Figure 5: Output graph for various wavelengths with inputs A = 1 and B = 0

As shown in the above figure, the power value in D is closer to 1 and is higher than 0.8 μW, and the power leakage to the BW output at the wavelengths is less than 0.18 μW. The difference between these two values is high enough to easily consider a suitable threshold limit for logic values of 0 and 1. In different modes, the combinations of two inputs and the desirable and undesirable power values in the D and BW outputs are shown in the following figures6

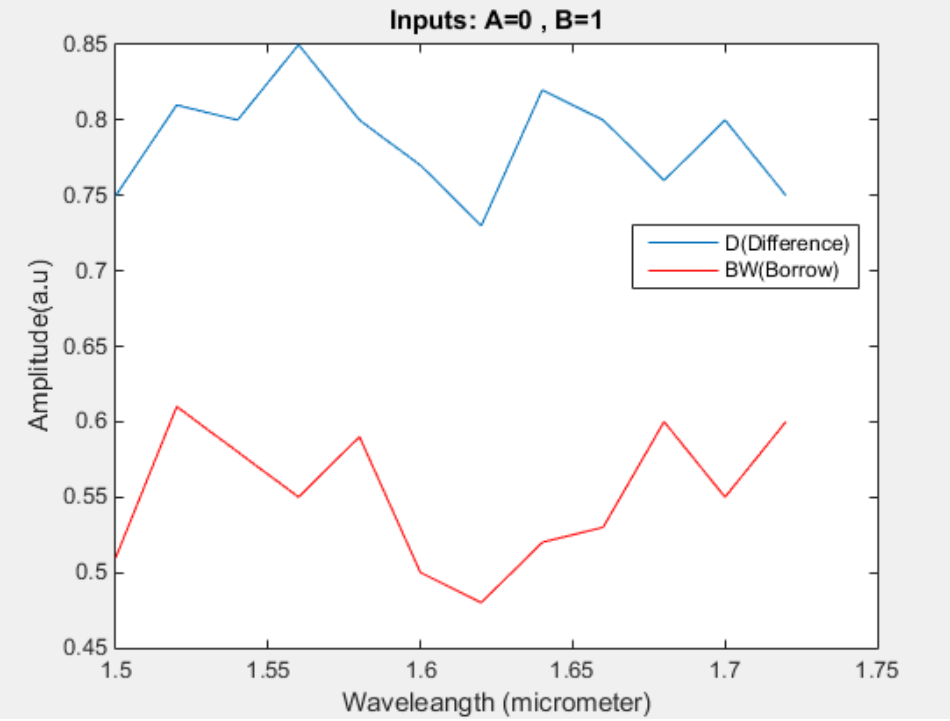


Figure 6: Output graph for various wavelengths with inputs A = 0 and B = 1

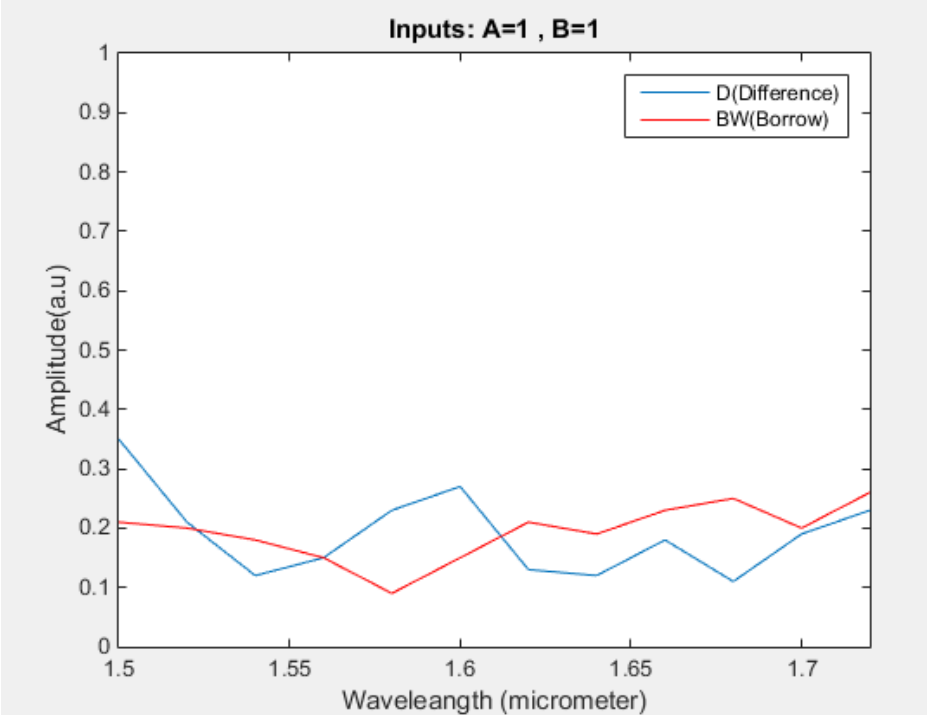


Figure 7: Output graph for various wavelengths with the inputs A=B=1

In the last figure7, both inputs are stimulated to unit power. In this case, both inputs are the logic "1" value, and the difference and the residual subtraction in the correct function require the logic value of 0 on both D and BW outputs. As shown in the figure, the output power of both design wavelengths is less than 0.2 μW, which indicates the proper functioning of the designed gate.

The contrast ratio is defined as the ratio of the ON power to OFF power in single ports and is calculated by using Equation 4.

$$CR = 10 \log PON / POFF \quad (4)$$

Where, PON and POFF are the levels of logic powers "1" and "0", respectively. The contrast ratio is 17.24 dB and 25.88 dB in differential and borrowing outputs, respectively. This improved contrast ratio plays an important role in photonic integrated circuits.

It is obvious that the proposed design has a better contrast ratio than the previous work, and our proposed subtractor provides a specific space in the output power between the logic "0" and "1" modes.

IV. CONCLUSIONS

Photonic crystal is one of the important structures for designing all-optical logic gates. These crystals have the least amount of power loss and have high power transferability in comparison to semiconductors and semiconductor optical amplifiers. All-Optical Half Subtractor based on PhC for the photonic Integrated Circuits are designed and its output is analyzed in terms of Difference and Borrow. The results for all four combinations of inputs of Half-Subtractor are analyzed. For a) A = 0, B = 1, b) A = 1,B = 0 c) A = B = 1 cases, the obtained output power level for Difference is 0.85 µW, 0.8 µW, 0.22 µW respectively and the corresponding Borrow output power is about 0.58 µW, 0.1µW and 0.1 µW. Better distinct output power levels for logic „0" and logic „1" are obtained with less input power of 1 µW. Improved contrast ratio (17.24 dB for Difference and 25.88 dB for Borrow) and ultra-compatibility has also proved that this proposed compact design can be certainly used for photonic integrated circuits.

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