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DESIGN OF LOW VOLTAGE MODIFIED WILSON CURRENT MIRROR CIRCUITS BASED ENERGY EFFICIENT LEVEL SHIFTERS

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Abstract — *Wide range level shifters are easiest energy efficient converters capable of the converting low voltages to their high voltage. Level Shifters are mainly used to the shifting voltage from a one level to other levels. Multi voltage systems utilized the advantages of level shifters. Multi voltage systems consist of low voltage as well as high voltage. Existing methods was implemented by a using the LVT (Low Threshold Voltage Transistor) which produce the leakage power dissipation. Proposed method is implementing by a using forced PMOS methods to reduce the leakage power. Usually Level Shifter is inserted only while crossing the low voltage domain to high voltage domain. In this paper modifies the Wilson current mirror circuits based level shifter is designed by using stack techniques. Measurement results were demonstrated by using cadence Tools.*

Keywords— *Level Shifters, Multi voltage systems, Widlar Wilson Circuits, Forced PMOS technique.*

I. INTRODUCTION

The design of modified Wilson circuits increased in power consumption, the price of packaging additionally will increase. In growing market of mobiles, battery powered electronic systems (e.g., cellular phones, Personal digital assistants, etc.). Demand designs of microelectronics circuits, low power dissipation. More generally, as density size and complexity of the chips continues to increases in the difficult to providing the adequate cooling might either add significant costs or limit the functionality of the computing systems, which makes its use of those integrated circuits. In their past ten years several techniques methodology tools for designing for low power circuits have been presented. However, only a few of them have found then their ways in current design flows [1]. There are three different major sources of power dissipations in a CMOS circuit. There are switching power, short circuit power, and leakage power. Switching power is due to their charging and discharging capacitors, driven by the circuits. Short circuit power is caused by the short circuits current that arise, when pairs of PMOS/NMOS transistors are conducting simultaneously.

Finally the Leakage power is originates from substrates injection and sub threshold effects. One of the major reasons causing the leakage power increases in the X sub threshold leakage power also increases. When technology features size scales down, supply voltage and threshold voltages also scale down. Sub threshold leakage power increase exponentially as threshold voltage decreases. Stack method, Forced NMOS, Forced PMOS and sleepy keeper method are the some of the leakage current reduction methods [2]. When technology feature size scales down, supply voltage and threshold voltage also scale down.

This paper presents a new design method of Level Shifter for wide range operations and bidirectional conversion.

I.LEVEL SHIFTERS

A. *Conventional Level Shifter*

Sub threshold Level Shifters is surveyed in these section. Conventional cross coupled LS is a differential cascade voltage switch logics (DCVSL) for raising a low voltage level, as shown in fig.1. The drive strength of NMOS transistor is enhanced to an overcome the leakage power of weakly conducting PMOS transistor. The operating ranges of CC LSs depend on the transistor threshold voltage (VT) and size; However, the operating range of CC LSs is difficult to extend to the sub threshold region (with respect to the NMOS v_t) because the NMOS drive strength decreases exponentially. This is often achieved by semiconductor unit size, i.e., creating the NMOS transistors sufficiently wide. However, the large width of NMOS transistors does not make it suitable for sub-threshold to above-threshold level shifting. For converting a sub threshold voltage, CC LS require an exponential increase in NMOS transistor size, which is impractical [3].

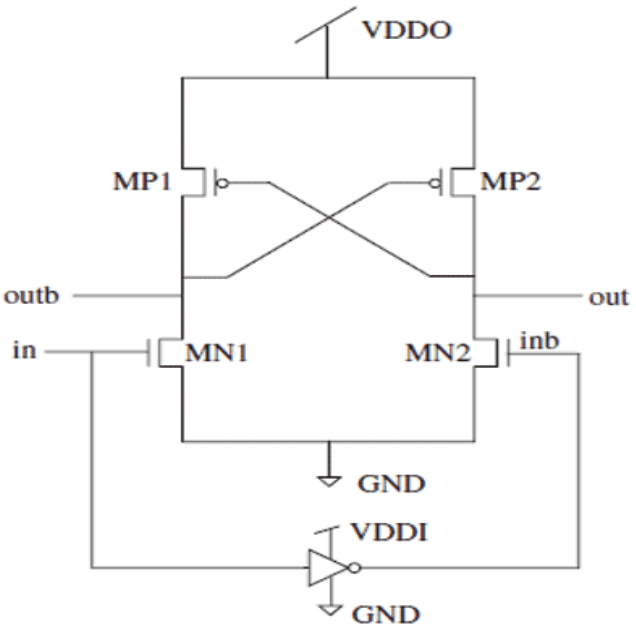

Fig.1Conventional Level Shifter

B. *Current Mirror based Level Shifter*

Fig.2 shows the conventional Level Shifter that use a basic current mirror (CM). The conventional Current Mirror Level Shifter can convert a deep sub threshold level because a high drain to source voltages of PMOS transistors facilitates the constructions of a stable current mirror, which offers an effective ON - OFF current comparison at the output node. However, a high amount of Quiescent current occurs, when the input voltage is super threshold. The current mirror level shifter can converts to a deep sub threshold level to above threshold because a high drain – to - source voltages of PMOS transistors facilitates the constructions of a stable current mirror, which offers an effective ON - OFF current comparison at the output node. This high power consumption limits to the use of the conventional Current Mirror Level Shifter [4].

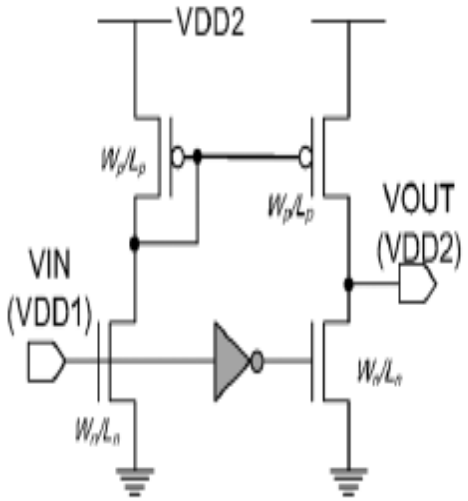

Fig.2. Current Mirror Based Level Shifter

C. *Wilson Current Mirror Based Level Shifter*

Fig.3 shows a CM type LS that used a Wilson current mirror (WCM), which clamps to the quiescent power consumptions under a super threshold input [4].

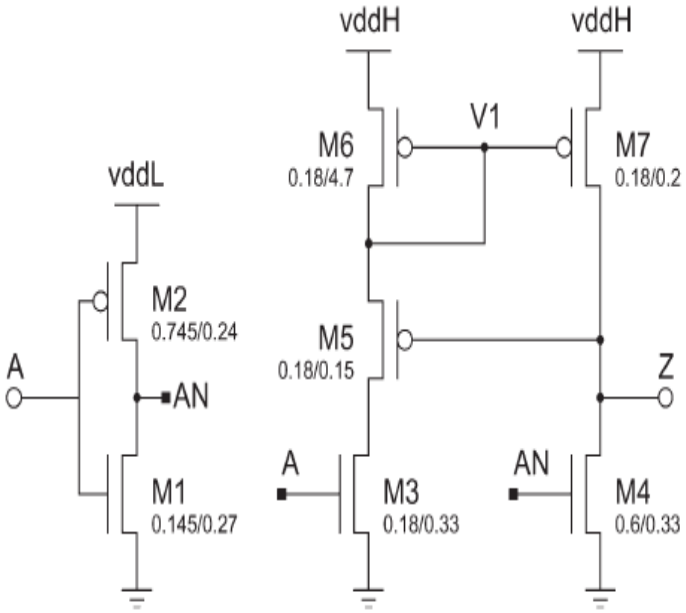

Fig.3. Wilson Current Mirror based level shifter

In a two stage Current Mirror Level Shifter of which the pull up driving strength is reduced by the header NMOS, which expands to the convertible input voltage. In a CC-type LS (CCPNR), in which the output stage is a part of the NOR gate fed by the primary input to accelerate the overall LS speed. I n uses a logic Error Correction Circuit (LECC), which monitors input and output updates data during the pulse. The MWCMHB LS is a hybrid structure comprising a modified Wilson current mirror and CMOS logic gates. The input and output levels range from a sub threshold voltage to the standard supply voltage defined in a transistor technology. Bidirectional level conversion is available; that is, input and output levels can be scaled independently.

*D. **Modified Wilson Current Mirror Based Level Shifter***

The MWCMHB LS structure is illustrated with three circuit blocks, as shown in Figure .4. A modified Wilson current mirror (MWCM) is located in Block 1. When VDD1 is sub threshold and VDD2 is high, the MWCM structure balances the rising and falling delay at Node A, without losing the original static bias that is favored in the WCM LS. However, when the VDD1 and VDD2 levels are close, the MWCM encounters the same problem as the WCM does. The cascode PMOS has insufficient drive currents and increases the rising delay. A modified Wilson current mirror (MWCM) is located in Block 1. When VDD1 is sub threshold and VDD2 is high, the MWCM structure balances the rising and falling delay at Node A, without losing the original static bias that is favored in the WCM LS. Therefore, in Block 3, a delay path is designed adaptively to reduce the rising delay and maintain a moderate duty cycle. An output inverter offers sufficient drive strength, which is required in a standard cell design. Unlike the CCPNR LS, which has a similar structure, the proposed LS uses a CM-type amplifier, a balancing delay path, and a complementary OR gate in Block 2.The CM type structure provides a wide operating range, and the stacked PMOS transistor in the complementary OR gate limit the leakage current.

Level shifter should satisfies the following condition those are

1. Small area for sub threshold level conversion
2. Low power consumption in super threshold Operations
3. Balancing rising and falling delay in the operating Range
4. Bidirectional level conversion

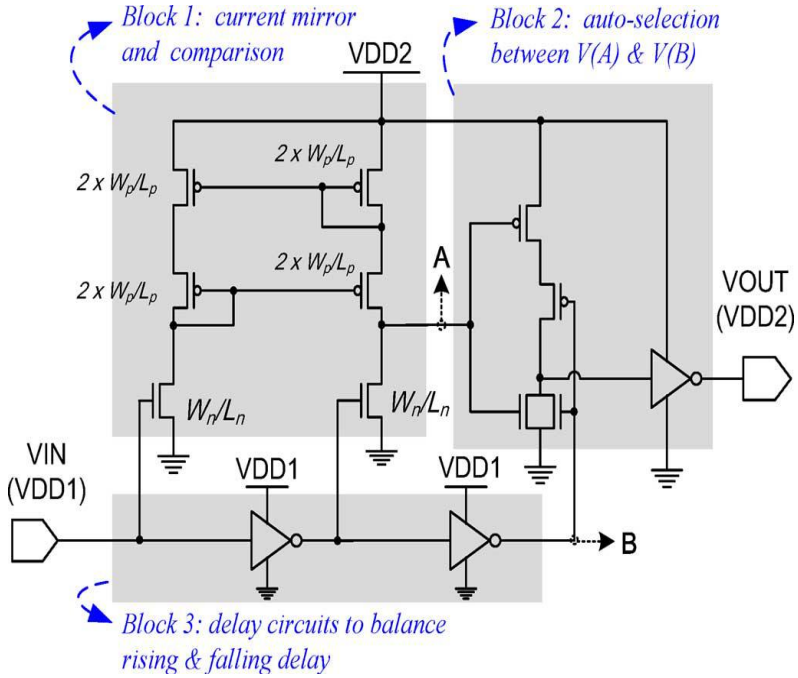

Fig.4. Modified Wison Current Mirror based Level Shifter

II.POWER REDUCTION METHOD

Forced PMOS is one of the methods of leakage power reduction Technique. In this method pull down network is not modified. Pull up network is only modified by the Forced PMOS method. An Existing PMOS Transistor is split into two each transistor is having the W/L ratio of half compare with existing transistor. Consider inverter as an example. By applying this Forced PMOS method to the inverter the power can be decreased from 2 pW to 1.75 pW. In this method two PMOS transistor increases the delay in the current flow path so that power can be increased. Other leakage power reduction methods are stack method and forced NMOS method.

Stack approach is one of the leakage power reduction methods, which forces a stack effect by breaking down an existing transistor into two half size transistors. When the two transistors are turned off together, induced reverse bias between the two transistors results in leakage current reduction. However, divided transistors increase delay significantly and could limit the usefulness of the approach.

In forced NMOS approach if input is given low as compared to threshold voltage., then at the same time PMOS turns on and NMOS turns off and if input is given high at the gate terminal as compared to threshold voltage, then at the same time PMOS turns off and NMOS turn on. Here, the two NMOS transistors which increase the delay in the flow of the current which ultimately decreases the leakage power in the circuit.

III. PROPOSED LEVEL SHIFTERS

In this section Existing Level shifters are modified by using the Forced NMOS approach. Figure 5,6,7,8 shows the conventional cross coupled, Current mirror based level shifter, Wilson current mirror based level shifter and modified Wilson current mirror based level shifter. These level shifters were designed by using the Forced PMOS method. Power was reduced when comparing with existing level shifters. In that planned interface circuit, P1is isolated from the input to reduce each the static power consumption and propagation delay. because the pull-up and pull-down networks are near at the same time on, the planned voltage interface circuit consumes no static power whereas driving high electrical phenomenon hundreds full swing (Vdd2) at high speed. In this circuit, solely I1 is provided by Vdd1.The rest of the circuit (to the correct of the demarcation line) is provided by Vdd2. This circuit operates within the following manner with a zero to 1transition at the input, node2is discharged through N1.P2 ensures that P1 is cut-off, and I2 ensures that P3 is cut-off throughout the output transition, so the tangency power consumption and output transition time are decreased.

In forced PMOS method pull up network is only modified. Here existing PMOS transistor W/L ratio is 0.5u/0.3u proposed circuit was designed by splitting the existing PMOS transistor into two each having the W/L ratio of 0.42u/0.5u.

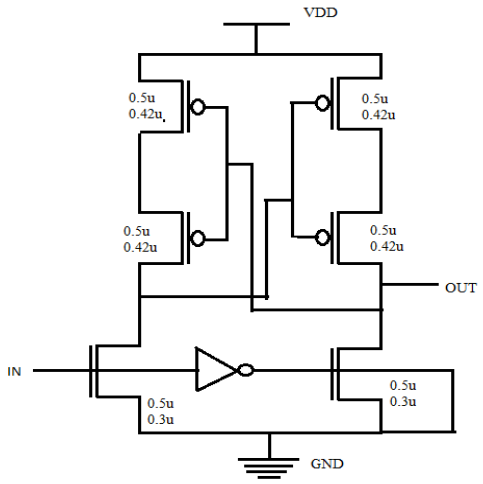

Fig.5. Modified Conventional cross coupled level shifter

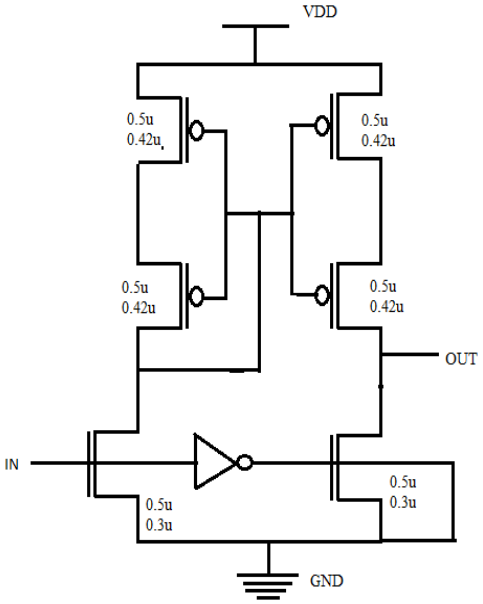

Fig.6. Current mirror based level shifter using Forced PMOS

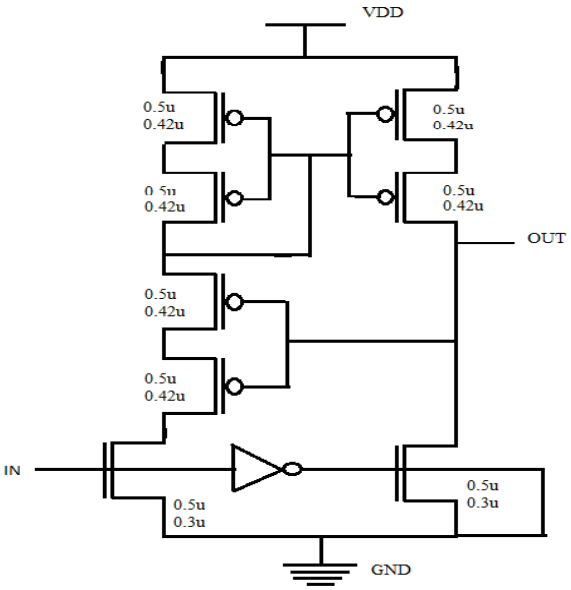

Fig.7. Wilson Current Mirror based level shifter using Forced PMOS

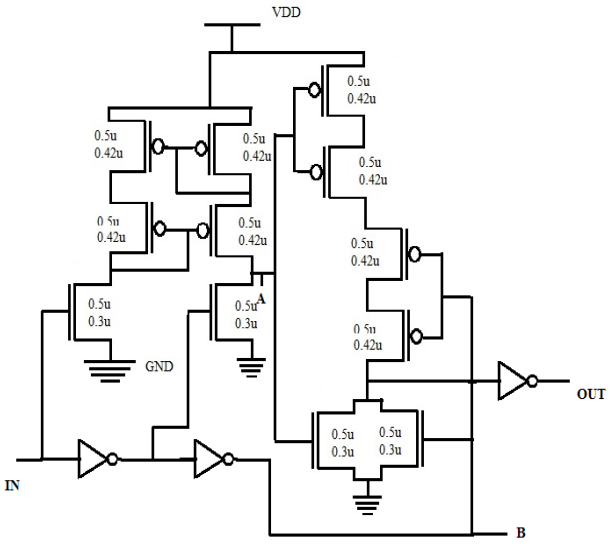

Fig.8. MWCM based level shifter using Forced PMOS

V.SIMULTION AND RESULT

Simulation results for Proposed Level shifters are shown in Figure 9,10,11,12 respectively. Waveform for Modified Conventional cross coupled level shifter is shown below diagram. Input voltage for cross coupled voltage is 2.5v and output voltage is 0.22v. Current mirror based level shifter is also shift the voltage from 2.5v to 0.22v.

Wilson current mirror based level shifter is used to shift the voltage from 2.5v to 0.13v.Modified Wilson current mirror based level shifter is a bidirectional level shifter which is used to shift the voltage from 1v to 5v.Waveform for MWCM is shown in Figure 12.

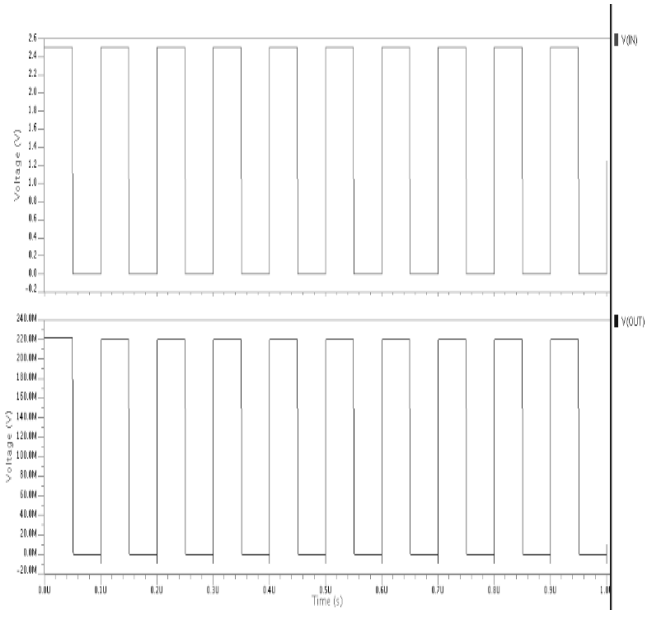

Fig.9. Waveform for conventional level shifter

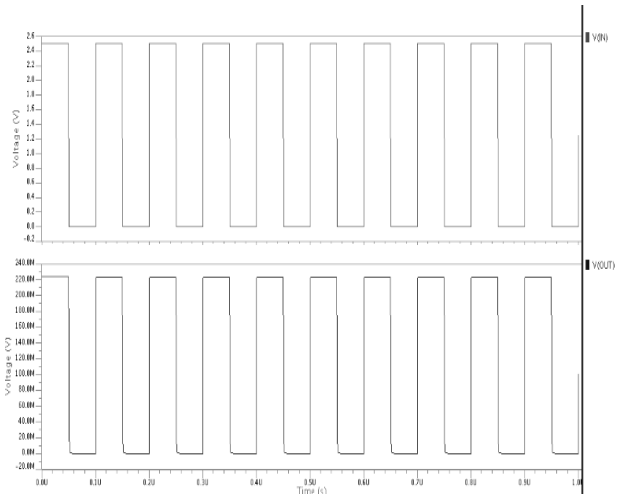

Fig.10. Waveform for current mirror based level shifter

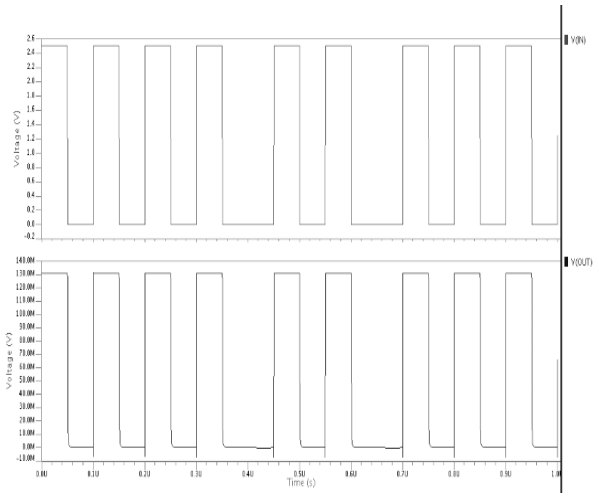

Fig.11. Waveform for Wilson current mirror based level shifter

Simulation can be performed by using the Mentor Graphics. Mentor Graphics is one of the Electron Device Automation tool.

In this tool Eldo, Calibre are mainly used for the simulation, LVS and DVS check. This Software is run at the LINUX operating system.

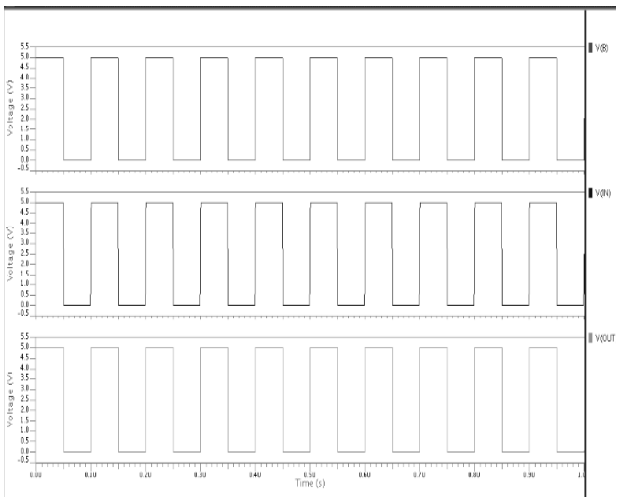

Fig.12. MWCM based level shifter

TABLE I. POWER AND DELAY FOR VARIOUS LEVEL SHIFTER WITHOUT FORCED PMOS METHOD

Level Shifting Technique	Output Voltage	Power (nW)	Delay (nS)	PDP (10^{-15})
CC	1.2V	1068.43	56.67	60.54
	1V	625.42	56.55	35.36
	0.8V	510.55	55.44	28.30
	0.6V	168.25	57.58	9.68
CM	1.2V	202.52	52.25	10.58
	1V	131.85	52.22	6.88
	0.8V	98.96	53.31	5.27
	0.6V	84.25	53.30	4.49
WCM	1.2V	94.40	52.14	4.92
	1V	85.11	51.65	4.39
	0.8V	79.37	50.79	4.03
	0.6V	72.42	50.23	3.63
TSCC	1.2V	263.78	54.67	14.42
	1V	223.93	54.13	12.12
	0.8V	182.95	53.54	9.75
	0.6V	98.45	55.87	5.50
CCPNR	1.2V	254.67	49.64	12.64
	1V	195.52	48.76	9.53
	0.8V	155.87	46.31	7.21
	0.6V	98.67	45.34	4.47
LECC	1.2V	91.65	48.65	4.45
	1V	82.04	46.87	3.64
	0.8V	73.85	44.46	3.28
	0.6V	57.09	40.98	2.33
MWCMHB	1.2V	70.36	39.56	2.78
	1V	51.76	37.34	1.93
	0.8V	45.89	36.25	1.66
	0.6V	41.09	32.49	1.33
PROPOSED	1.2V	51.23	29.76	1.52
	1V	46.54	28.38	1.32
	0.8V	38.63	26.54	1.29
	0.6V	32.58	24.79	0.80

Table. II. POWER AND DELAY FOR VARIOUS LEVEL SHIFTERS WITH FORCED PMOS METHOD

Level shifters	Power	Delay
Conventional Level Shifter	1.8021(mW)	0.3 ns
Current mirror based level shifter	1.7876(mW)	0.5ns
Wilson current mirror based level shifter	1.0391(mW)	0.2ns
Modified Wilson current mirror based level shifter	250.0337(nW)	0.5ns

Table I and II shows the comparison of Normal level shifter design and level shifter design using Forced PMOS method. Comparing with existing and proposed method delay is slightly increased and power is decreased in proposed method.

VI .CONCLUSION

Conventional level shifter has the power dissipation of 4.6943 mW. The same circuit is designed by using Forced PMOS method means that time power is decreased from 4.6943mW to 1.8021mW.Likewise Current mirror based level shifter, Wilson current mirror based level shifter, Modified Wilson current mirror based level shifter is reduce the power consumption from 4.3694mW,1.7154mW and 250.7207nW to 1.7876mW,1.0391mW and 250.0347nW.

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