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# A Novel Topology of a Double-Frequency Buck Converter

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**Abstract:** *Improving the efficiency and dynamics of power converters is a concerned tradeoff in power electronics. The increase of switching frequency can improve the dynamics of power converters, but the efficiency may be degraded. A double-frequency (DF) buck converter is proposed to address this concern. This converter is comprised of two buck cells: one works at high frequency, and another works at low frequency. It operates in a way that current in the high-frequency switch is diverted through the low-frequency switch. Thus, the converter can operate at very high frequency without adding extra control circuits. Moreover, the switching loss of the converter remains small. The proposed converter exhibits improved steady state and transient responses with low switching loss. An ac small-signal model of the DF buck converter is also given to show that the dynamics of output voltage depends only on the high-frequency buck cell parameters, and is independent of the low-frequency buck cell parameters. Simulation and experimental results demonstrate that the proposed converter greatly improves the efficiency and exhibits nearly the same dynamics as the conventional high-frequency buck converter. Furthermore, the proposed topology can be extended to other dc–dc converters by the DF switch-inductor three-terminal net-work structure.*

***Keywords***-AC small-signal model, buck converter, efficiency, power conversion, switch inductor network.

## I. INTRODUCTION

The demand of high-performance power converter is increased dramatically with the broadening of power converter's application fields. In order to improve the transient and steady state performance of power converters and to enhance power density, high switching frequency is an effective method. However, switching frequency rise causes higher switching losses and greater electromagnetic interference. This, in turn, limits the increase of switching frequency and hinders the improvement of system performance. Active and passive soft-switching techniques have been introduced to reduce switching losses. While these can create more favourable switching trajectories for active power devices, they will generally increase the complexity of control and some-times are affected by the variable input and output condition

However, parallel operation has interaction problem that causes circulating current. To avoid the circulating current,. approaches such as isolation, high impedance, and one-converter approach are utilized. These efforts increase the control complexity. The interleaving operation employs *N* converters to operate in parallel with interleaved clocks, so the total dynamics can reach higher performance due to the fact that the equivalent frequency is *N* times the single converter frequency. Nevertheless, the circulating current phenomenon also exists.

A single-phase boost-type zero-voltage-transition (ZVT) pulse width-modulated converter proposed in adopts an additional shunt resonant network to form an additional Boost cell to realize soft switching of the main switches. However, the auxiliary switches operate in hard switch and high frequency. A similar topology of single-phase rectifier is given in, where total harmonic distortion of the input line current is reduced and the efficiency improved. Its operation is different from the ZVT circuit. The boost-type topology, however, is not very effective to enhance the output voltage performance in that the capacitor ripple voltage is determined by the low frequency. Hence, this topology is not suitable for improvement of dc output transient and steady state performances. Moreover, the main Boost circuit and the added cell are coupled, and the added Boost cell has an effect on the inductor current input. Splitting the filter inductor of buck converter into two parts with added auxiliary active switch and diode has been proposed to improve the output voltage response at load current step-down transient situation, but not at load current step-up transient situation. Additional transformer and switches are needed to realize the improvement at step-up transient. To make the circuits in and function as designed, it is required to detect the load transient event, then to trigger or shut down the auxiliary switch. This increases the complexity of the control circuit. Moreover, oscillations at the output voltage occur due to the frequent on and off operations at each transient event. On the other hand, high-frequency switching converter or linear power supply in parallel with low-frequency converter proposed in and enhances the output voltage response. Paralleling high-frequency converter approach also requires the load transient information, while linear power supply method suffers from low efficiency. Moreover, the parallel structure brings about the circulating current problem. Additional current sharing control is needed to overcome this problem.

 

## II. PROPOSED DF BUCK CONVERTER

The topology of a conventional buck converter is shown in Fig. 1.

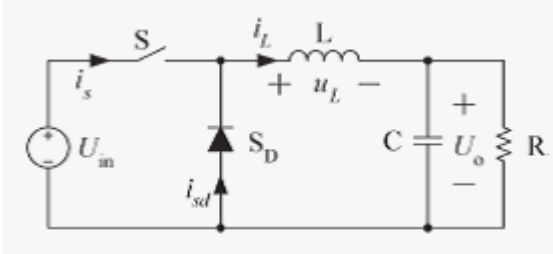


Fig 1. Schematic of buck converter.

In the steady state, the input ($U_{in}$) and the output ($U_o$) of the converter are governed by

$$U_o = D \cdot U_{in}$$

Where D is the duty ratio. If the buck converter works in the continuous conduction mode, then the inductor current $i_L$ can be regarded as a current source. In each switching cycle, both the current flowing through the switch and the voltage across the diode is averaged.

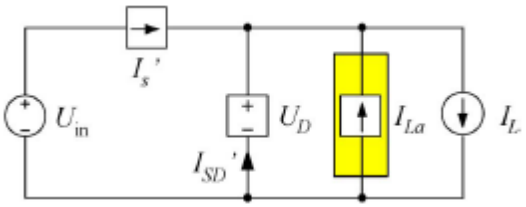


Fig 2. Average model of buck converter with the added CCS

The average model of buck converter is shown in Fig 2, excluding the added CCS $I_{La}$, and its governing equations are

$$I_S = D \cdot I_L$$

$$U_D = D \cdot U_{in}$$

$$I_D = (1 - D) \cdot I_L.$$

To enhance the steady-state response and the transient response of the buck converter, the switching frequency should be increased; but higher switching frequency steps up the switching loss dramatically. A CCS, which is in parallel with the load terminal, is added to tackle this loss problem. Fig 2. shows such modification. The load current through the active switch is diverted by the CCS. The currents through the active switch and the diode can be expressed as

$$I_S' = D \cdot (I_L - I_{La})$$

$$I_D' = (1 - D) \cdot (I_L - I_{La}).$$

It can be seen that when the load current and the CCS are the same, both the currents through the active switch and the diode are nearly zero. In this paper, we propose to use a buck cell working at lower frequency to realize the CCS. The proposed converter is called the DF buck converter; because these buck cells work at two different frequencies. Schematic of this DF buck converter is shown in Fig 3.

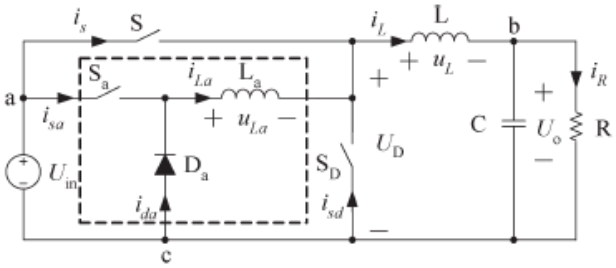


Fig 3: Schematic of the proposed DF buck converter.

The cell containing L, S, and $S_D$ works at higher frequency, and is called the high-frequency buck cell. Another cell containing $L_a$, $S_a$, and $D_a$ works at lower frequency, and is called the low-frequency buck cell.

The high frequency buck cell is used to enhance the output performance, and the low-frequency buck cell to improve the converter efficiency. An active switch, instead of a diode as in the conventional unidirectional buck converter, is employed to realize $S_D$ in the high-frequency buck cell. This active switch transfers the energy stored in the low-frequency cell to the source during the transient stage of load step-down.

It works complementarily with high-frequency cell switch S, and improves the transient response. The switch S is controlled to operate at the high frequency $f_h$, and the corresponding switching period is $T_{sh}$. On the other hand, the

switch Sa is controlled to work at a low frequency fl, and the corresponding switching period is $T_{sl}$. Assume that the high frequency is an integer multiples of the low frequency, i.e.,

$$f_h = M f_l.$$

At each low-frequency cycle, four switching states exist. Table1 lists the switching states according to the status of switches S and $S_a$.

| State | Active Switches | |
|---|---|---|
| | $S$ | $S_a$ |
| $a$ | ON | ON |
| $b$ | OFF | ON |
| $c$ | ON | OFF |
| $d$ | OFF | OFF |

TABLE1: Switching States

The state a denotes that both switches S and $S_a$ are on. The equivalent circuit is shown in Fig 4(a).

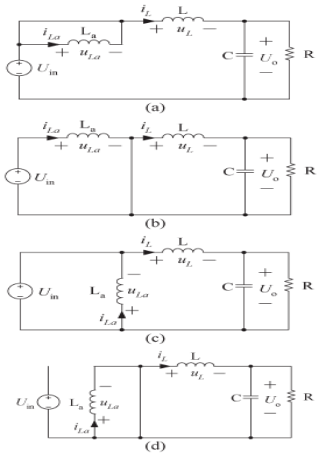


Fig .4: Equivalent circuits of DF buck converter in different switching states (a) State a. (b) State b. (c) State c. (d) State d.

In a similar manner, the equivalent circuits of states b, c, and d are shown in Fig 5.4 (b)–(d), respectively.

The governing equations of state a are expressed as

$$\begin{aligned} u_{\mathrm{L}} &= U_{\mathrm{in}} - U_{\mathrm{o}} \\ \frac{di_{\mathrm{L}}}{dt} &= \frac{u_{\mathrm{L}}}{L_{\mathrm{a}}} = \frac{U_{\mathrm{in}} - U_{\mathrm{o}}}{L_{\mathrm{a}}} \\ u_{\mathrm{La}} &= 0 \\ \frac{di_{\mathrm{La}}}{dt} &= \frac{u_{\mathrm{La}}}{L_{\mathrm{a}}} = 0. \end{aligned}$$

In this state, the voltage uL across the inductor L is positive, and the voltage uLa across La is zero. Hence, the current iL flowing through L rises, and the current iLa flowing through La does not change.

The governing equations of state b can be described by

$$\begin{aligned} u_{\mathrm{L}} &= -U_{\mathrm{o}} \\ \frac{di_{\mathrm{L}}}{dt} &= \frac{u_{\mathrm{L}}}{L} = \frac{-U_{\mathrm{o}}}{L} \\ u_{\mathrm{La}} &= U_{\mathrm{in}} \\ \frac{di_{\mathrm{La}}}{dt} &= \frac{u_{\mathrm{La}}}{L_{\mathrm{a}}} = \frac{U_{\mathrm{in}}}{L_{\mathrm{a}}}. \end{aligned}$$

At this state, the voltage uL across L is negative, so the current iL decreases. The voltage uLa across La is positive, and the current iLa flowing through La rises.

In state c, the equivalent circuit equations are derived as

$$\begin{aligned} u_{\mathrm{L}} &= U_{\mathrm{in}} - U_{\mathrm{o}} \\ \frac{di_{\mathrm{L}}}{dt} &= \frac{u_{\mathrm{L}}}{L} = \frac{U_{\mathrm{in}} - U_{\mathrm{o}}}{L} \\ u_{\mathrm{La}} &= -U_{\mathrm{in}} \\ \frac{di_{\mathrm{La}}}{dt} &= \frac{u_{\mathrm{La}}}{L_{\mathrm{a}}} = -\frac{U_{\mathrm{in}}}{L_{\mathrm{a}}}. \end{aligned}$$

The voltage $u_L$ across L is positive, so the current $i_L$ rises. Since the voltage $u_{La}$ across La is negative, the current $i_{La}$ through La decreases.

 

Finally, the equations of state d are

$$u_{\mathrm{L}} = -U_{\mathrm{o}}$$
$$\frac{di_{\mathrm{L}}}{dt} = \frac{u_{\mathrm{L}}}{L} = \frac{-U_{\mathrm{o}}}{L}$$
$$u_{\mathrm{La}} = 0$$
$$\frac{di_{\mathrm{La}}}{dt} = \frac{u_{\mathrm{La}}}{L_{\mathrm{a}}} = 0.$$

The voltage $u_L$ across L is negative, so the current $i_L$ flowing through L decreases. The voltage $u_{La}$ across La is zero, and the current $i_{La}$ flowing through La remains the same. From equivalent circuits, we find that the low-frequency buck cell does not affect the output inductor voltage, which has the same waveform and value as that of the conventional buck converter. That is, the voltage across the output inductor is $U_{in} - U_o$ when the switch is on, and is $-U_o$ when the switch is off. The voltage and current waveforms of DF buck in one low frequency cycle $T_{sl}$ are shown in Fig 5.5, where M = 4.

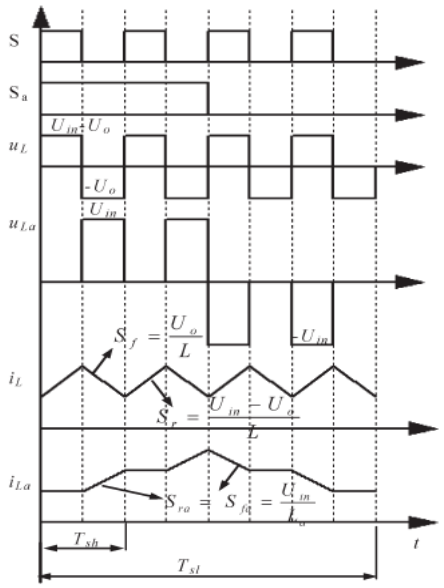


Fig 5: Voltage and current waveforms in one switching period $T_{sl}$.

In the conduction mode of low-frequency switch, the voltage across the low-frequency inductor La alternates between zero and $U_{in}$. Thus, the equivalent slope of the current $i_{La}$ is positive. At the switch-off interval, $U_{La}$ varies from zero to $-U_{in}$, the equivalent slope of $i_{La}$ becomes negative. As a result, if we employ proper control method, the low-frequency inductor can be controlled to follow the output inductor current.

## III. PERFORMANCE EVALUATION

The CPM control circuit used to control the proposed DF buck converter is shown in Fig 6.

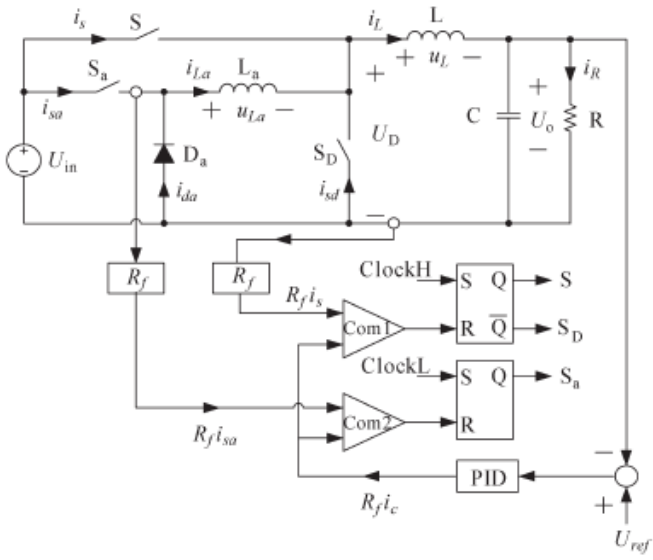


Fig 6: CPM control diagram.

In the control diagram, the output voltage is fed back and compared with $U_{ref}$. The quantity $R_f \cdot I_C$ is used as the current reference for the buck cells. The currents flowing through inductors L and La are expected to be equal to this reference value in the steady state. The low-frequency buck cell diverts the current flowing through high-frequency switches S and $S_D$.

This control circuit, like standard current mode control, does not need additional load transient information, which is not the case in other methods. Since no specific control circuit is required, complexity of the control circuitry of the DF buck converter is similar to that of the conventional buck converter. The implementation is simple and can be done by commercial CPM chips.

**A. STEADY-STATE PERFORMANCE**

Performance of the DF buck converter is evaluated by looking at the steady-state and transient responses of three circuits: a DF buck, a single high-frequency buck converter whose switching frequency is the same as the higher frequency of DF buck, and a single low-frequency buck converter whose switching frequency is equal to the lower frequency of DF buck. Parameters used in the simulation are

$U_{in}$ = 48 V, $U_o$ = 10 V, C= 470 μF

DF buck: L = 100 μH, La = 1 mH, fl = 10 kHz, fh = 100 kHz

High-frequency buck: L = 100 μH, f= 100 kHz

Low-frequency buck: La = 1 mH, f= 10 kHz.

The output voltage waveforms of various buck converters are shown in Fig 7. It can be seen that the steady state performance of DF buck and that of single high-frequency buck converter are almost the same.

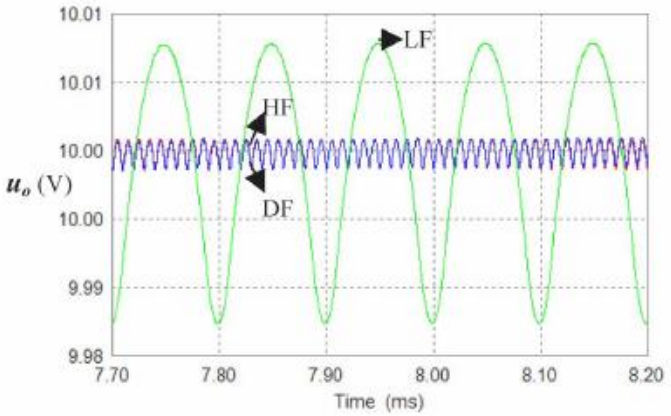


Fig 7: Output voltage waveform comparison in the steady state.

**B. TRANSIENT PERFORMANCE ANALYSIS**

This section investigates the transient response of the DF buck converter. If the load resistance is reduced from 2R to R, the load current will increase from 0.5 IR to IR. Since the currents through inductor L and La cannot change abruptly, at this transient instant, the output voltage decreases due to the increased load current that is partially supplied by the output capacitor. The feedback control loop regulates the duty ratio of each buck cell to control the current of inductor L, iL, and the current of La, iLa. It increases the duty ratio of the high frequency switch so that iL rises. Then, iLa rises too. Note that the low-frequency inductance is selected to be larger than the high-frequency one to reduce the current ripple of $i_{La}$. If the inductor has larger inductance, the current flowing through it will have lower dynamic response speed with the same voltage excitation. As shown in Fig., when low-frequency switch is on, the average voltage applied to low-frequency inductor is 1 − d times the input voltage $U_{in}$. This is the same as the voltage across the high-frequency inductor, $U_{in} - U_o$, when high-frequency switch is on. On the other hand, when the low-frequency switch is off, the average voltage across low frequency inductor is −d times $U_{in}$. This average voltage is also the same as that across the high-frequency inductor when high-frequency switch is off. Hence, $i_{La}$ rises slower than $i_L$. Moreover, the current through the high-frequency switch increases momentarily, but soon back to the steady state level due to the current feedback loop.

If the load resistance is increased from R to 2R, then the load current will decrease from IR to 0.5 IR, so is the low-frequency inductor current $i_{La}$. At this moment, $i_{La}$ can freewheel through SD when the switch S is off. When S is on, the energy stored in La can be fed back to the source via the switch S. As a result, the impact to output response by the low-frequency inductor is largely alleviated. Figure shows the output voltage waveforms of three different buck converters when the load changes. Fig 8(a) is for the load change from 2 to 4 Ω, and Fig 5.8 (b) is for the load change from 4 to 2 Ω.

 

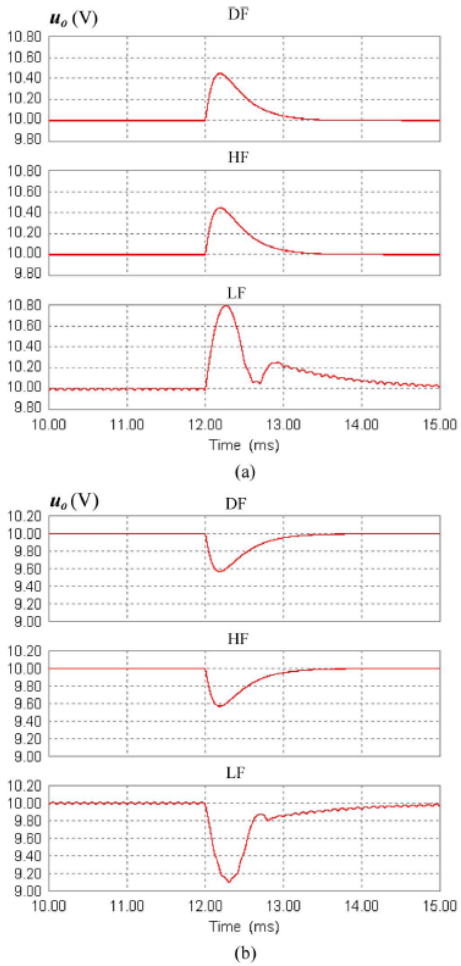


Fig 8: Output voltage transient response comparison (a) Load step-up. (b) Load step-down.

It is observed that the DF buck and the single high-frequency buck converters exhibit almost the same transient responses during load changing, and much better than the single low-frequency buck converter does. The effect of switch current diversion of the high-frequency cell and the low-frequency cell is also investigated. The current waveforms are shown in Fig 9.

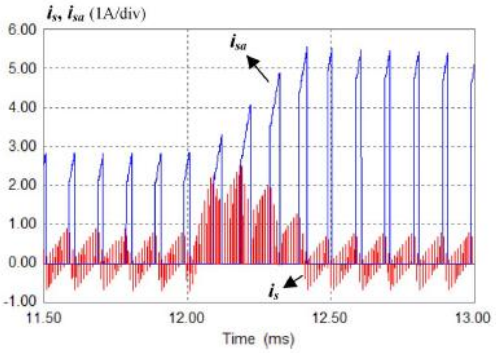


Fig 9. Switch current waveforms.

The waveform with large magnitude denotes the current flowing through the low-frequency switch $I_{sa}$, and the small magnitude is the current of the high-frequency switch $i_{sa}$. The load is changed from 4 to 2 Ω at the 12-ms time instant. A major portion of the increased load current is diverted to the low-frequency buck cell, while the current through the high-frequency switch remains the same. The current diversion enables the reduction of switching loss in high-frequency buck cell and improves the efficiency.

**C. EFFICIENCY ANALYSIS**

In order to analyze the efficiency improvement of the proposed DF buck converter, the efficiency expression is analyzed in the section. The analysis is also applied to the single high frequency buck and low-frequency buck converters. Various loss estimation methods have been proposed in the literature based on different assumptions.

A simple loss model is adopted here in that we just want to show the efficiency relationship between the DF buck and single high-frequency buck, not to develop a new loss model. In the analysis, we have the following assumptions.

1) The conduction losses of active switch and diode are estimated, respectively, according to their conduction voltages $U_{on}$ and $U_F$.

2) The switching transient processes are assumed to satisfy the linear current and voltage waveforms. Moreover, the turn-on time ton is the same for all switches and diodes, so is the turn-off time $t_{off}$.

3) Since the switching loss usually dominates the total loss, losses of the output capacitor and output inductor are not calculated here.

In a single-frequency buck converter, the total loss $P_{SF}$ comes from four parts, the conduction loss $P_{scon}$ and switching loss $P_{ss}$ of the active switch S, and the conduction loss $P_{dcon}$ and switching loss Psd of the diode. When the input voltage is $U_{in}$, duty ratio is D, the inductor average current is IL, and the switching frequency is $f_s$, the losses can be estimated according to the following equations

$$\begin{aligned} P_{\mathrm{scon}} &= D \cdot U_{\mathrm{on}} I_{\mathrm{L}} \\ P_{\mathrm{dcon}} &= (1-D) \cdot U_{\mathrm{F}} I_{\mathrm{L}} \\ P_{\mathrm{ss}} &= \frac{1}{2} f_{\mathrm{s}} \cdot U_{\mathrm{in}} I_{\mathrm{L}} (t_{\mathrm{on}} + t_{\mathrm{off}}) \\ P_{\mathrm{sd}} &= \frac{1}{2} f_{\mathrm{s}} \cdot U_{\mathrm{in}} I_{\mathrm{L}} (t_{\mathrm{on}} + t_{\mathrm{off}}). \end{aligned}$$

For single-frequency buck converter, the conduction losses are the same; the difference is on the switching frequencies fh and fl. For DF buck, the losses consist of two portions: high frequency cell losses and low-frequency cell losses. The current chopped by the high-frequency cell is the difference between high-frequency inductor current $i_L$ and low-frequency inductor current $i_{La}$. This difference is roughly equal to 0.5 $I_{Lapk}$, where $I_{Lapk}$ is the peak–peak low-frequency inductor current ripple, because the inductor current ripple of the high-frequency cell is small compared with that of the low-frequency cell. Moreover, the average current in low-frequency inductor is IL − 0.5 $I_{Lapk}$ with the peak current control. The loss break down can be expressed as follows:

The losses in the high-frequency cell are

$$\begin{aligned} P_{\mathrm{sconH}} &= 0.5D \cdot U_{\mathrm{on}} I_{\mathrm{Lapk}} \\ P_{\mathrm{dconH}} &= 0.5(1-D) \cdot U_{\mathrm{F}} I_{\mathrm{Lapk}} \\ P_{\mathrm{ssH}} &= \frac{1}{4} f_{\mathrm{h}} \cdot U_{\mathrm{in}} I_{\mathrm{Lapk}} (t_{\mathrm{on}} + t_{\mathrm{off}}) \\ P_{\mathrm{sdH}} &= \frac{1}{4} f_{\mathrm{h}} \cdot U_{\mathrm{in}} I_{\mathrm{Lapk}} (t_{\mathrm{on}} + t_{\mathrm{off}}). \end{aligned}$$

The losses in the low-frequency cell include

$$\begin{aligned} P_{\mathrm{sconL}} &= D \cdot U_{\mathrm{on}} (I_{\mathrm{L}} - 0.5 I_{\mathrm{Lapk}}) \\ P_{\mathrm{dconL}} &= (1-D) \cdot U_{\mathrm{F}} (I_{\mathrm{L}} - 0.5 I_{\mathrm{Lapk}}) \\ P_{\mathrm{ssL}} &= \frac{1}{2} f_{\mathrm{l}} \cdot U_{\mathrm{in}} (I_{\mathrm{L}} - 0.5 I_{\mathrm{Lapk}}) (t_{\mathrm{on}} + t_{\mathrm{off}}) \\ P_{\mathrm{sdL}} &= \frac{1}{2} f_{\mathrm{l}} \cdot U_{\mathrm{in}} (I_{\mathrm{L}} - 0.5 I_{\mathrm{Lapk}}) (t_{\mathrm{on}} + t_{\mathrm{off}}). \end{aligned}$$

Then, the total conduction loss $P_{con}$ DF in the DF buck is approximately the same as that in the single frequency buck converter

$$P_{\mathrm{conDF}} \approx P_{\mathrm{scon}} + P_{\mathrm{dcon}}.$$

In the case the low-frequency inductor current is small with reference to the inductor average current, the total switching loss $P_{sDF}$ can be approximated as

$$P_{\mathrm{sDF}} \approx f_{\mathrm{l}} \cdot U_{\mathrm{in}} I_{\mathrm{L}} (t_{\mathrm{on}} + t_{\mathrm{off}}).$$

It follows that the total conduction loss of DF buck converter is the same as the single-frequency buck conductor. This result also can be reasoned from the fact that the total currents flowing through the DF buck switches and diodes are the same as that through a single-frequency buck. On the other hand, the total switching loss is nearly the same as the single low-frequency buck, and is much smaller than that of the single high-frequency buck. Hence, the DF buck converter improves the efficiency by current diversion to the low-frequency cell. Although assumptions and approximations are made in the aforementioned analysis, it reveals the efficiency mechanism of the DF buck converter.

 

## IV. EXPERIMENTAL RESULTS

In this section, the ac small-signal model of the DF buck converter is presented. The conventional buck converter, which operates at only one switching frequency, is also given for comparison. Moreover, we show that the operation of the high frequency buck cell is decoupled from the low-frequency cell. The state equations of the high-frequency cell are obtained using the averaging method as in

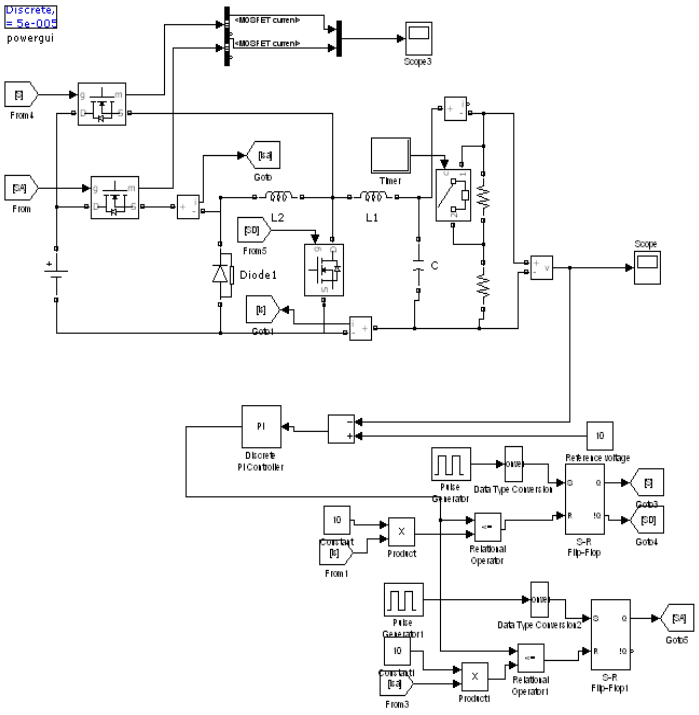


Fig 10 Double Frequency Buck Converter

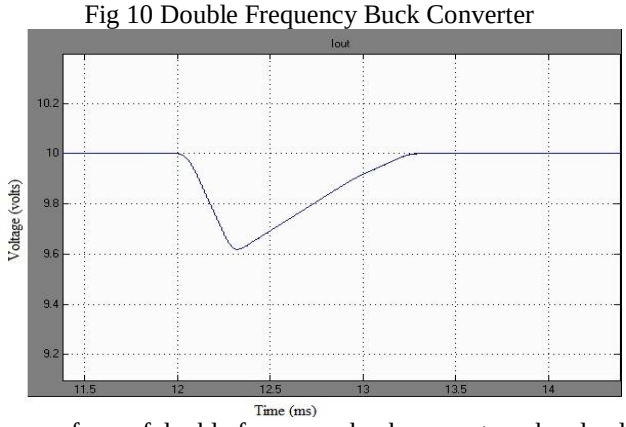


Fig 11 Output wave form of double frequency buck converter when load is step down

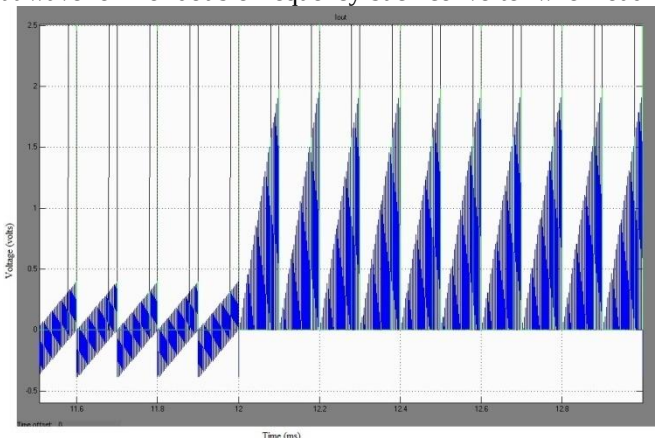


Fig 12 Double frequency buck converter switch current waveforms

## V. CONCLUSION

This project has explaining the concept of a novel topology of double frequency buck converter. Analytical and experimental results have demonstrated that, the double frequency buck converter not only exhibits the same steady state and transient performance but also improving the efficiency of conventional buck converters successfully. The proposed converter does not need the load transient change information for accurate current control and does not have the current circulating problem. Future work will investigate whether the proposed buck converter is applicable for high current or high dynamics specifications.

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