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Crosstalk Modeling and Analysis of Coupled RLC Interconnect for Signal Integrity

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Abstract— *With the technology advancements in the field of chip fabrication, the signal clock rates and data-rates are in several Giga-Hertz ranges. Simultaneously, signal rise times (edge rates) are in Pico-seconds range. On-chip interconnects on a multilayer board stack-up plays a vital role and constitute as major source of circuit delay than gate delays. This is because of decrease of trace width and various devices parasitic's on the chip. These can cause several implications such as electro-magnetic (EMI) issues in the designs. These problems can pose several design challenges to the designers with the Signal Integrity problems such as ringing, double clocking, non-monotonicity and performance degradation of designs. Typically, there are numerous analytical and numerical approaches used for the analysis of high speed interconnects. Each approach is different from the other in different domains of evaluation. Here, crosstalk voltage modeling and analysis of coupled RLGC models of interconnects with transient analysis in time domain is proposed. Transient analysis of lumped, coupled and distributed models of RLC interconnects is performed and performance metrics delays, average power, PDP and crosstalk voltages are measured. Hence, accurate modeling and validation of interconnect models is essential for the successful transmission of signals without ringing, crosstalk and EMI problems. These reduce the propagation delays and increase the overall circuit performance in-terms of speed.*

Index Terms— *Microstrip, Interconnect/trace, RLC, EMI, Crosstalk, Far End Crosstalk(FEXT), Near End Crosstalk(NEXT), Signal Integrity(SI), Delays, lumped, PDP,*

I. INTRODUCTION

In the deep-submicron (DSM) regime, high speed designs have faster edge rates signals and switching fast characteristics. Advancements in the chip fabrication technology, present high speed logics and designs are operating at much higher speed. The clock rates of the signal in high speed (>10MHz) designs have reached the GHz range and edge rates of the signal droped below 100pico-seconds range (e.g. DDR2, DDR3 and DDR4 designs) and signal frequency content of digital signals have extended to ≈10GHz. In addition, designs on IC's are becoming more complex, complicated with decreased trace widths and smaller geometries. On a multilayer board stack-up, the effects of increase in frequency (GHz), decrease of trace widths and edge rates of the signals are always posing challenges to the designers with several critical signal integrity problems. These problems of SI are directly related to dV/dt or dI/dt, fast rise times that significantly worse some of the noise phenomena: power/ground switching noise, crosstalk, ringing, reflections and over/shoot. Many of problems of SI are electromagnetic in nature referred as EMI/EMC. These can degrade the overall performance of the system. So, it becomes essential to understand, where these problems of SI come from, analyze them and solve the problems at the early stage of design else the process of solving is time taking and cost effective. The fundamental goal of SI is to ensure high speed, reliable data transmission without ringing, crosstalk, double clocking, non-monotonicity etc.SI is the measure of quality of signal (QoS), determined by quality (shape with thresholds) and arrival time of the signal. The signal timing depends on delays which in-turn depends on the physical length of interconnects, that the signal needs to propagate through. The designers must ensure the reliability of the designs by highlighting the problems of SI and EMI. Hence, thereby increases the quality of signal transmission that are high speed, reliable to obtain optimum performances from the designs. Interconnects constitute as dominant source of circuit delay than gate delays [1]. Depending on the physical length, often interconnects on the IC are modeled as distributed model with resistance, capacitance and inductance parasitic's. Interconnect delays is playing a vital role in circuit design and performance.

In a complicated multi-layered high speed interconnect system designs, propagation delays and signal coupling greatly affects circuit performances and lowers the yield of IC chips. A proper care needs to be taken regarding critical interconnects spacing, dimensions, layouts, and device parasitic's etc., prior to design. On a multilayer board stack-up, crosstalk is referred as the undesired voltage imparted from a aggressor line to a adjacent trace/interconnect (victim). Magnitude of crosstalk voltage induced in to a victim line is a function of rise time, trace geometry and type of terminations used.

Major impacts of cross talk in high speed designs are:

(a) Crosstalk induces timing delays that change the signal propagation time, and in-turn leads to setup/hold time failures.

(b) Crosstalk induces glitches at the output, this causes voltage spikes on interconnect, results in false logic.

Hence, an accurate interconnect modeling, estimate and characterization of the crosstalk peak noise in interconnects is therefore very crucial for today's high speed designs. Model characterization is performed using transient analysis in time domain. The performance metrics of coupled lumped and distributed RLC models are evaluated. The objective of this work is to model and analyze the crosstalk coupling noise between the aggressor(s) and a victim line of a coupled RLGC

interconnects. Delay modeling of lumped model of RLC is presented in section-2. Subsequently crosstalk modeling of coupled interconnects in section-3. Crosstalk analysis of distributed interconnect model is presented in section-4 then followed by conclusion in section-5.

II. DELAY MODELING OF LUMPED RLC INTERCONNECT

For SI analysis, interconnect/trace on a chip are either modeled as lumped or distributed models of transmission lines that serves as medium of sending signals. The propagation delay along the trace depends on circuit parasitic's and on the physical length of trace. Delay modeling of lumped model of RLC interconnect is shown in Figure.1. Here, voltage along both ends of trace changes instantaneously with propagation time(tp>>pD) neglected. But in a distributed model, the signal propagation time(tp) is considered along with length of the trace.

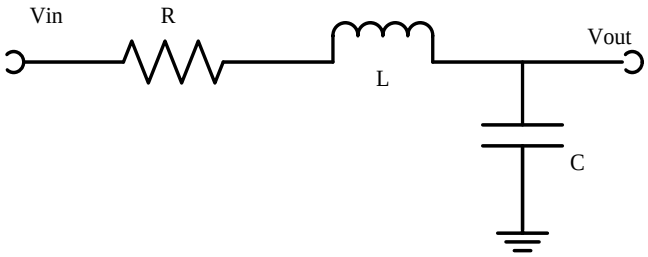

Fig. 1. Model of RLC Interconnect.

Apply the KVL to the RLC model of interconnect shown in Fig.1. Assume that i(t) be the current flowing in the RLC model which yields equation (1):

$$V_i(t) = V_R + V_L + V_C \tag{1}$$

$$V_i(t) = iR + L\frac{d}{dt}i(t) + \frac{1}{C}\int i(t)dt$$

$$V_i(t) = RCV_C(t) + LC\frac{d}{dt}V_C(t)) + V_C(t) \tag{2}$$

Differentiate the equation (2) w.r.t to t yields

$$\frac{d}{dt}V_i(t) = C\frac{d}{dt}V_C(t)R + LC\frac{d^2}{dt^2}V_C(t)) + V_C(t)$$

$$\frac{1}{LC}\frac{d}{dt}V_i(t) = \frac{R}{L}\frac{d}{dt}V_C(t) + \frac{d^2}{dt^2}V_C(t)) + \frac{V_C(t)}{LC} \tag{3}$$

Since the obtained equation (3) is in time domain, use Laplace Transforms to covert from time domain to frequency domain for easy analysis.

$$\frac{1}{LC}V_i(s) = V_C(s)\left[s^2 + \frac{R}{L}s + \frac{1}{LC}\right]$$

$$\frac{V_C(s)}{V_i(s)} = \frac{1/LC}{s^2 + sR/L + 1/LC}$$

The transfer function of lumped model of RLC interconnects in frequency domain is given by second order equation (4):

$$H(s) = \frac{1/LC}{s^2 + sR/L + 1/LC} \tag{4}$$

The standard second order characteristic transfer function is given by equation (5) .

$$H(s) = \frac{\omega_n^2}{s^2 + 2\xi\omega_n s + \omega_n^2} \tag{5}$$

On comparing the second order transfer function of RLC model i.e. equation (4) with the standard form of characteristic equation (4), we obtain the parameters such as angular frequency(w_n) and damping factor(ξ).

$$\omega_n^2 = \frac{1}{LC} \quad , \quad 2\xi\omega_n = \frac{R}{L}$$

Delay (τ) of a lumped model of RLC interconnects is defined by the R, L, and C parasitic elements and is given by (6):

$$\tau = 2L/R \tag{6}$$

Approximate delay (τ) for distributed models of RLC interconnect of n^{th} stage is given by (7).

$$\tau = \frac{2L}{R} + \frac{R^2 + RL + 2L}{R} + .. + \frac{nR^2 + nRL + 2L}{R} \tag{7}$$

Figure.2 shows the transient analysis of the lumped model of RLC interconnect with the element parameters: R=15Ω, L=22.5nH and C=9.0pF. Transient analysis is performed with a pulse as input with edgerate(rise, falltime) equals 50ps and period of pulse is 40ns. Here, RLC interconnect/ trace is assumed as a microstrip on a PCB. The length of the trace/interconnect is L=3 inch, width W=8.0 mils, Dielectric height H=6.0 mils with a dielectric constant $\varepsilon_r = 4.3$. The characteristic impedance of interconnect is Z_0=50Ω and the delay through the trace is td=448ps.

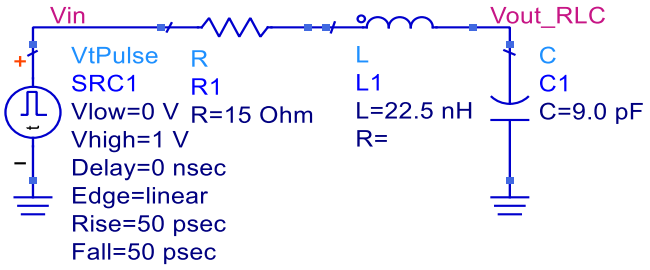

Fig. 2. Transient analysis of RLC Interconnect.

The transient response of 3 inch RLC interconnect is shown in Fig.3. Response shows that ringing is present at the output and this is due to the inductance (L) effect at high frequencies.

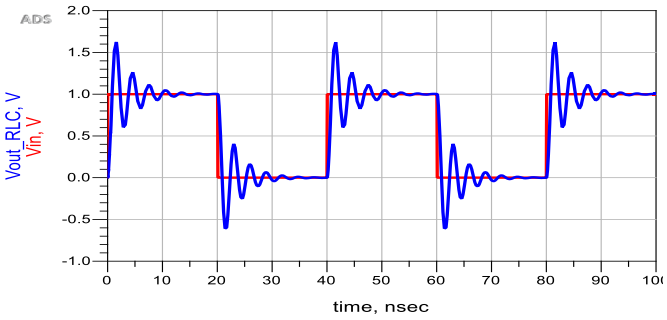

Fig. 3. Transient Response of RLC Interconnect.

III. Crosstalk Modeling of Coupled Interconnects

A PCB stackup is a multilayer board with many signal traces, vias and power planes(Vdd, Gnd) on it. At high frequencies interconnect/trace on a PCB are often modeled as transmission lines i.e. microstrip, stripline, etc with various dielectric materials used as substrates. The signal propagates through the trace at a speed of 6''/1ns which equals 165ps/inch approximately. A model of coupled traces is shown in Fig.4.

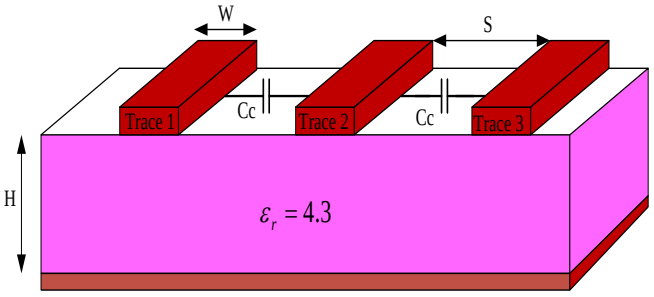

Fig. 4. Coupled model of trace/interconnect on a substrate.

On a multilayer board stack-up, crosstalk coupling happens when two signal traces/interconnects are running side by side to each other for some significant length i.e. data line. Crosstalk is generated between the traces due to coupling(C_C) and energy gets coupled from one trace(aggressor) to the adjacent trace(victim). Crosstalk increases with fast edge-rates(<100ps) and ringing thereby increasing di/dt. Crosstalk problems can be solved by placing the signal traces in close proximity to the (Vdd, Gnd) planes, use of guard traces and increase copper pour on the board to decrease current density. A relationship between trace width(W) and impedance(Z_0) of the trace/interconnect is given as (8):

$$Width(W) \alpha \frac{1}{Z_0} \tag{8}$$

High speed designs that are operating at high frequencies and fast edge-rates, crosstalk effect between traces/interconnects is an undesired effect that can cause several SI problems. Therefore, accurate crosstalk modelling between coupled interconnects and characterization is very essential. Crosstalk can affect the mutual inductance (M) as well as coupling capacitance (Cc=2.0pF) between interconnects.

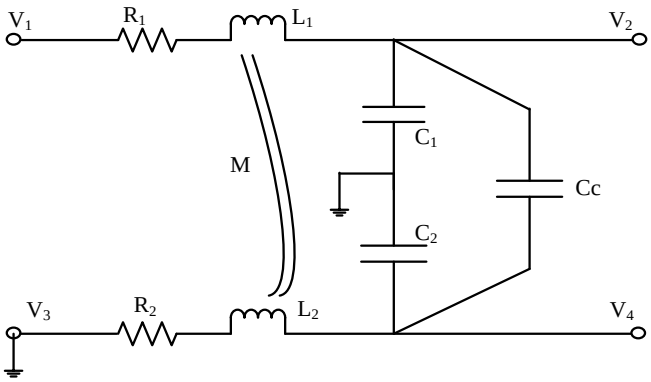

Fig. 5. Model of Coupled RLC Interconnect.

Figure.5 is used for theoretical modeling and analysis of crosstalk voltage in a coupled RLC interconnects. Analysis is performed with assumption V3=0 (Gnd) and the coupling coefficient between the inductors L1 and L2 is K=0.2. The crosstalk voltage induced by aggressor line on to Victim line are of two kinds i.e. Far End Crosstalk (FEXT) at V4 as output and Near End Crosstalk (NEXT) at V3 are estimated for a coupled RLC interconnect model shown in Fig.5.

Now applying the nodal analysis to coupled RLC model of interconnect shown in Fig.5.

$$\frac{V_2 - V_1}{(R_1 + sL_1)} + \frac{V_2}{1/sC_1} + \frac{V_2 - V_4}{1/sC_C} = 0 \tag{9}$$

$$V_2\left[\frac{1}{(R_1 + sL_1)} + sC_1 + sC_C\right] = \frac{V_1}{(R_1 + sL_1)} + V_4 * sC_C$$

$$V_2\left[(1 + sR_1C_1 + sR_1C_C + s^2L_1C_1 + s^2L_1C_C)\right] = V_1 + V_4 * (sR_1C_C + s^2L_1C_C) \tag{10}$$

$$\frac{V_4 - V_2}{1/sC_C} + \frac{V_4}{(R_2 + sL_2)} + \frac{V_4}{1/sC_2} = 0 \tag{11}$$

$$V_4\left[\frac{1}{(R_2 + sL_2)} + sC_2 + sC_C\right] = V_2 * sC_C \qquad V_4 = \frac{sR_2C_C + s^2L_2C_C}{\left[(1 + sR_2C_C + sR_2C_2 + s^2L_2C_C + s^2L_2C_2\right]} * V_2 \tag{12}$$

The output voltage V_2 of the aggressor trace w.r.t input voltage V_1 is obtained by substitution of equation (12) in (10).

$$V_2\left[(1 + sR_1C_1 + sR_1C_C + s^2L_1C_1 + s^2L_1C_C)\right] = V_1 + \frac{(sR_1C_C + s^2L_1C_C)(sR_2C_C + s^2L_2C_C)}{(1 + sR_2C_1 + sR_2C_C + s^2L_2C_2 + s^2L_2C_C)} * V_2$$

$$V_2\left[\frac{(1 + s(R_1C_1 + R_1C_C) + s^2(L_1C_1 + L_1C_C)) * (1 + s(R_2C_1 + R_2C_C) + s^2(L_2C_2 + L_2C_C)) - (sR_1C_C + s^2L_1C_C)(sR_2C_C + s^2L_2C_C)}{(1 + sR_2C_1 + sR_2C_C + s^2L_2C_2 + s^2L_2C_C)}\right] = V_1$$

$$V_2\begin{bmatrix} 1 + s(R_1C_1 + R_2C_2 + R_1C_C + R_2C_C) + s^2(L_2C_C + R_1R_2C_1C_C + R_1R_2C_1C_2 + \\ R_1R_2C_2C_C + L_2C_2 + L_1C_1 + L_1C_C) + s^3(R_2L_1C_2C_C + R_2L_1C_1C_2 + R_2L_1C_1C_C + \\ R_1C_1L_2C_2 + R_1C_1L_2C_C + R_1L_2C_2C_C) + s^4L_1L_2(C_1C_2 + C_1C_C + C_2C_C) \end{bmatrix} = V_1 * \left[(1 + sR_2C_C + sR_2C_2 + s^2L_2C_C + s^2L_2C_2)\right] \tag{13}$$

Therefore, output voltage V_2 of the aggressor trace with victim trace grounded (V_3=0) is given by equation (14).

$$V_2 = V_1 * \frac{1 + sR_2(C_C + C_2) + s^2L_2(C_C + C_2)}{(1 + s(R_1C_1 + R_2C_2 + R_1C_C + R_2C_C) + s^2(L_1(C_C + C_1) + R_1R_2(C_2C_C + C_1Cc + C_1C_2) + L_2(C_2 + C_C))} + s^3(R_2L_1(C_2C_C + C_1C_C + C_1C_2) + R_1L_2(C_2C_C + C_1C_C + C_1C_2)) + s^4(L_1L_2(C_2C_C + C_1C_C + C_1C_2)) \tag{14}$$

The crosstalk voltage, FEXT (V_4) at the end of victim trace because of coupling of aggressor trace is calculated as follows. Here equation (12) can be is re-written as:

$$V_2 = V_4 * \frac{(1 + sR_2C_C + sR_2C_2 + s^2L_2C_C + s^2L_2C_2)}{(sR_2C_C + s^2L_2C_C)}$$

Substitute value of V_2 in equation (10) to obtain the theoretical expression for crosstalk voltage FEXT (V_4) on the victim trace.

$$V_4\left[\frac{(1 + sR_2C_C + sR_2C_2 + s^2L_2C_C + s^2L_2C_2)}{(sR_2C_C + s^2L_2C_C)}\right]\left[(1 + sR_1C_C + sR_1C_1 + s^2L_1C_C + s^2L_1C_1)\right] = V_1 + V_4(sR_1C_C + s^2L_1C_C)$$

On simplifying the above equation, crosstalk voltage FEXT (V_4) is derived as in equation (15).

$$V_4 = V_1 * \frac{sR_2C_C + s^2L_2C_C}{(1 + s(R_1C_1 + R_2C_2 + R_1C_C + R_2C_C) + s^2(L_1(C_C + C_1) + R_1R_2(C_2C_C + C_1C_C + C_1C_2) + L_2(C_2 + C_C))} + s^3(R_2L_1(C_2C_C + C_1C_C + C_1C_2) + R_1L_2(C_2C_C + C_1C_C + C_1C_2)) + s^4(L_1L_2(C_2C_C + C_1C_C + C_1C_2)) \tag{15}$$

Similarly, theoretical expression for crosstalk voltage NEXT (V_3) is derived as in equation (16).

$$V_3 = \frac{C_C}{(Cc + C_2) + sR_1(C_1C_2 + C_1C_C + C_2C_C) + s^2L_1(C_1C_2 + C_2C_C + C_1C_C)} \tag{16}$$

A. Transient Analysis of Coupled RLC Interconnect

The transient analysis objective is to evaluate the amount of crosstalk voltage injected on to victim trace due to both capacitive and inductive coupling. During analysis, RLC interconnect/ trace is assumed as a microstrip on a multilayer PCB of length L=3 inch, width W=8.0 mils, Dielectric height H=6.0 mils with a dielectric constant $\varepsilon_r = 4.3$.The characteristic impedance of trace is Z_0=50Ω and the delay through the trace is t_d=448ps. The trace element parameters are: R_1=15Ω, R_2=15Ω, C_1=C_2=9.0pF, C_C=2.0pF, L_1=L_2=22.5nH, K=0.2.

Therefore with these parameters the output voltage V_2 obtained on the aggressor line is given in equation (17).

$$\frac{V_2}{V_1} = \frac{2.475\text{e-}19s^2 + 1.65\text{e-}10s + 1}{5.923\text{e-}38s^4 + 7.897\text{e-}29s^3 + 5.213\text{e-}19s^2 + 3.3\text{e-}10s + 1} \quad (17)$$

Crosstalk voltage FEXT, on Victim is given in equation (18).

$$\frac{V_4}{V_1} = \frac{4.5\text{e-}20s^2 + 3\text{e-}11s + 1}{5.923\text{e-}38s^4 + 7.897\text{e-}29s^3 + 5.213\text{e-}19s^2 + 3.3\text{e-}10s + 1} \quad (18)$$

Crosstalk voltage NEXT, on Victim is given in equation (19).

$$\frac{V_3}{V_1} = \frac{2\text{e-}12}{2.632\text{e-}30s^2 + 1.755\text{e-}21s + 1.1\text{e-}11} \quad (19)$$

The transient analysis of two 3 inches coupled RLC trace/interconnects shown in Fig.6. is performed for a rising, falling edge-rates of 50ps respectively. A pulse is applied on the aggressor trace (V_1) with victim trace (V_3=0) as grounded.

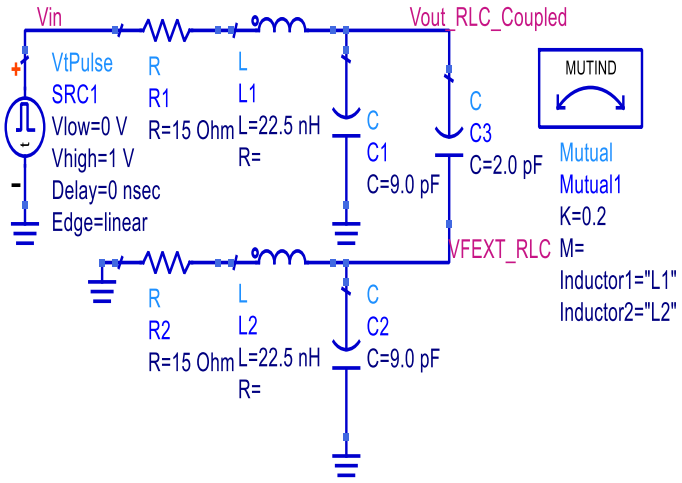

Fig. 6. Transient Analysis of Coupled RLC Interconnect.

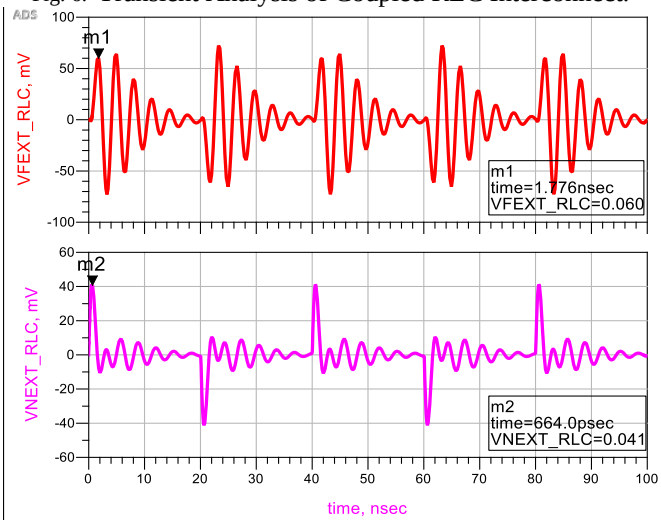

Fig. 7. FEXT and NEXT Response of Coupled RLC Interconnect.

Figure.7 shows the crosstalk voltage response of a coupled RLC respectively because of the affect of aggressor on to the victim trace. FEXT voltage is ≈ 133 mV peak-to-peak and NEXT voltage ≈ 52 mV peak-to-peak. FEXT voltage (>100 mV) could cause several signal integrity problems.

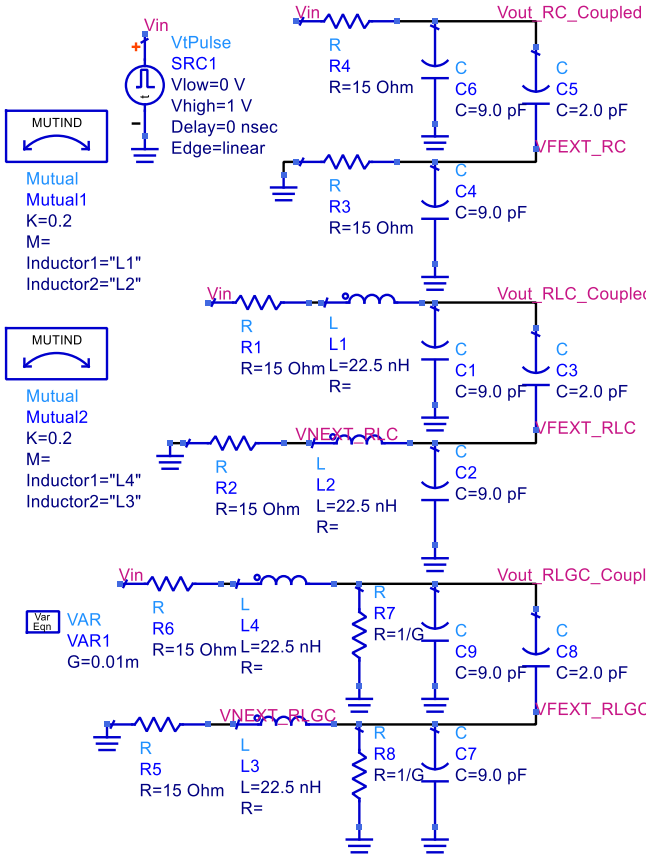

Fig. 8. Transient Analysis of Coupled RC, RLC and RLGC Interconnects.

The transient analysis of all coupled RC, RLC and RLGC trace/interconnects is shown in Fig.8. Crosstalk voltage FEXT response of RC, RLC and RLGC trace is shown in Fig.9.

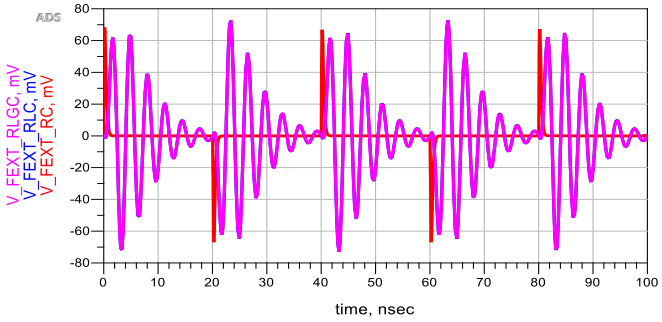

Fig. 9. FEXT Response of Coupled RC, RLC and RLGC Interconnects.

B. Effect of Mutual Inductance (M) on Coupled Inductors

At high frequencies, reactive component inductance(L) creates numerous signal integrity problems i.e. ringing due to inductive coupling. The inductors L_1 and L_2 are coupled with coupling coefficient K (0< K <1) so as to obtain minimum crosstalk.

$$K = \frac{M}{\sqrt{L1 * L2}} \tag{20}$$

An extra inductance gets added because of the coupling between the inductor coils L_1 and L_2 and is called as mutual inductance (M).

$$L_T = L_1 + L_2 + M$$

$$M = K * \sqrt{L_1 * L_2} \tag{21}$$

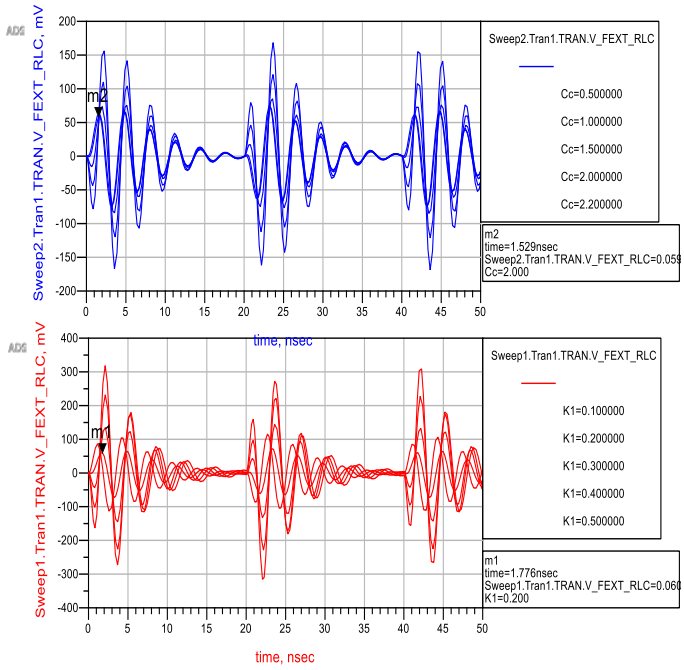

Fig. 10. Response for different values of K and C_C on Coupled Interconnects.

Parametric simulation response of 3 inch coupled RLC trace for different values of coupling coefficient (K=0.1:0.1:0.5) and coupling capacitor (C_C=0.5:0.5:2.2) is shown in Fig.10. This helps to find the optimal values of K and C_C so that the crosstalk voltage FEXT, on the victim trace is as low as possible. From the simulation result it is evident that for K=0.2 and C_C=2.0pF the crosstalk voltages on the victim trace is low. In a 3 inch coupled RLC trace inductors L_1 and L_2 are coupled through a mutual inductance (M) which adds an extra inductance on to interconnect. In order to observe the effects of M on L_1 and L_2 two test cases have been considered. The step response for output voltage, FEXT and NEXT voltage response respectively with selected optimum values of K=0.2, C_C=2.0pF and L_1=L_2=22.5nH, M=4.5nH are shown in Fig.11, Fig.12 and Fig.13.

Case (i): (L1-M) and (L_2-M) = (22.5nH-4.5nH) =18nH

$$\frac{V_2}{V_1} = \frac{1.98e-19s^2+1.65e-10s+1}{3.79e-38s^4+6.32e-29s^3+4.22e-19s^2+3.3e-10s+1}$$

$$\frac{V_4}{V_1} = \frac{1.2e-09s^2+s}{3.79e-38s^4+6.32e-29s^3+4.22e-19s^2+3.3e-10s+1}$$

$$\frac{V_3}{V_1} = \frac{1.82e-01}{1.91e-19s^2+1.6e-10s+1}$$

Case (ii): (L1+M) and (L_2+M) = (22.5nH+4.5nH) = 27nH

$$\frac{V_2}{V_1} = \frac{2.97e-19s^2+1.65e-10s+1}{8.53e-38s^4+9.48e-29s^3+6.2e-19s^2+3.3e-10s+1} \quad \frac{V_4}{V_1} = \frac{1.8e-09s^2+s}{8.53e-38s^4+9.48e-29s^3+6.2e-19s^2+3.3e-10s+1}$$

$$\frac{V3}{V1} = \frac{1.82e-001}{2.87e-019s^2+1.6e-010s+1}$$

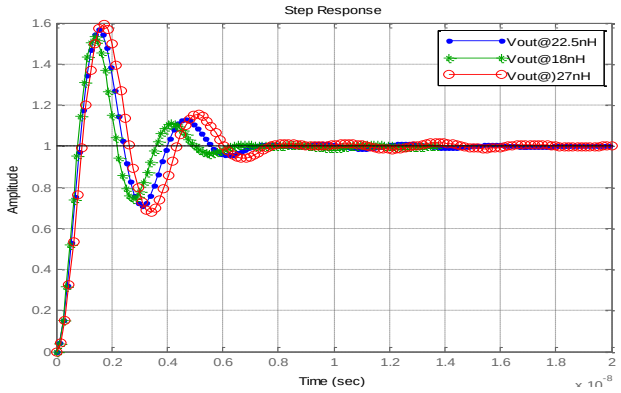

Fig. 11. Analysis of Vout with L=22.5nh, 18nH and 27nH.

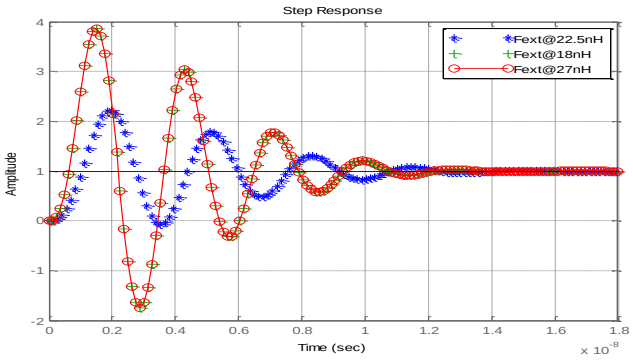

Fig. 12. FEXT Voltage with L=22.5nh, 18nH and 27nH.

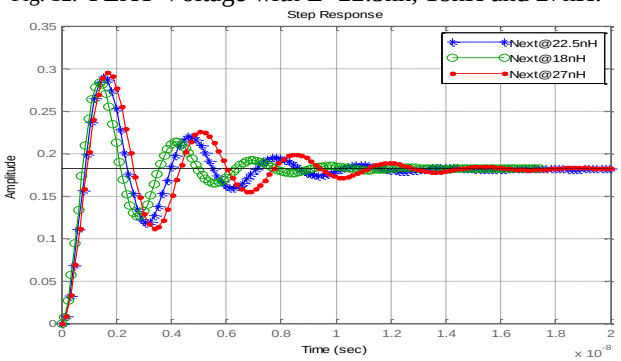

Fig. 13. NEXT Voltage with L=22.5nh, 18nH and 27nH.

IV. CROSSTALK ANALYSIS OF DISTRIBUTED RLC MODEL

A. Distributed model of RLC interconnect

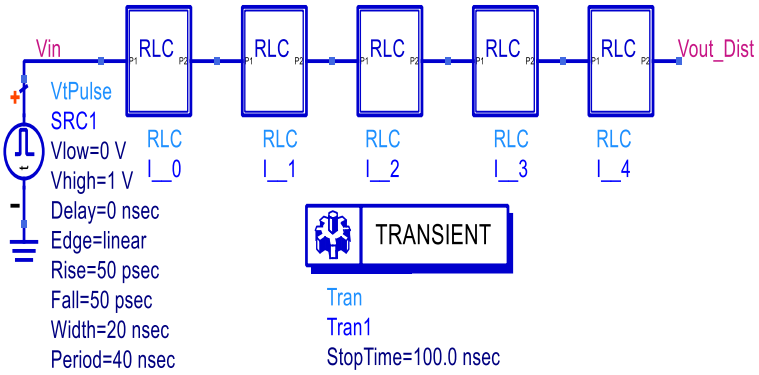

Fig. 14. Transient Analysis of Distributed model of RLC interconnect.

The transient analysis of distributed model of RLC trace/interconnects is obtained by cascading of lumped RLC is shown in Fig.14. RLC interconnect/ trace is on a PCB is assumed as a microstrip of length L=5*3 inch=15 inches, width W=8.0 mils, Dielectric height H=6.0 mils with a dielectric constant $\varepsilon_r = 4.3$.Simulation response is shown in Fig.15, which shows that the delay and time of flight have increased when compared with result in Fig.3. A comparison of lumped RLC and distributed RLC models is listed in Table II.

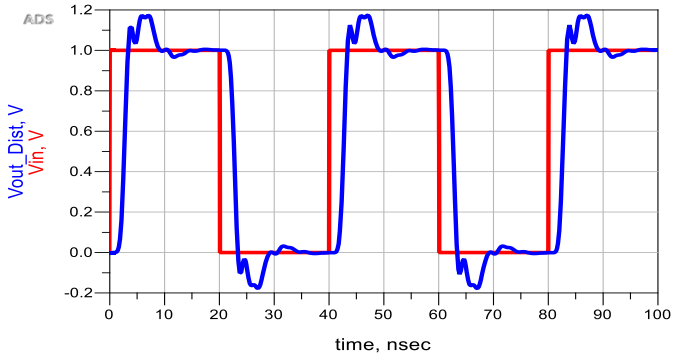

Fig. 15. Transient Analysis of Distributed model of RLC interconnect.

B. Distributed Coupled RLC interconnect model

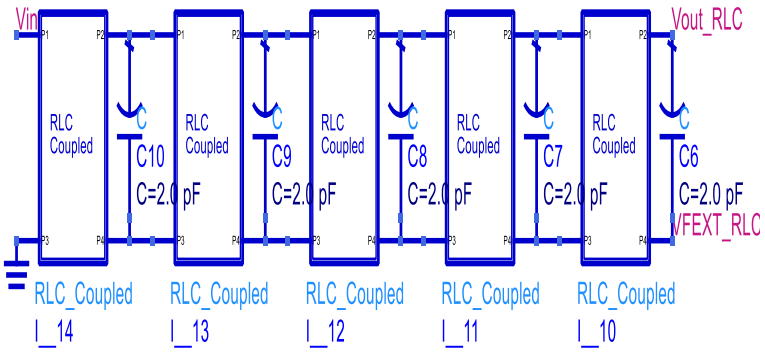

Fig. 16. Transient Analysis of Distributed Coupled RLC model.

Transient Analysis of microstip trace of coupled length L=5*3 inch=15 inches, width W=8.0 mils, Dielectric height H=6.0 mils with a dielectric constant $\varepsilon_r = 4.3$ on a multilayer PCB is shown in Fig.16. The two traces are coupled through capacitive coupling Cc=2.0pF.The transient response for output voltage and crosstalk voltages FEXT and NEXT are shown in Fig.17 and Fig.18.

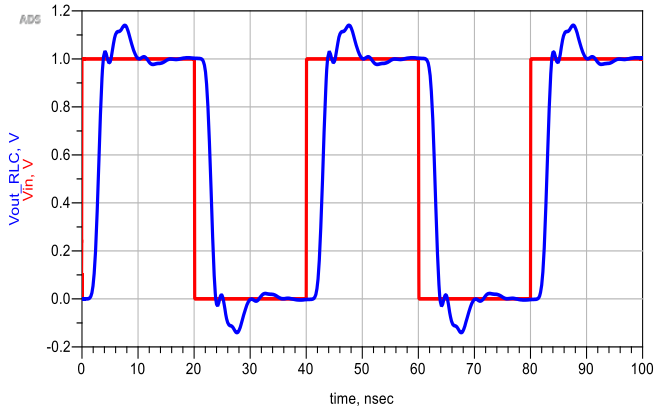

Fig. 17. Transient Response of Distributed model of Coupled RLC.

FEXT voltage is ≈ 268 mV peak-to-peak and NEXT voltage ≈ 84 mV peak-to-peak. Typically, FEXT voltage (>100 mV) could cause several signal integrity problems.

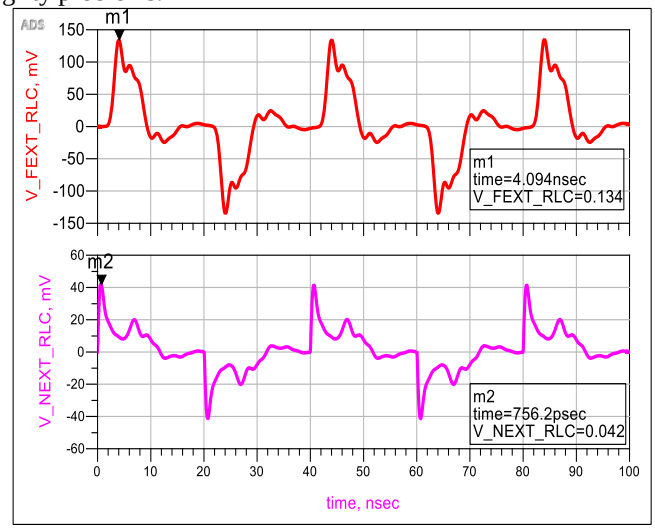

Fig. 18. FEXT and NEXT Response of Distributed Coupled RLC Interconnect.

Figure.19 and Table-I shows the crosstalk voltage FEXT response of all the distributed coupled models of RC, RLC and RLGC trace/interconnects with microstrip parameters.

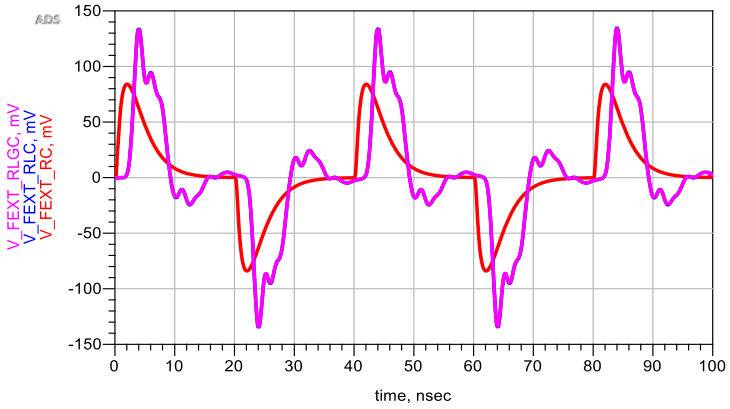

Fig. 19. FEXT Response of Distributed Coupled RC, RLC and RLGC Interconnect.

TABLE I. COMPARISON OF CROSSTALK VOLTAGES OF COUPLED INTERCONNECTS.

Type of Models	**Lumped Coupled Models**		**Distributed Coupled Models**	
	VNEXT (mV)	VFEXT (mV)	VNEXT (mV)	VFEXT (mV)
RC	0	134	80	168
RLC	52	133	84	268
RLGC	51	133	82	268

Table I lists the comparison of crosstalk voltages FEXT and NEXT for coupled models of RLC trace/interconnects in a transient analysis.

TABLE II. COMPARISON OF DELAYS AND POWER IN INTERCONNECTS.

	Lumped Models			**Distributed Models**		
	Delay (ps)	**Avg Power (uW)**	**PDP (Joules)**	**Delay (ns)**	**Avg Power (mW)**	**PDP (Joules)**
RC	338.00	255.00	8.619 e-14	4.17	1.33	5.546 e-12
RLC	778.62	319.20	2.485 e-13	3.315	1.337	4.434 e-12
RLGC	778.78	324.25	2.525 e-13	3.317	1.363	4.521 e-12

TABLE III. COMPARISON OF DELAYS AND POWER IN COUPLED INTERCONNECTS.

	Coupled Lumped Models			**Coupled Distributed Models**		
	Delay (ps)	**Avg Power (uW)**	**PDP (Joules)**	**Delay (ns)**	**Avg Power (mW)**	**PDP (Joules)**
RC	394.26	314.61	1.240 e-13	5.017	1.631	8.185 e-12
RLC	845.86	296.58	2.508 e-13	3.844	1.660	6.381 e-12
RLGC	846.02	302.63	2.560 e-13	3.848	1.684	6.480 e-12

The length of the trace/interconnects also determines the delay and timing of output signal. The amount of delay for a given length (L) varies from layer to layer on a multilayer PCB. Table II lists the comparison of delay, average power and power delay product (PDP) in lumped, distributed models. Table III lists the comparison of coupled lumped models and coupled distributed models of interconnects with SPICE simulation.

V. CONCLUSION

In this paper, an approach for modeling and analysis of crosstalk noise voltage in a coupled model of RLC trace/ interconnect is proposed. This is used to determine the crosstalk coupling effect between the two on-chip traces viz: aggressor and a victim trace. The effect of inductive cross-talk, capacitive crosstalk, and coupling are considered for various combinations coupling coefficient (K) and Cc on the aggressor and victim lines. Characterizations of all models of RLGC traces in time domain are performed with properties of microstrip (as trace) on a multilayer PCB. In the transient analysis crosstalk voltage metrics FEXT, NEXT are measured and compared for each coupled model of interconnects. The modeling approach can be used for fast estimation of crosstalk voltages in coupled traces. A detailed SPICE analysis of all RC, RLC and RLGC trace models are performed for propagation delays, average power and power delay products (PDP). A comparison of all models of interconnects with metrics are listed in tables.

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