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CASCADED MULTILEVEL INVERTER BASED UNIFIED POWER FLOW CONTROLLER

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ABSTRACT- *In this paper, a cascaded multilevel inverter based unified power flow compensating scheme is proposed. The topology consists of two cascaded multilevel inverter for shunt and series compensations. They are connected to the transmission system through open-end windings of a three-phase transformer. The source current and voltage are compensated by STATCOM and SSSC respectively. The simulation study is carried out in MATLAB/SIMULINK to predict the performance of the scheme under balanced, unbalanced and fault conditions. The dc-link voltages of the inverters are regulated at different levels to obtain four-level operation. The system behavior is analyzed for various operating conditions.*

Keywords: *cascaded multilevel inverter, UPFC.*

I INTRODUCTION

The application of flexible ac transmission systems (FACTS) controllers, such as static compensator (STATCOM) and static synchronous series compensator (SSSC), is increasing in power systems. Because they have the ability to stabilize the transmission systems, reactive power compensation, active power oscillation damping, flicker attenuation, voltage regulation and to improve power quality (PQ) in distribution systems [3]. Generally, in high-power applications, var compensation is achieved using multilevel inverters [4]. These inverters consist of a large number of dc sources which are usually realized by Capacitors. Hence, the converters draw a small amount of active power to maintain dc voltage of capacitors and to compensate the losses in the converter. However, due to mismatch in conduction and switching losses of the switching devices, the capacitors voltages are unbalanced. Balancing these voltages is a major research challenge in multilevel inverters. Various control schemes using different topologies are reported in [5]–[9]. Among the three conventional multilevel inverter topologies, cascade H-bridge is the most popular for static var compensation because of its advantages like absence of clamped diodes and reduced number of capacitors [7], [8].However, the other types requires a Large number of dc capacitors. The control of individual dc-link voltage of the capacitors is difficult.

When the multi-level converter is applied to a STATCOM, each of cascaded H-bridge converters should be equipped with an isolated and split dc capacitor without any power source or circuit. This allows us to eliminate a bulky, heavy and costly line-frequency transformer from the cascade STATCOM [1]. Static var compensation by cascading conventional multilevel/ two level inverters is an attractive solution for high-power applications [1].

Static Synchronous Series Compensator (SSSC) is a FACTS device which has its wide range of applications in transmission lines and grids. Based on the performance of these FACTS devices flickering and SSR can also be reduced in transmission grids SSSC based hybrid series compensation scheme combine the capacitor action with TCSC and SSSC are employed in damping of SSR(sub-synchronous resonance)[2].when a cascade H- bridge multilevel inverter is used as SSSC. In this system harmonics can be reduced and also the transmission line voltage fluctuation can be minimized.

The idea of the unified power flow controller (UPFC) was first proposed by Gyugi in 1992 [4]. Since then, as the most sophisticated flexible ac transmission systems (FACTS) device, the UPFC has been researched widely and many papers dealing with UPFC's modeling, analysis, control, and application have been published in recent ten years The UPFC combines the functions of several FACTS devices and is capable of realizing voltage regulation, series compensation, and phase angle regulation at the same time, thus realizing the separate control of the active power and reactive power transmitted simultaneously over the line. Inverter 1 is in parallel with the transmission line, while Inverter 2 in series with the transmission line. The two inverters are connected back-to-back through a common dc-link. This arrangement enables real power flow in either direction between the two inverters. Inverter 2 provides the main function of the UPFC by injecting an ac voltage through a series connected transformer has controllable magnitude and phase angle and can be considered as a synchronous ac voltage source. Because the transmission line current flows through this voltage source, the Inverter 2 needs to exchange active and reactive power with the transmission line through the transformer. The needed reactive power can be generated independently by itself. The active power exchange is actually provided or absorbed by inverter1 through the common DC link.[3].

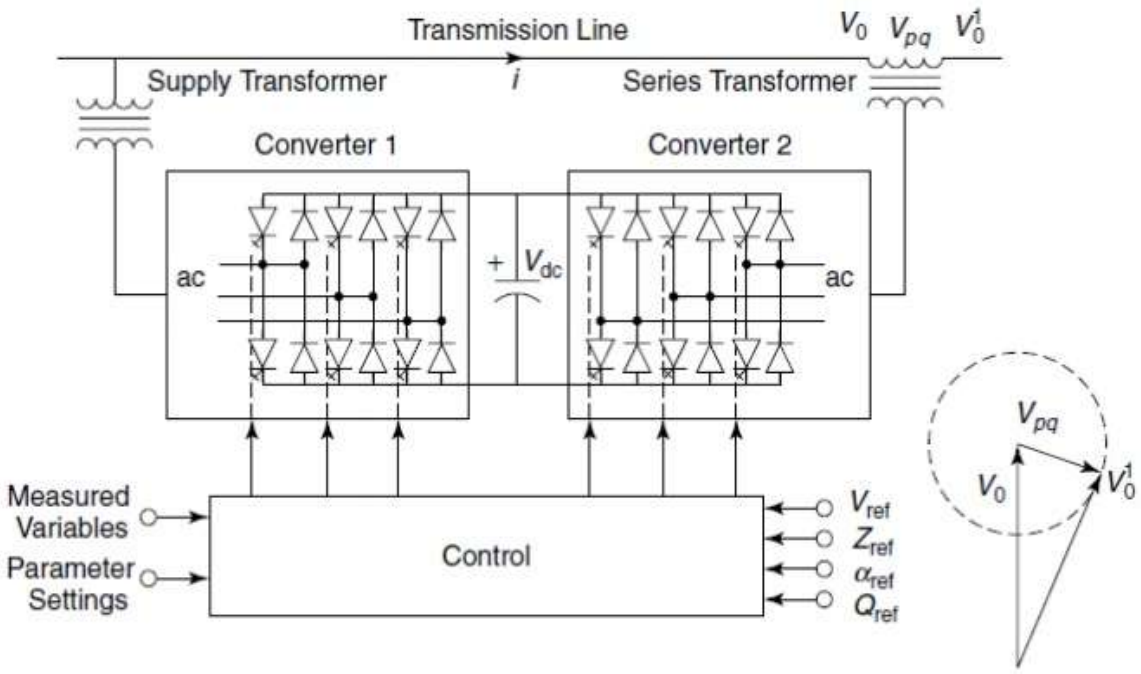

Fig.1 The implementation of the UPFC using two "back – to –back" VSCs with a common DC-link capacitor.

II CASCADED MULTILEVEL INVERTER BASED UPFC

In UPFC the shunt compensation is done by cascaded multilevel inverter based STATCOM and the series compensation is by cascaded multilevel inverter based SSSC separate control techniques are used for the reference voltage calculation. The switches used here are IGBT and the signals produced by sinusoidal pulse width modulation.

A. CONTROL TECHNIQUE FOR STATCOM

From [1] the following control technique is used for the control of STATCOM. The control block diagram is shown in Fig.2. The unit signals sin(ωt) and cos(ωt) are generated using three phase supply voltage (V_a, V_b, V_c).The converter currents (I_a, I_b, I_c) are transformed to the synchronous rotating reference frame using the unit signals. The switching frequency ripple in the converter current components is eliminated using a low pass filter. The controller generates the reference voltages. The inverter supplies the desired reactive current and draws required active current to regulate total dc-link voltage $V^*_{dc1}+ V^*_{dc2}$.The additional control is required to regulate individual dc-link voltages of the inverters. The resulting voltage of the cascaded converter can be given as $e_1\angle\delta$, where$e_{1=}\sqrt{ed2 + eq2}$and $\delta= \tan^{-1}\{(e_q) / (e_d)\}$.The active power transfer between the source and inverter depends on δ and is usually small in the inverters supplying var to the grid. Henceδ, can be assumed to be proportional to e_q . Therefore, the q -axis reference voltage component of inverter-2 e^*_{q2} is derived to control the dc-link voltage of inverter-2 as

$$e^*_{q2} = (V^*_{dc2} - V_{dc2}) \left(k_{p4} + \frac{k_{i4}}{s}\right) \quad (1)$$

The q -axis reference voltage component of inverter-1 e^*_{q1} is obtained as

$$e^*_{q1=} e^*_q - e^*_{q2} \quad (2)$$

The dc-link voltage of inverter-2 V_{dc2} is controlled at 0.366 times the dc-link voltage of inverter-1V_{dc1} .It results in four-level operation in the output voltage and improves the harmonic spectrum. Expressing dc-link voltages of inverter-1 and inverter-2 in terms of total dc-link voltageV_{dc2} as

$$V_{dc1} = 0.732 V_{dc} \quad (3)$$

$$V_{dc2} = 0.268 V_{dc} \quad (4)$$

Since the dc-link voltages of the two inverters are regulated, the reference -axis voltage componente^*_q is divided in between the two inverters in proportion to their respective dc-link voltage as

- $e_{d1}^{*} = 0.732e_{d}^{*}$ (5)
- $e_{d2}^{*} = 0.268e_{d}^{*}$ (6)

For a given power, if $(V_{dc2}^{*} > V_{dc2}$, $\delta_2 = \tan^{-1}\{(e_{q2}^{*}) / (e_{d2}^{*})\}$ increases and $\delta_1 = \tan^{-1}\{(e_{q1}^{*}) / (e_{d1}^{*})\}$ decreases. Therefore, power transfer to inverter-2 increases, while it decreases for inverter-1.

The power transfer to inverter-2 is directly controlled, while for inverter-1, it is controlled indirectly. Therefore, during disturbances, the dc-link voltage of inverter-2 is restored to its reference quickly compared to that of inverter-1.Network voltages is unbalanced due to asymmetric faults or unbalanced loads. As a result, negative-sequence voltage appears in the supply voltage. This causes a double supply frequency component in the dc-link voltage of the inverter.This double frequency component injects the third harmonic component in the ac side. The negative-sequence reference voltage components of the invertere_{dn}^{*} and e_{qn}^{*} are controlled similar to positive-sequence components in the negative synchronous rotating frame as

$$e_{dn}^{*} = -x_3 - (\omega L)i_{qn} + v_{dn}. \quad (7)$$

$$e_{qn}^{*} = -x_4 - (\omega L)i_{dn} + v_{qn} \quad (8)$$

Where v_{dn} and v_{qn} are d- q axes negative-sequence voltage components of the supply i_{dn} and i_{qn} are d-q axes negative-sequence current components of the inverter, respectively. The control parameters x_3 and x_4 are controlled as follows:

$$x_3 = \left(k_{p2} + \frac{k_{i2}}{s}\right)(i_{dn}^{*} - i_{dn}) \quad (9)$$

$$x_4 = \left(k_{p3} + \frac{k_{i3}}{s}\right)(i_{qn}^{*} - i_{qn}) \quad (10)$$

The reference values for negative-sequence current component are set at zero to block the negative-sequence current from flowing through the inverter.

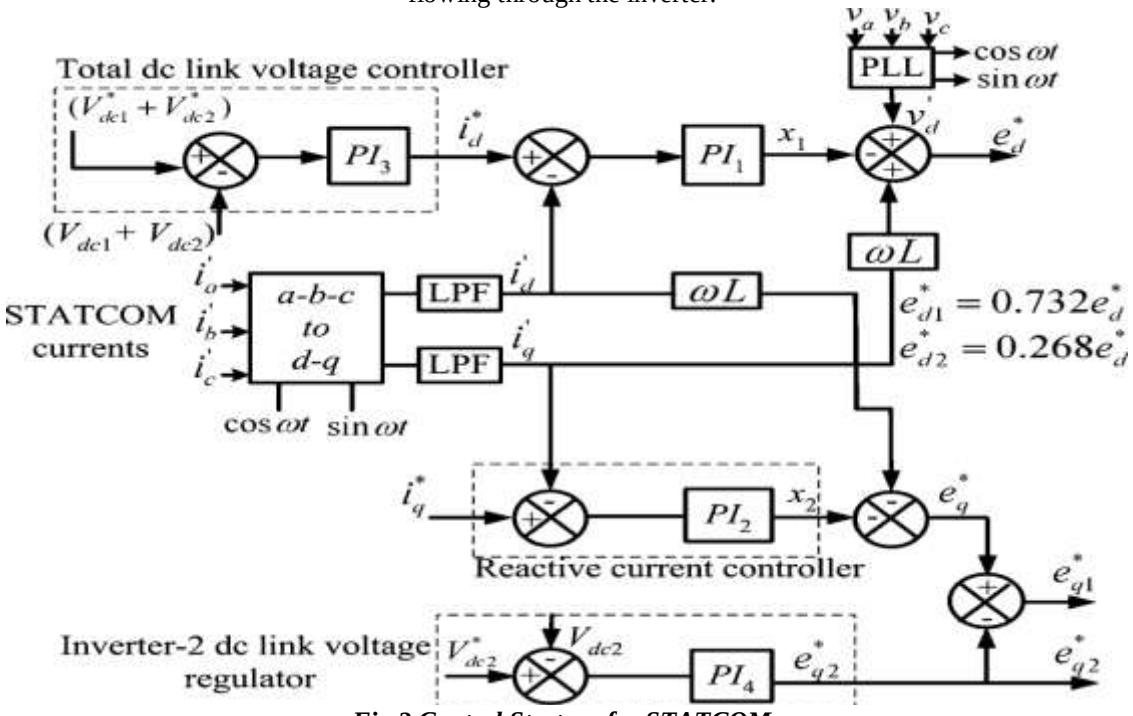

Fig.2.Control Strategy for STATCOM

B. CONTROL STRATEGY FOR SSSC

Fig.3. illustrates the control scheme employs in SSSC to produce the switching signal. The three phase grid voltages with supply voltage (400V) magnitude and with 120 degree phase shift with each other is compared with the load voltages. The signal obtained is used to produce the switching signals with the help of relay system i.e the signal is produced until its value is lower the actual rate. The inverted signals are produced to the remaining three switches.

$V_{ga} = V_L \sin(\omega t)$ (11)

$V_{gb} = V_L \sin(\omega t - (2\pi/3))$ (12)

$V_{gc} = V_L \sin(\omega t + (2\pi/3))$ (13)

Where $V_1 V_2$ and V_3 will be the switching signals for upper arminverter 1&2whereas $V_{01} V_{02}$ and V_{03} are the inverted signals which will be the switching pulses for the lower arm of inverter 1&2.

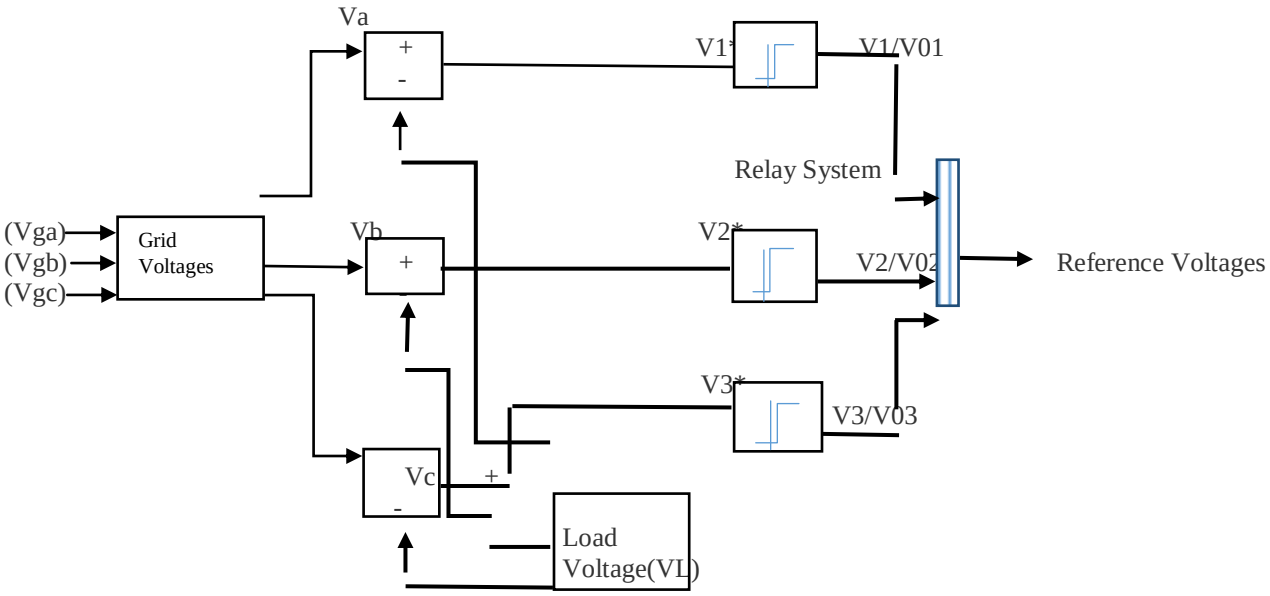

Fig.3.Control block diagram for SSSC

III SIMULATION RESULTS

The method is analyzed in MATLAB for various operating conditions, the switching pulse are produced by sinusoidal pulse width modulation technique. The results of the switching signal for the respective carrier and reference wave is shown in figure.6 as it is seen from the control scheme which is employed for STATCOM the necessary for the conversion of three phase quantity into two phase. It is done through park transformation (synchronous reference frame). The transformation is used to convert grid voltages, STATCOM currents and for load currents. Fig.5 shows the simulated result of d-q transformed signal from the three phase signal. It can be seen that the quadrature axis current leads the direct axis current by 90 degrees.

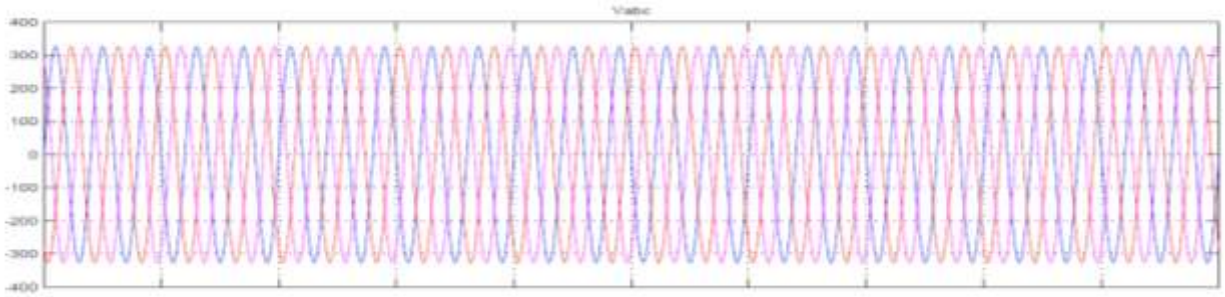

Fig.4 Three phase grid voltages(Va,Vb,Vc with 120^0 phase shift)

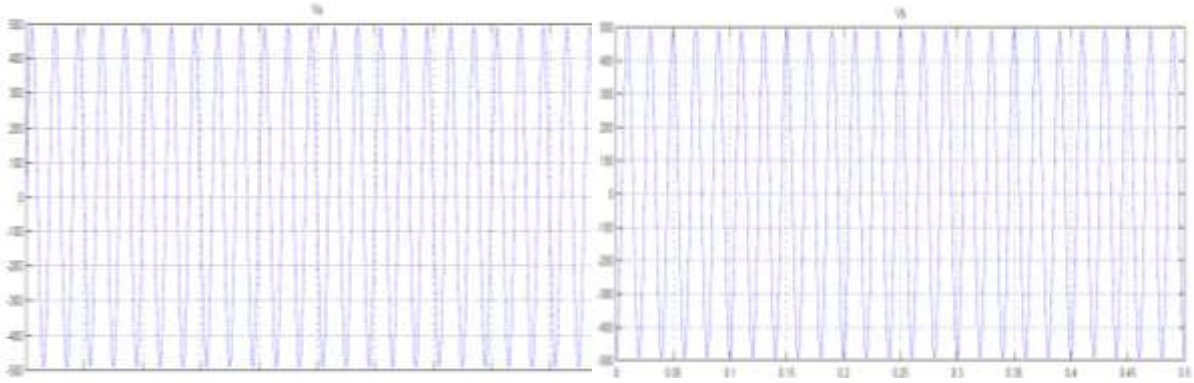

Fig.5: d-axis & q-axis component waveform after transformation

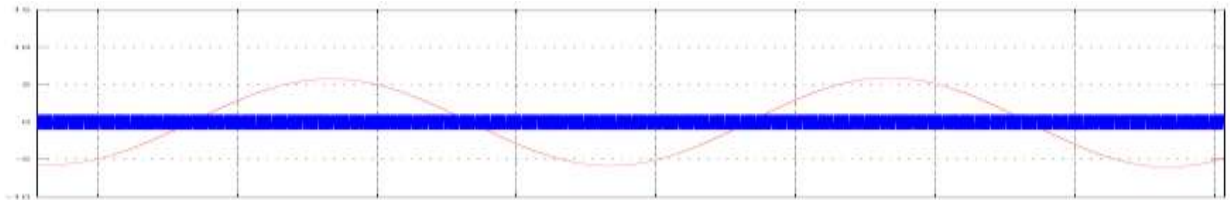

Fig.6 Reference sine waves and carrier triangular signal

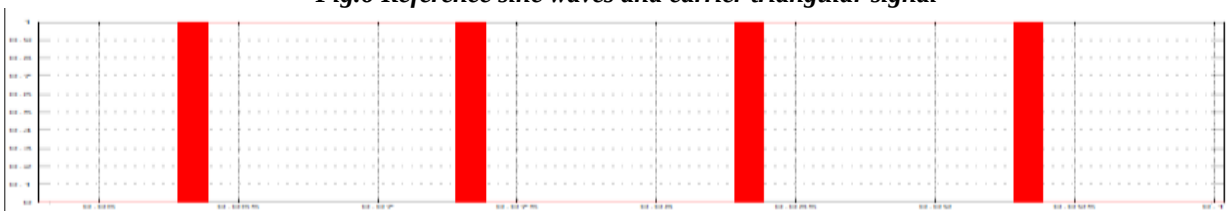

Fig.7. SPWM output

Following figure shows the cascaded multilevel inverter with IGBT switches. These switches are triggered by the above mentioned schemes. The inverter 1 DC link is 659V and inverter 2 DC link voltage is 241V. The total DC link voltage is maintained with respect to its reference values for smooth operation. The transformer high voltage endings are connected to the transmission line in series in case of SSSC. Whereas the neutral points are connected with each other in STATCOM.

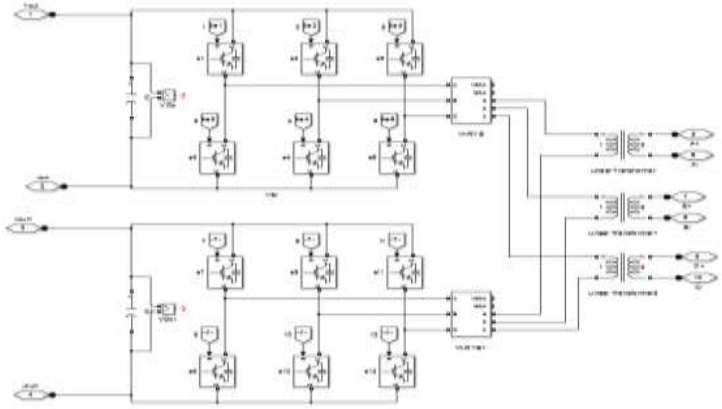

Fig.8. The inverter output of the CMI based STATCOM and SSSC

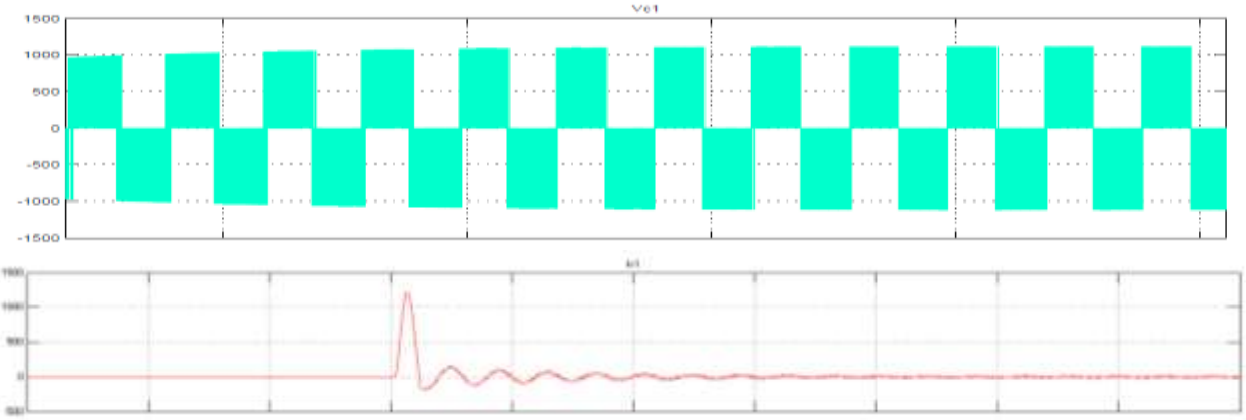

Fig.10 Inverter output voltage and current waveform

Loads that are used for analyzing the performance are non-linear load and reactive load (capacitive or inductive) with 5MVA capacity. For linear load the operation is checked for capacitive current lead and lag. For nonlinear load it is observed that the current and voltage are non-sinusoidal. The STATCOM injects current which compensates the current and the SSSC will

compensate the voltage. Fig.11 illustrate the cascaded multilevel inverter based STATCOM operation, for analyzing the STATCOM operation takes place at 0.15s of the total operation. This is done by a breaker with step time of 0.15s.

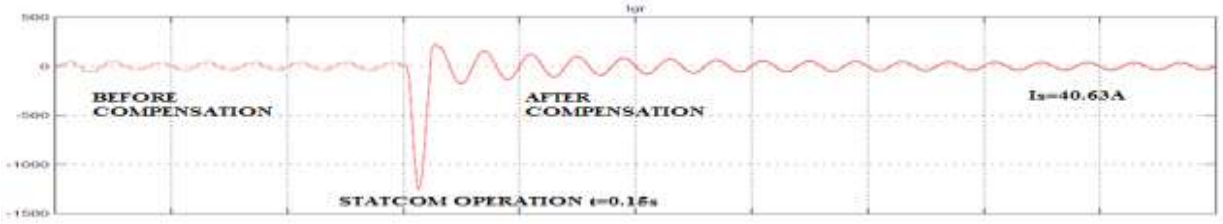

Fig.11: STATCOM operation source current compensation load

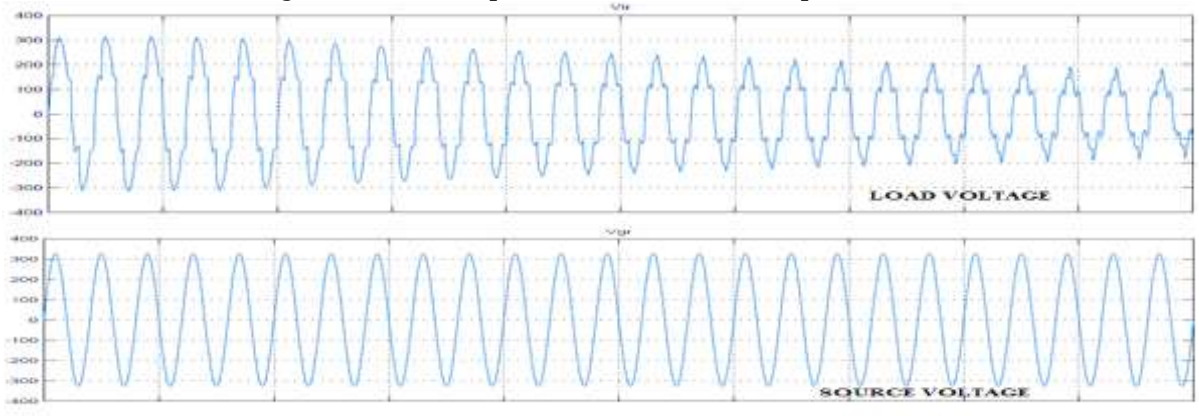

Fig.12: SSSC voltage compensation: load and source voltages.

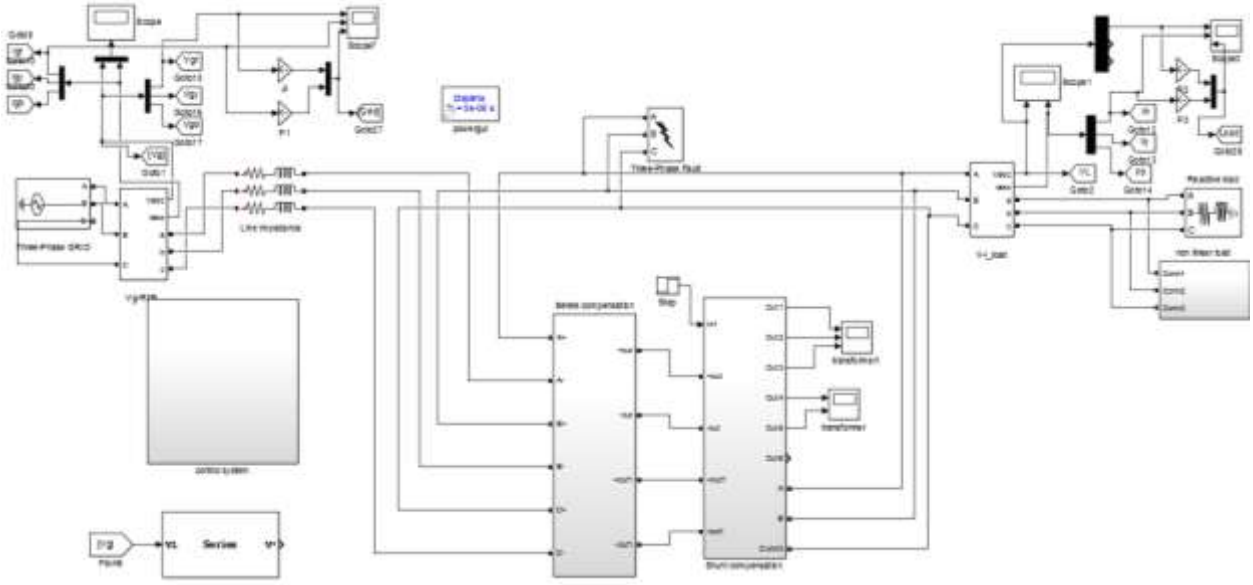

Fig.13:UPFC simulation diagram

Fig.13 is the overall simulation diagram of Unified Power Flow Control, the modification is done thus the reactive power compensation is done in both shunt and series. In order to validate the performance of the system with UPFC, the model is designed with the source modeling in MATLAB/Simulink and the experimental waveforms are obtained. The performance of the UPFC is studied under steady state condition. The performances of the existing and proposed methods are validated with the models to their efficiency conditions. The shunt control is by cascaded multilevel inverter based STATCOM, which will regulate the current. And the series compensation is done by cascaded multilevel inverter based SSSC, which is responsible for voltage compensation. A three phase fault is introduced at the time of 0.2s to 0.22s as shown in the circuitry

S.No	Parameters	Specification
1	Source voltage	400V
2	Supply frequency	50Hz
3	Inverter 1 DC link voltage	659V
4	Inverter 2 DC link voltage	241V
5	Carrier frequency	20Khz
6	Transformer rating	11KV/400
7	Rated power	5 MVA

Table.1.specification of UPFC Simulink

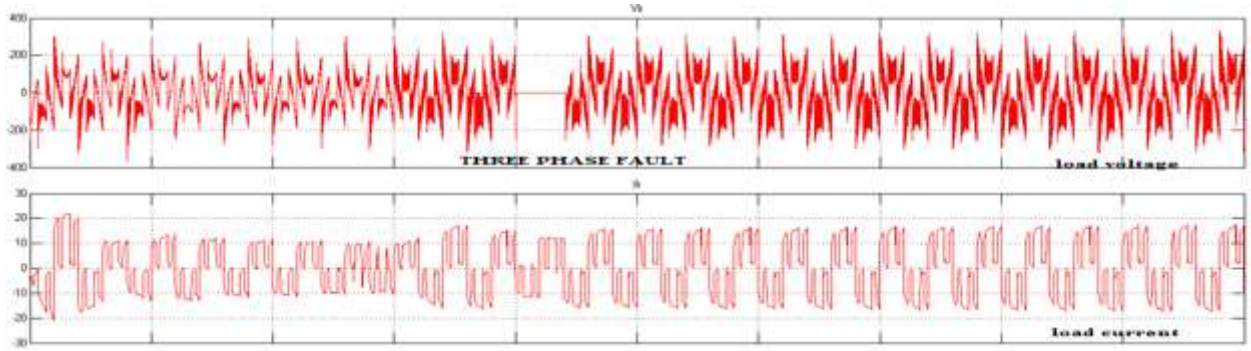

Fig.14. Load Voltage and Current waveforms under fault conditions

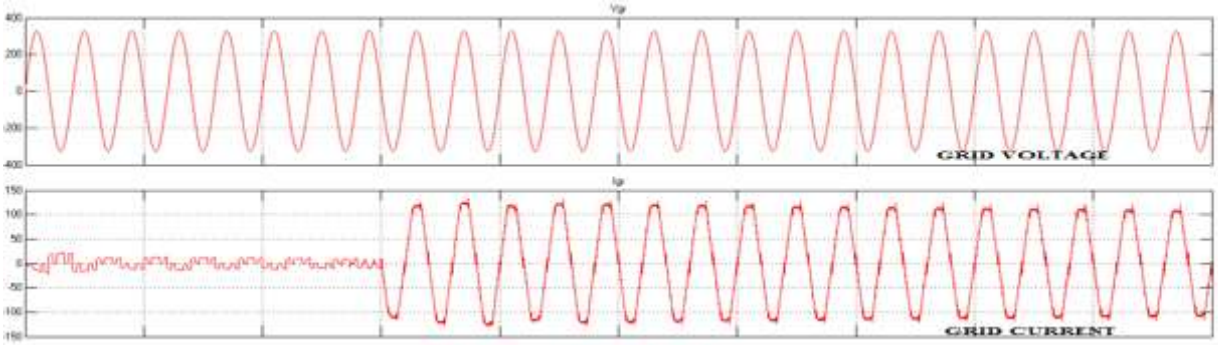

Fig.15 Voltage and Current waveforms after compensation

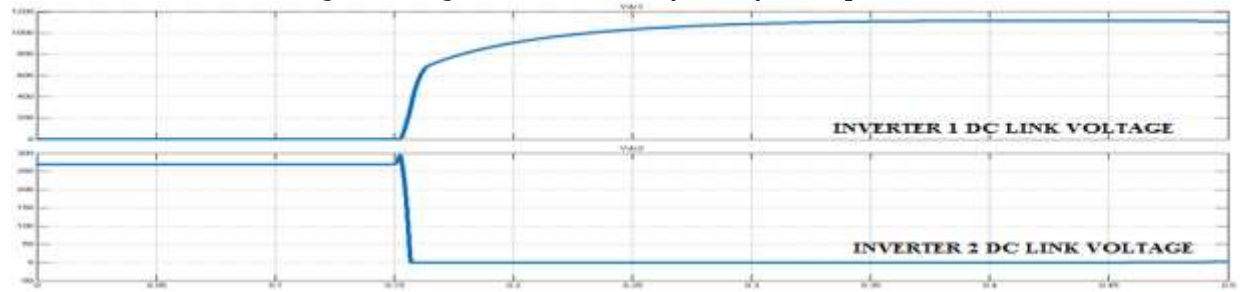

Fig.16.DC link voltage balancing

IV CONCLUSION

DC link voltage balance is one of the major problem in cascaded inverter based multilevel UPFC. A simple static unified power flow reactive compensating scheme using a cascaded two-level inverter-based multilevel inverter is developed. The bus voltage and real power flow in the transmission line is simultaneously controlled by SSSC, whereas the reactive power flow in the transmission line and load current is controlled and compensated by STATCOM. In this work the shunt

and series operation of FACTS controller working under load compensation and during the fault condition in the ideal transmission line network is analyzed using MATLAB/SIMULINK. The dc-link voltages of the inverters are maintained throughout the operation as expected. The simulation study is carried out to predict the performance of the proposed scheme under balanced and unbalanced supply-voltage conditions. The system behavior is analyzed for various operating conditions.

Future work is to be implemented as a transformer-less UPFC based on an innovative configuration of two cascade multilevel inverters(CMIs) since the conventional unified power-flow controller (UPFC) that consists of two back-to-back inverters requires bulky and often complicated.

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