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FPGA IMPLEMENTATION OF ENCODER and DECODER FOR GOLAY CODES

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Abstract- *This brief lays out FPGA implementation of encoder and decoder for Golay codes. Golay codes are error detection and correction codes and it corrects errors in the receiving end in the received data to reduce retransmission events . Encoding algorithm for both the binary Golay code(G23) and extended binary Golay code (G24) implementation based on cyclic redundancy check encoding method. Decoding architecture for G24(24, 12, 8) based on an error detection and correction method and here correction upto four erros is possible in the data. Synthesis and Simulation results obtained in Xilinx tool. Debugging FPGA design using XILINX Chipscope Pro tool.*

Keywords: *Architecture, Golay Code, Extended golay code, Encoder, Decoder, ChipscopePro, FPGA,VLSI Xilinx ISE tool.*

I.INTRODUCTION

Error correcting codes are Golay and Extended Golay codes. Representation of Golay code (G23) is (23,12,7) . By adding parity bits to the G23, Extended Golay code is obtained and it is represented as (24,12,8). Golay codes are perfect codes. Golay block codes are used in space mission, wireless transmission to enhance the system bit-errors-rate per unit time, Golay block code applied in transmission systems, low-power laser-ultrasound. In addition golay codes generate photo acoustic signal and for far field radiation pattern it provides cancellation of lobes. Electronic design automation technology is used for generating Golay codes to overcome this G24 is used. Error-detection and correction for Golay block(24,12, 8) code by using decoder. Decoder provides channel coding over transmission. To specify or design an error control code we have to specify the encoder, essentially error control code do takes k bits(message) and convert into n bits (n>k). To decrease power/bit, to detect and correct errors, encoder adds redundancy to the k bits this n bits sent through the channel to decoder and do FEC to obtain the message**.**

II.LITERATURE WORK

Golay [1] discusses a coding scheme for 23 binary symbols that allows us ,detect a maximum of three transmission errors. He proposed G23=(23, 12, 7) code whereas the extended Golay code is G24=(24, 12 ,8). Peng and Farrel [2] present the construction of Golay code by the direct sum of two binary codes involving 4 component codes. Two of which are simple linear block codes (repetition code and SPC code) and other two component codes are systematic and its modified version. The approaches uses the following construction and two (8, 4, 4) codes. Honary and Markaraian [3] proposed trellis decoder and simple encoder for golay code and generalized array codes (GACs) are used for encoding and decoding. Classon [4] give a hexacaode multilevel Golay encoder and hexacode Golay decoder to provide channel coding over transmission ,by using GF(4)= [0, 1, w, w^2] the hexacode characters are derived . Encoding methods are complicated in [2]-[4],hence unsuited for encoder hardware implementation. Weng and Lee [5] proposed converting message to code for G23 contain shift register , a combinational logic circuit that generates the parity bit in the transmitter, doubling the frequency, a five bit sequential circuit ,combinational logic. For electronic circuit as opposed to being done by a computer program of encoding process, shift register based CRC generation is preferred but drawbacks like long delays, rate of encoding is less for fast applications. Abbaszadeh and Rushforth[9] come up with one method of decoding named maximum likelihood decoding of coding system of binary numbers 0 or 1(L) of length n in the existence of noise model which mimics the random processes effect that occur in nature maps an arbitrary point **x** in R" onto that codeword **U** closest to **X** in Euclidean distance. Decoding Techniques [10]–[11],have been presented.

III.GOLAY CODE and EXTENDED GOLAY CODE

Golay codes and Extended Golay codes are linear block codes.(23,12,7) is representation of binary golay code, 23 bits is codeword length , data bits is 12 bits, two binary Golay codes should have minimum distance between them is 7.

Representation of Binary code is 0 or 1. Finite field consists finite no of elements and performs different binary arithmetic operations. To construct binary codes finite fields are required. To generate coding sequence polynomial is used. In this, characteristic polynomial and message with redundant bits allows long division process, so check bits are generated. Golay codeword(G23) generated and it has cyclic invariance. Check bits are appended with message bits the message gives the encoded Golay codeword(G24). Binary linear code is appended with parity bit for generation of Extended Golay code(24,12,8).Parity bit 0 appended if weight is even for binary linear code otherwise 1 appended.

IV.ALGORITHM,ARCHITECTURE OF ENCODERFOR GOLAY CODE and EXTENDED GOLAY CODE

A.Algorithm for Golay Encoder

STEP 1:For check bits generation we have to choose polynomial (12 bits)
STEP 2:For polynomial division process message bits(12 bits) are appended with redundancy bits(11 zeroes)
STEP 3:The result which is obtained by polynomial division process except first bit in the result remaining are check bits. Appending check bits with message bits gives G23
STEP4:For the conversion of G23 to G24,parity bit is added. Parity bit 0 is appended if G23 weight is even and 1 is appended if G23 weight is odd.

B. Architecture Of Encoder For Binary Golay Code And Extended Golay Code

Figure 1 shows M(x) 12 bits is given to MUX (0 as selection line) are stored in R1,the polynomial g(x) 12 bits stores in R2 performs binary XOR operation and stored in R3. The residual result obtained in the division ,circularly left shifted by no of leading zeroes in the result stored inR4. Here priority encoder detects the leading zeroes and gets left shifted by number of leading zeroes before '1' bit in the residual result. circularly left shifted result given to muxline(1). Figure 2 shows control loop mechanism for generating Golay codeword. The control subtractor input is p which performs bit wise or operation for priority encoder output ,if p=1 operation performs otherwise no operation and used for control loop mechanism .control subtractor one input is initialized with appended bits to the message that is 11 bits in long division process stored in R5.substraction performs for the control subtractor inputs and stored in R7.After result of subtractor is zero, result stored in R7 and R6 loaded with the encoded codeword of 23 bits when the result of subtractor is zero. The encoded codeword 23 bits stored in R6,counter counts the number of 1's and stored in R9[0]. R6' has 23bits appended with 0 and R6 "has 23 bits appended with 1. 2:1 mux select either R6' or R6"depending on R9 [0], which acts as the select line for the multiplexer. The encoded G24 stored in R[10].

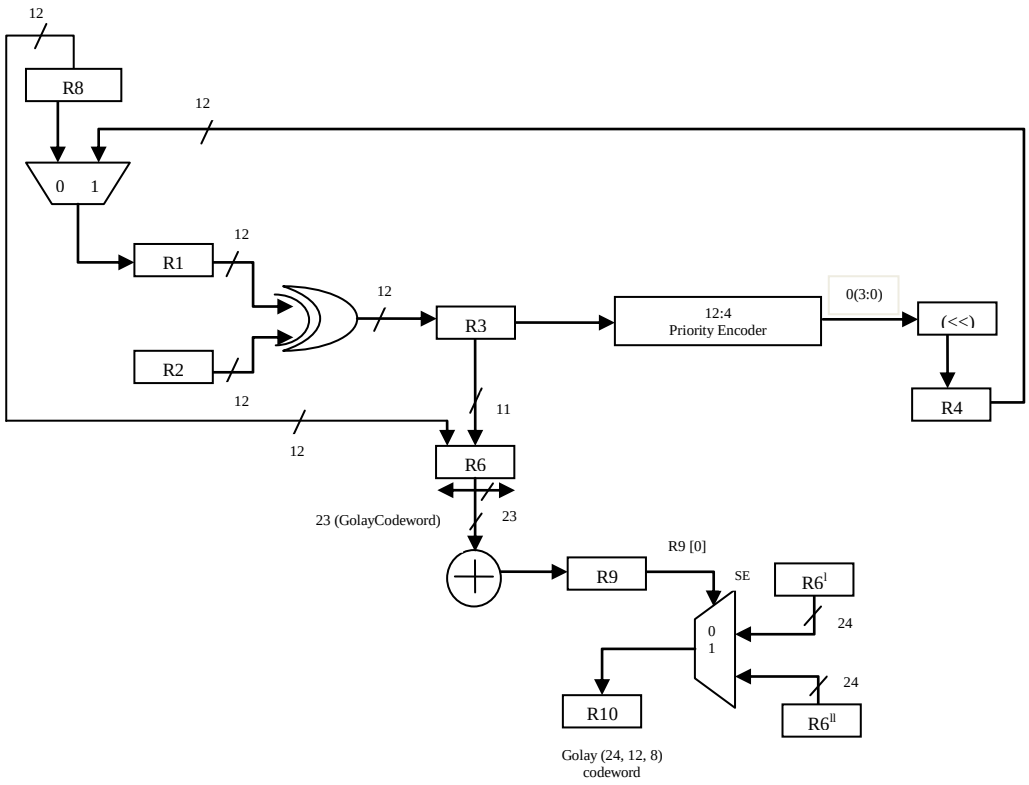

Figure 1.Architecture For Generating Binary Golay Code and Conversion Of G23 TO G24

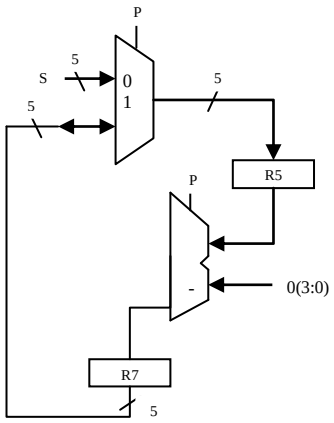

Figure 2.Iteration Control Unit

III. ERROR DETECTION and CORRECTION

Whenever a message is transmitted, message corrupted by noise or message get corrupted, so error detecting codes are used. For a message addition of redundancy bits ,during transmission of message helps to detect error this process named error detecting codes. parity check is example of error-detecting code .With error-detecting code, we send some data to know the original message from the wrong message that we received, this code named as error-correcting code. Error correcting code identify the exact position of wrong bit, by using parity check we identify the errors and wrong bit position. Once the wrong bit position is identified its Value changed from 0 to 1 or 1 to 0 to get the correct message.

A. Proposed Architecture Of Decoder For Extended Golay Code

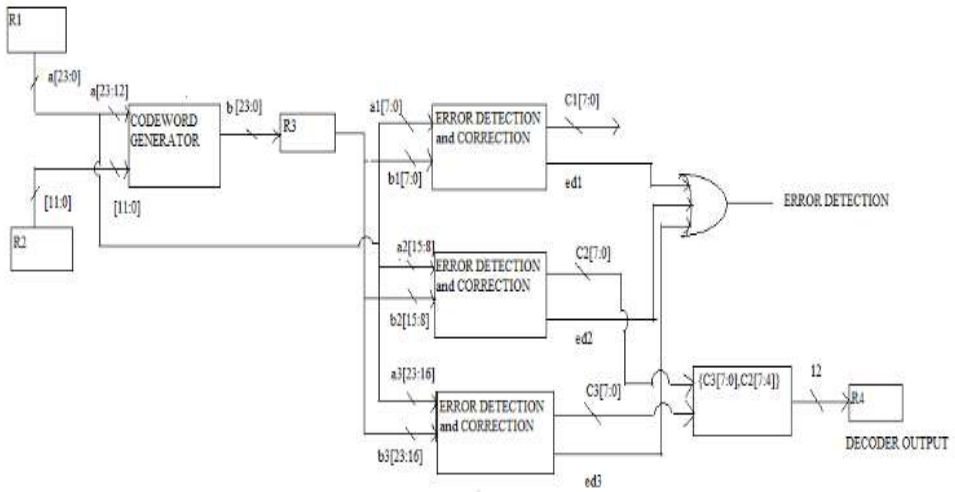

Figure 3.Architecture Of Decoder For Extended Golay Code

Figure 3 shows the encoded extended Golay codeword a[23:0] is one input stored in R1 and the polynomial[11:0] used for encoder is taken as other input stored in R2 these are inputs for codeword generator. By taking a [23:12] and [11:0] bits as inputs to codeword generator ,by using the logic used in encoder, generates final Extended Golay codeword b[23:0] stored in R3.For each error detection and correction blocks the given two inputs a1[7:0]b1[7:0],a2[15:8] b2[15:8],a3[23:16] b3[23:16],the outputs are c1[7:0] c2[7:0] c3[7:0] and ed1,ed2,ed3.Here, error detection and correction operation performs, the decoder output is obtained. To find detection and correction of errors at b[23:0].Error detection is done by comparing the given two inputs .Error correction is done by performing XOR operation of the given two input given to error detection and correction blocks , then parity bits generated c[7:0] ,and(&)

operation performs for parity bits c[7:0], if output is high at particular bit position of parity bits, then the particular b[7:0] bits position value is changed from 0 to 1 or 1to 0 to get the original codeword and finally decoder output is obtained. Here , decoder can correct upto 4 errors in the codeword.

IV.EXPERIMENTAL RESULTS

The Xilinx ISE Design Suite 14.2 utilized for aggregation and recreation for plan rundown blend report were done Xilinx Corporation. The principle parts in equipment many-sided quality outline as far as various rationale cuts and LUT's for fortified IOB's utilized and the standardized power utilization at 50 MHz clock recurrence. The usage of straight prescient coding is straight forwardly outlined in light of necessities more power reserve funds in utilization and equipment many-sided quality can be accomplished in view of ASIC or VLSI acknowledgment execution on Spartan-3E FPGA pack.

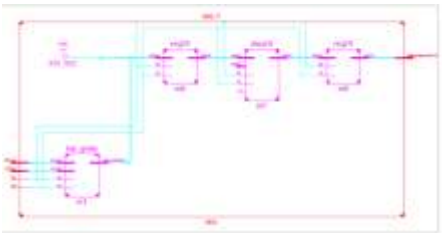

Figure 4. Rtl Schematic Of Encoder

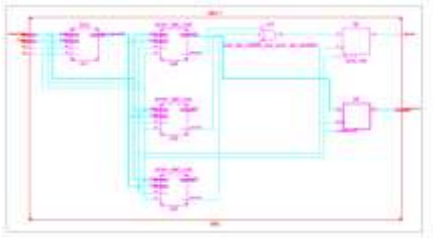

Figure 5.Rtl Schematic Of Decoder

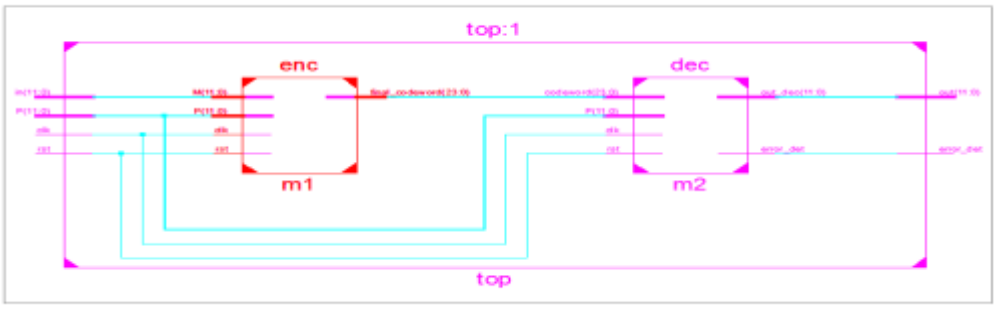

Figure 6.RTL Schematic Of Encoder and Decoder

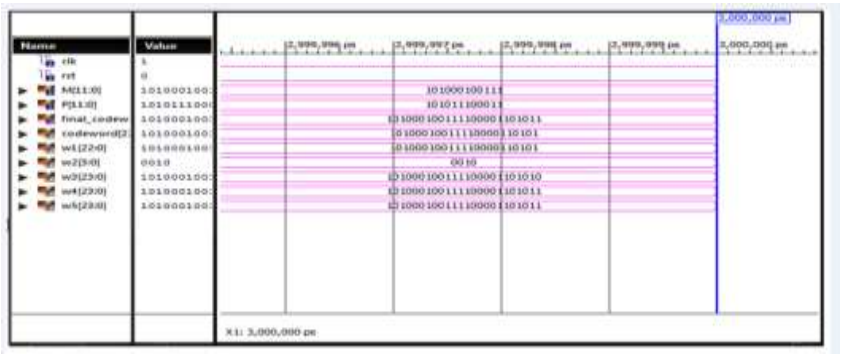

Figure 7.Simulation Result of Encoder For Generating GolayCode, Extended Golay Code

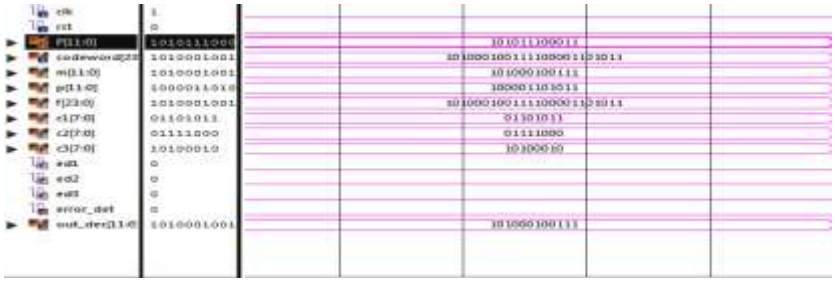

Figure 8. Simulation Result Of Decoder For Extended Golay Code

Figure 9. Simulation Results of Decoder For 2 Bit And 4 Bit Error Correction

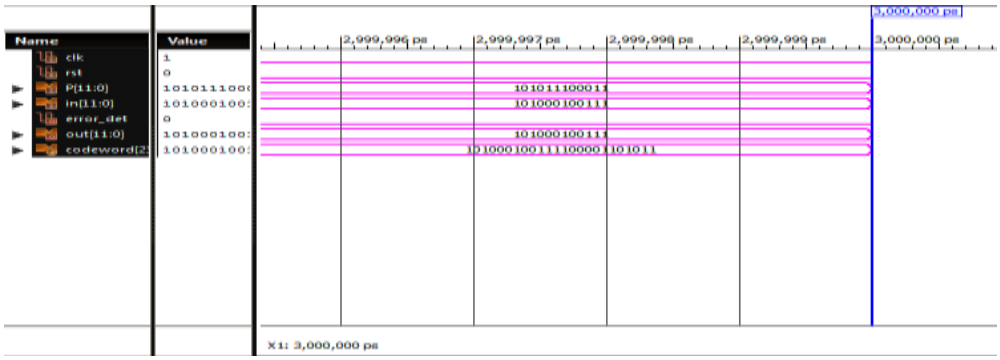

Figure 10.Simulation Result Of Encoder and Decoder

The simulation result of top module output gives Extended Golay codeword by using algorithm of encoder and decoder output obtained by using error detection and correction. Implementing on FPGA after loading the user defined variables and design constraints file using a chip scope pro technique and dumping in to FPGA after generating a .bit file and .ucf file and .cdc file after loading the FPGA pins into data sheet will be generated based on the inputs of data and outputs of an decoder. After completing the synthesis then compile all and implement, place and route then generate a bit file. Then bit file is loaded into spartan-3E kit in order to implement in chip scope pro .

Figure 11.Implementation Of Bit File On FPGA by Using CHIPSCOPE PRO

Green colour LED glow indicates that error is present in codeword , it shows error detection on Spartan- 3E FPGA by using Chipscope Pro tool.

Table 1. Design Utilization Of Encoder and Decoder

Device Utilization Summary (estimated values)			
Logic Utilization	Used	Available	Utilization
Number of Slices	1013	4656	21%
Number of Slice Flip Flops	1354	9312	14%
Number of 4 input LUTs	1346	9312	14%
Number of bonded IOBs	39	232	16%
Number of GCLKs	1	24	4%

Device Utilization Summary (estimated values)			
Logic Utilization	Used	Available	Utilization
Number of Slices	510	4656	10%
Number of Slice Flip Flops	684	9312	7%
Number of 4 input LUTs	665	9312	7%
Number of bonded IOBs	50	232	21%
Number of GCLKs	1	24	4%

The device utilization of area report on the design the more it takes place in ENCODER compare DECODER we can see in the results the consumption of an area. As well as the comparison Table 2. shown below with respect to timing and power reports also.

Table 2. Timing and Power Report

Result	ENCODER	DECODER
Timing report	4.134ns	4.040ns
Power report	0.081 watts	0.080watts
Total real time Xs to completion	15.00 secs	11.00 secs
Total real time Xst to completion	15.03 secs	10.96secs
Total memory usage	282104 kilobytes	266552 kilobytes

V. CONCLUSION

In this paper, Golay code correct errors in the receiveing end in the received data to reduce retransmissions ,decreasing the probability that the channel will get overloaded. So ,message bits given to encoder and adds redundancy bits to the message bits, to decrease the power/bit, to detect and correct errors. This message bits sent through the channel to decoder and do forward error correction to obtain the message.The program is dumped on FPGA by utilizing chip scope genius method on Spartan-3E FPGA pack keeping in mind the end goal to find the error detection of the codeword.

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