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DESIGN OF LOW NOISE AMPLIFIER FOR SEISMIC SIGNALS

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ABSTRACT:

This paper presents a comparative study of different existing Low Noise Amplifier (LNA) for Low frequency sensor ap-plication. The focus of this paper is on conditioning low frequency sensor signal like for biomedical signal acquisition, seismic wave alertness system etc, the design is more concentrated on some applications like seismic detection, where unpredictability and unknown nature of seismic signal is a concerned factor.

Typical single frequency LNA is required to operate with low noise, high gain and good linearity at 2.4 GHz. The design adopts feedback, and balanced topology to counter the problem of conventional LNA design which has difficulty in meeting the design specification

The Differential Difference Amplifier(DDA) architecture discussed here may be suitable for micro power sensor interface in scaled CMOS Technology.

Index terms*— Analog Front-end (AFE), Sensors, Amplifier Noise, CMOS Amplifier, Noise Efficiency Factor (NEF).*

INTRODUCTION

In last few decades, there has been a growing interest on low frequency signal conditioning for all kind of sensors and specially specially for biomedical, seismic applications [3]. In this kind of signal conditioning circuit architecture, a key element is Differential Amplifier which must able to amplify the low frequency signals detected by the sensor and reject the undesired noise. Different amplifier topologies can be found in literature to solve the challenging noise-power-area trade off [4]. Very often, the sensor signal bandwidth is low with additive noise. The amplifier noise is one of the most important parameter to be considered in design process. In this paper common LNA topologies suitable for low noise application such as Open Loop Network (OLN), Capacitive Feedback Network (CFN), Miller Integrator Network (MIFN) etc are reviewed, paying a special attention to the noise performance. Afterward, a Fully Differential Difference Amplifier(FDDA) architecture has been presented which could be a good solution considering the increasing of DC offset voltage and flicker noise is a serious problem in scaled CMOS technologies. The proposed FDDA has been designed and simulated in 180 nm standard bulk CMOS technology.

FEATURES OF LOW FREQUENCY SENSOR SIGNALS

To arrive at a proper topology, we need to investigate sensor signals and their attributes properly. So, the frequency and amplitude of low frequency sensor signals such as ECG, EEG, EMG and seismic signal etc are presented in Table I. In this table, LFP stands for Local Field Potential and AP stands for Action Potential. As our work is more focused to amplify seismic signal, commonly used commercial seismic sensors are also examined in Table II to understand the characteristics of the input signal of Analog Front-end (AFE) block.

TABLE I
FEATURES OF LOW FREQUENCY SENSOR SIGNALS [15]

Type of Signal	Frequency	amplitude
EEG	1-100Hz	1-10 V
ECG	5-500Hz	1-10mV
EMG	20Hz-1KHz	100 V-10mV
LPF	1Hz-500Hz	10 V-5mV
AP	300Hz-5KHz	10 V-5mV
Seismic	10mHz-100Hz	1 V-1mV

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COMPARISON TABLE OF PREVIOUSLY REPORTED FRONT-END AMPLIFIER FOR SENSOR APPLICATION

Parameters	[2] (2003)	[6] (2008)	[7] (2009)	[8] (2010)	[9] (2011)	[10] (2012)	[11] (2013)	[12] (2013)	[13] (2014)	[14] (2014)	[17] (2016)
Voltage Supply(V)	2.5	1.65	1.8	2	1.8	1	1.8	1.8	1.8	1.8	1.6
Technology (m)	1.5	0.35	0.18	0.35	0.11	0.13	0.11	0.35	0.18	0.18	0.13
Input Referred Noise ()	2.2	4.9	5.4	6.08	3.5	2.2	1	1	3.28	3.2	3.8
Gain (dB)	38.4	40	70	32	39.4	40	61	52	40.18	72	46
Bandwidth (Hz)	0.025-7.2K	0.1-20K	98.4-9.1K	-	10-10.2K	50m-9.5K	0.001-5.1k	0.1-6K	10.02K BW	0.2-6K	192-7.4K
CMRR (dB)	83	90	45	-	70.1	80	60	90	76	60	86
PSRR (dB)	85	80	50	-	63.8	80	70	78	80	76	75
Input Range (m)	12.3	-	2.4		5.7	1	0.9	-	-	-	3
Power Consumption (W)	80	-	41.55	8.3	7.92	12.1	1.18	8.1	4.10	7.02	1.92
NEF	4	8	4.9	5.55	3.35	2.9	1.9	1.84	4.37	3.08	2.19

TABLE IISPECIFICATION OF DIFFERENT TYPES OF SEISMOMETERS

Type of Seismometer (Pizoelectric Sensor)	Frequency Range (Hz)	Temperature (max)
Normal Seismomete (1)	0.2Hz-1.3KHz	80 ℃
Ultra Low Frequency Seismometer (2)	0.05Hz-450Hz	65 ℃
Ultra Low Frequency Dual Output Seismometer (3)	0.01Hz-350Hz	65 ℃

In Table II, the seismometer-(1), (2) and (3) are 731-207 seismic accelerometer low frequency vibration sensor, 731A seismic accelerometer ultra-quiet, ultra low frequency vibration sensor and 735T seismic accelerometer ultra-quiet vibration sensor with temperature output respectively.

AVAILABLE TOPOLOGIES FOR LOW NOISE AMPLIFIER

OLN TECHNOLOGY

An open-loop OTA is used in this approach to directly amplify the neural signal . The high-pass pole frequency is determined by an input decoupling capacitor C_i together with a resistor R_f which in turn sets the input common-mode voltage of the OTA. The low-pass corner frequency is again determined by the OTA response. In spite of its simplicity, the midband gain is subject to large variations since it is determined by the OTA DC gain. In addition, the noise contributed by the input resistor is directly amplified to the output and it may become dominant in the total input-referred rms noise. Hence, the achievable *NEF* value depends on the midband gain and the input decoupling capacitor (C_i). Roughly speaking, the lower the *NEF* value targeted, the larger the input decoupling capacitors required. Regarding the OTA implementation, it is convenient to have a β value close to unity in order to avoid a substantial signal attenuation at the input of the amplifier. Seeking to suppress the Miller multiplication of the input pair C_{GD} which would drastically increase the parasitic capacitance C_{pi}, the

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cascode amplifier of Figure 3d offers a good trade-off between input signal attenuation and output swing.

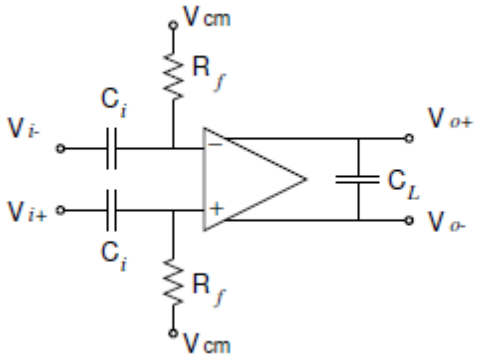

Fig. 1. Open Loop Network (OLN) Topology

CFN Topology

In this simple architecture, the high-pass pole frequency is obtained by the feedback resistor (R_f) and capacitor (C_f), whereas the low-pass pole frequency is determined by the OTA_1 response. The midband gain is given by the capacitor ratio C_i/C_f, as long as the OTA DC gain is much higher than M_{bq} (note that the feedback factor β can be approximated by the inverse of M_{bq}). Given that the required mid-band gains for neural applications are relatively high (M_{bq}~ 45 dB), cascode OTAs able to provide DC gains above 60 dB must be used. Under low voltage supply conditions, as it is typically found in neural recording interfaces, the use of telescopic OTAs is practically ruled out due to output swing considerations and, hence, folded-cascoded or current mirror topologies are conventionally employed at the price of considerably increasing the excess noise (η) and supply current (k) factors of the OTA [2,17,37]. For instance, assuming a differential ($\gamma = 2$) folded-cascode OTA topology as shown in figure, a transistor slope factor n around 1.8, and typical factors $\eta \sim 1.5$, $k \sim 4.4$, a *NEF* above 5.5 is obtained in this topology. Current scaling [37] and current splitting [17] techniques applied to the folded-cascode OTA, together with the use of degeneration resistances at the sources of transistors M_3 and M_4, have been proposed to reduce the *NEF* value.

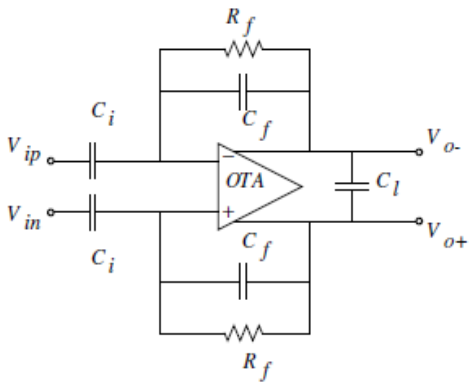

Fig. 2. Capacitive Feedback Network (CFN) Topology

MIFN Topology:

In this approach, the high-pass roll-off of the bandpass characteristic is implemented by an active integrator placed in a feedback path around OTA_1 [3]. The low-pass corner frequency is again determined by the frequency response of OTA_1, and the midband gain is directly given by the DC gain of this amplifier. This feature allows high midband gains without resorting to large capacitor ratios, however, strong variations in M_{bq} can be expected due to technology process deviations. Given that the DC gain requirements for both OTAs are not very demanding ($A_{o1} \approx M_{bq}$, $A_{o2} \gg 1$), simpler OTA topologies than in the CFN approach can be used. A good choice for OTA_1 is the cascode stage of Figure 3b which can obtain DC gains in the order of 50dB without impacting neither noise nor power consumption performance (in [3] a current mirror amplifier is employed). An even simpler structure can be used for OTA_2 as, for instance, the stage of Figure 3c.

figure plots the *NEF* of MIFN topology in terms of the transconductance ratio α, assuming practical values for the OTA parameters ($\eta_{1,2} \sim 0.7$, $k_{1,2} \sim 2$). As can be seen, a minimum *NEF* value of about 7.5 is obtained for α values around unity. Hence, the MIFN topology usually presents worst noise performance than CFN, mainly because of the power consumption requirements of the second OTA. A similar conclusion can be extracted for the area requirement since large C_i and C_l capacitors are required to keep the input-referred noise low (C_i amounts 35 pF). Further, a decoupling circuit must be used for

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blocking the dc offsets from the electrode-tissue interface.

For a particular application, it is extremely hard to compare and analyse the design trade offs in various topologies. One figure of merit that has been used widely as a part of research is Noise Efficiency Factor (NEF).

The mathematical expression of NEF defined as,

$$NEF = \sqrt{2I_{total}/(\Pi \cdot U_t \cdot 4KT \cdot BW)}$$

where Ut= KT/q is the thermal voltage, q is the electron charge, K is the Boltzmann's constant, T is the absolute temperature, is the total current consumption of the LNA and BW stands for its 3 dB-bandwidth. Note that this paper focuses exclusively on low noise amplifier design. So, flicker noise is also important factor in the noise characteristics of the amplifier, but it can be substantially reduced by using large transistor dimensions or chopper or auto-zero techniques.

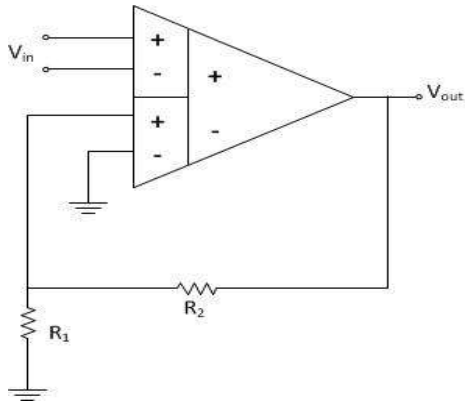
We are now in deep submicron region in CMOS technology where matching is a major problem due to scaling of the device. Therefore mismatch is critical factor in Common Mode Rejection Ratio (CMRR) of differential amplifier in any design specially in Analog Front-end Block. Other important factors are dopant variation and lithographic error with the technology variation. So, DDA is a suitable solution for realizing higher CMRR, which is most important parameter for the design of LNA in low frequency signal conditioning applications.

DDA

The Differential Difference Amplifier (DDA) is an emerging CMOS analog design building block. It is basically an exten-sion of the conventional operational amplifier. An operational amplifier employs only one differential input, whereas DDA has two differential inputs. Two voltage-to-current converters of DDA convert the differential voltage into the current, later these currents are subtracted and converted into voltage by current to voltage converter and amplified.

The mathematical expression of in figure 4 can be expressed as,

$$V_{out} = A_o[(V_{pp} - V_{pn}) - (V_{np} - V_{nn})]$$



Where, is the open loop gain of DDA. Similar to traditional operational amplifier operation, as → infinite, (−) = (−). Now, for finite open loop gain, the difference between the two differential voltage increases. Therefore, the open loop gain is required to be as large as possible to achieve better performance.

Reported Works on DDA:

J. Huijsing first introduced the DDA using CMOS tech-nology. Many basic circuits such as comparator with floating inputs, level shifter, instrumentation amplifier and resistor-less unity gain inverting amplifier using DDA have been realized by Sackinger and Guggebuhl [20]. The DDA attracted researchers due to its inherent high input impedances and requirement of less passive components for realizations of various circuits. Ismail et al. realized DDA based adder, substractor, multiplier, integrator, filters and phase lead-lag compensator [18]. Soliman et al proposed current feedback differential difference amplifier with constant bandwidth, in-dependent of the closed loop gain and with higher slew rate [21].

Most of the high performance analog integrated circuits incorporate fully differential signal paths. In 2001, Ismail et al. [22] proposed the fully differential difference amplifier. Fully differential architectures have several advantages over the single ended outputs. They provide a larger output voltage swing and are less susceptible to common-mode noise. Also, even-order non-linearities are suppressed in the differential output of a balanced circuit, which is symmetric with perfectly matched elements on the either side of an axis of symmetry.

However, the DDA has been discussed in very few literature, particularly for fully-differential applications. Here, internal circuit of FDDA and its transient response and AC responses are shown. The gain of the amplifier is 60 Db

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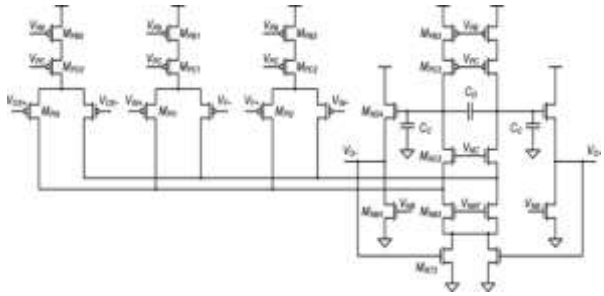
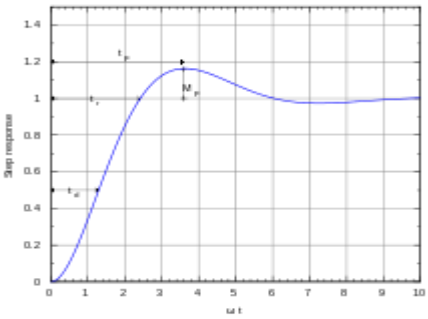
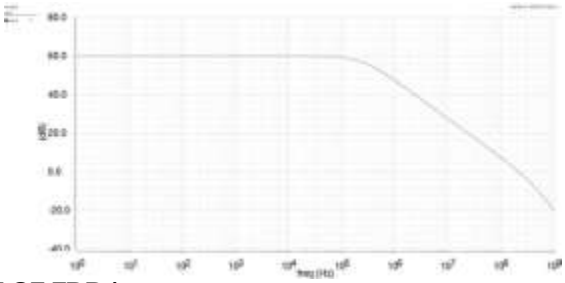


INTERNAL STRUCTURE OF DDA

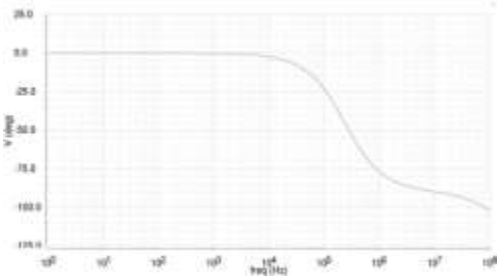
SIMULATION RESULTS



Transient Response of FDD



GAIN OF FDDA



PHASE OF FDDA:

CONCLUSION

The challenge of processing the low frequency sensor signal in the presence of noise is met by a specially designed very low noise Analog Front-end (AFE) amplifier. The DDA described in this paper has a near relation to the operating principle of many ordinary instrumentation amplifiers. Two differences must be noted that an ordinary instrumentation amplifier has an internally wired feedback and the closed-loop gain is adjusted by different gain factors of the transconductance elements, i.e., adjustable by the resistor. In contrast, the DDA described here is an open-loop device and hence more general than the instrumentation amplifier. It is a good solution for realizing higher CMRR, which is very important for design of LNA in deep submicron region in CMOS technology.

REFERENCES

[1] Gosselin B., *"Recent Advances in Neural Recording Microsystems,"* Sensors 2011, 11, pp. 4572–4597.

[2] R. R. Harrison and C. Charles, *"A low-power low-noise CMOS amplifier for neural recording applications,"* IEEE J. Solid-State Circ.,June 2003, vol. 38, no. 3, pp. 958-965.

[3] Perelman Y.and Ginosar R., *"An Integrated System for Multichannel Neuronal Recording with Spike/LFP Separation, Integrated A/D Conversion and Threshold Detection,"* IEEE Trans. Biomed. Eng. 2007, 54, pp. 130-137.

[4] W. Zhao, H. Li, Y. Zhang, *"A Low-Noise Integrated Bioamplifier with Active DC Offset Suppression"*, IEEE Trans. Biomed. Circ. & Syst.,Nov. 2009, pp. 5-8, .

[5] W. Wattanapanitch, M. Fee and R. Sarpeshkar, *"An energy-efficient micropower neural recording amplifier,"* IEEE Trans. Biomed. Circ. & Syst., vol. 1,Jun. 2007, pp. 136-147.

[6] Chae, M.; Liu, W.; Zhi, Y.; Chen, T.; Kim, J.; Sivaprakasam, M.; Yuce, M., *"A 128-Channel 6 mW Wireless Neural Recording IC with On-the-Fly Spike Sorting and UWB Tansmitter,"* In Proceedings of the IEEE International Solid-State Circuits Conference (ISSCC'08), San Francisco, CA, USA, 3–7 February 2008; pp. 146-603.

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[7] Gosselin, B.; Ayoub, A.E.; Roy, J.F.; Sawan, M.; Lepore, F.; Chaudhuri, A.; Guitton, *"A Mixed-Signal Multichip Neural Recording Interface With Bandwidth Reductionr,"* IEEE Trans. Biomed. Circuits Syst. 2009, 3, pp. 129-141.

[8] Shahrokhi, F.; Abdelhalim, K.; Serletis, D.; Carlen, P.L.; Genov, R, *"The 128-channel fully differential digital integrated neural recording and stimulation interface,"* IEEE Trans. Biomed. Circuits Syst. 2010, 4, pp. 149-161.

[9] Majidzadeh, V.; Schmid, A.; Leblebici, Y, *"Energy Efficient Low-Noise Neural Recording Amplifier With Enhanced Noise Efficiency Factor,"* IEEE Trans. Biomed. Circuits Syst. 2011, 5, pp. 262-271.

[10] Zhang, F.; Holleman, J.; Otis, B.P., *"Design of ultra-low power biopo-tential amplifiers for biosignal acquisition applications,"* IEEE Trans. Biomed. Circuits Syst. 2012, 6, pp. 344-355.

[11] Zou, X.; Liu, L.; Cheong, J.H.; Yao, L.; Li, P.; Cheng, M.Y.; Goh, W.L.; Rajkumar, R.; Dawe, G.; Cheng, K.W.; Je, M, *"A 100-Channel 1-mW Implantable Neural Recording IC,"* IEEE Trans. Circuits Syst. I Regul. Pap. 2013, 60, pp. 2584-2596.

[12] Chang, C.W.; Chiou, J.C., *"A Wireless and Batteryless Microsystem with Implantable Grid Electrode/3-Dimensional Probe Array for ECoG and Extracellular Neural Recording in Rats.,"*Sensors 2013, 13, pp. 4624-4639.

[13] Sepehrian, H.; Mirbozorgi, A.; Gosselin, B, *"A Low-Power Current-Reuse Analog Front-End for Multi-Channel Neural Signal Recording,"* In Proceedings of the 12th IEEE International NEWCAS conference (NEWCAS'14), Trois-Rivieres, Quebec, Canada, 22-25 June 2014.

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