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Design And Implementation of High Speed Scan-Hold Flip Flop based Shift Registers

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Abstract: *There has been a great increase in the number of electronic devices and the requirement of high speed design has been increasing exponentially. Here, thus the design of the flip-flop and the sequential logic devices has been a prime constraint in the overall speed performances. Thus to increase the overall speed performance of the flip-flip design, various methodologies have been proposed. The major shift registers used in various digital devices are Serial-In - Serial-Out, Universal shift registers has been developed. In our proposed work, we have proposed scan mode Flip-Flop and these flip-flop based Shift register design. The proposed modified design of the scan multiplexer based D Flip-Flip has been used for the implementation of various shift registers. Here, the Serial In Serial Out, Parallel In Parallel out, and Universal Shift Register design has been presented. Our proposed design is shown to have lower delay and minimize the gate count. The simulation has been done using Xilinx ISE 9.1 and Target device is to be SPARTAN 3E.*

Keywords: *High speed, D-Flip flop, Shift registers, Scan Flip Flop, Gate count, Propagation delay*

I. INTRODUCTION

Electronics market is leading the share of overall business day by day. The need of the high speed and smart devices has been increasing day by day. Thus, the electronics device requirement has been increasing day by day. Thus, to fulfill the needs and requirement of the fast evolving world, we need to introduce the high speed VLSI designs. The miniaturization, reduction in power consumption, reduction in propagation delay has been the hot research topics in the world. Various VLSI Experts and researchers have been working in this field.
Thus, the need of the sequential logic circuits has been in advent. Thus, conventional Flip flops cannot fulfill the requirements. We need to modify the design of D-Flip Flops for the reduction in the delay and power consumption. The various scan based D-Flip flop has been proposed earlier. The delay propagation error in the propagation and hold time need to be analyzed. In our work, we have been proposing the design based on the scan D- flip flops and the modes like Hold mode and without hold mode has been proposed. The design has been modified for the conventional scan flip flops by introducing the clocking techniques and thus speed has been shown to be reduced. We have presented the design of the scan D- Flip Flops and various Shift registers have been designed to compare the time delay with the conventional design. Thus 26.7% reduction in the delay is reported as compared to previous design [23].

II. CONVENTIONAL FLIP FLOPS & SHIFT REGISTERS

Various clocked gate D-Flip flops have been used conventionally. The “D flip flop” will store and output whatever logic level is applied to its data terminal so long as the clock input is HIGH. Once the clock input goes LOW the “set” and “reset” inputs of the flip-flop are both held at logic level “1” so it will not change state and store whatever data was present on its output before the clock transition occurred. In other words the output is “latched” at either logic “0” or logic “1”.

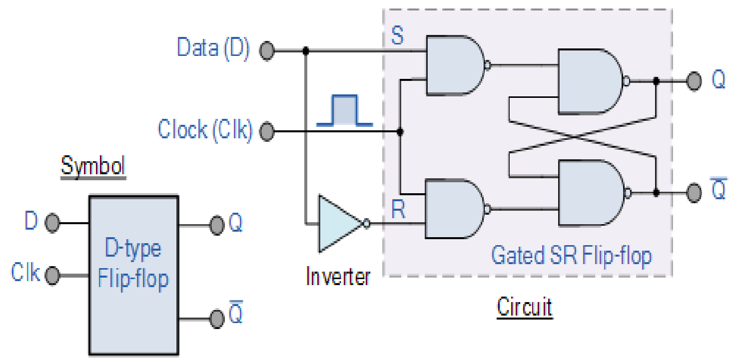

Fig.1 Circuit and diagram of the D-Flip Flop

Shift Registers are used for data storage or for the movement of data and are therefore commonly used inside calculators or computers to store data such as two binary numbers before they are added together, or to convert the data from either a serial to parallel or parallel to serial format. The individual data latches that make up a single shift register are all driven by a common clock (Clk) signal making them synchronous devices. Also, the directional movement of the data through a shift register can be either to the left, (left shifting) to the right, (right shifting) left-in but right-out, (rotation) or both left and right shifting within the same register thereby making it *bidirectional*.

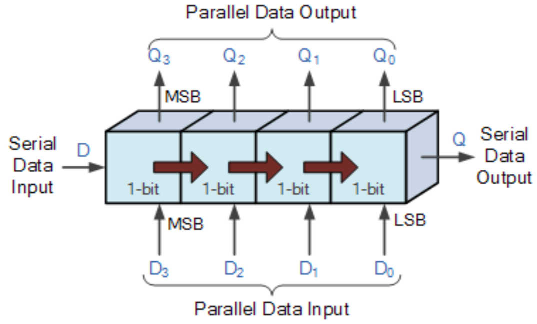

Fig.2 Logic Diagram of the Shift registers

III. SCAN BASED FLIP FLOPS

Scan flip-flops can be distributed among any number of shift registers, each having a separate scan-in and scan-out pin. Test sequence length is determined by the longest scan shift register. Scan chain is a technique used in design for testing. The objective is to make testing easier by providing a simple way to set and observe every flip-flop in an IC. The basic structure of scan includes the following set of signals in order to control and observe the scan mechanism.

1. Scan_in and scan out define the input and output of a scan chain. In a full scan mode usually each input drives only one chain and scan out observe one as well.
2. A scan enable pin is a special signal that is added to a design. When this signal is asserted, every flip-flop in the design is connected into a long shift register.
3. Clock signal which is used for controlling all the FFs in the chain during shift phase and the capture phase. An arbitrary pattern can be entered into the chain of flip-flops, and the state of every flip-flop can be read out.

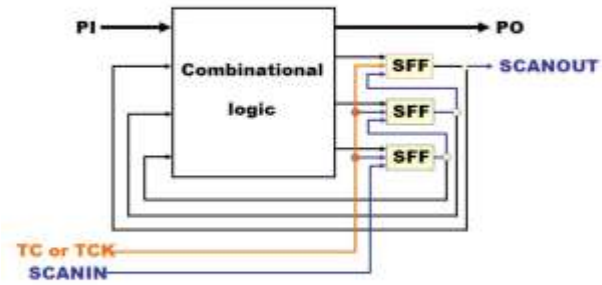

Fig.3 Logic Diagram of Conventional Scan flip flop

IV. PROPOSED DESIGN

A. Hold Mode Flip-Flop:

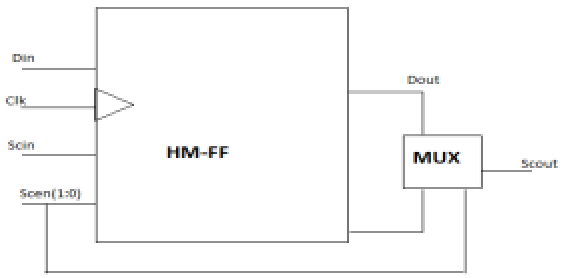

Fig.4 Proposed logic diagram of the Hold mode Flip flop

The Single clock pulse with Hold Mode (HM-FF) Flip flop is based on scan register and uses 4 multiplexers to form D-FF. The Single clock pulse with Hold Mode (HM-FF) .Flip Flop has one more input and one more output compared to other flip flop such as D-FF. Other than the Clock and Din (Data in), scan –enable (scen) exists. Scan-output (sout) is the additional output added. The internal logic provides the register to run in hold mode and it can bypass the register to directly drive the value of (scin). We have an additional multiplexer to multiplex scan out with the Dout.

B. With out Hold Mode Flip Flop

The Single clock pulse Without Hold Mode (WHMFF) Flip Flop is based on scan register and uses 2 multiplexers to form D-FF the Single clock pulse Without Hold Mode (WHMFF) Flip Flop has one more input and one more output as compared to conventional D-FF. Other than the Clock and Din (Data in), scan-enable (scen) exists. Scan-output (sout) is the additional output added. It is used to reduce the area overhead of the Single clock pulse with Hold Mode (HM) Flip Flop.

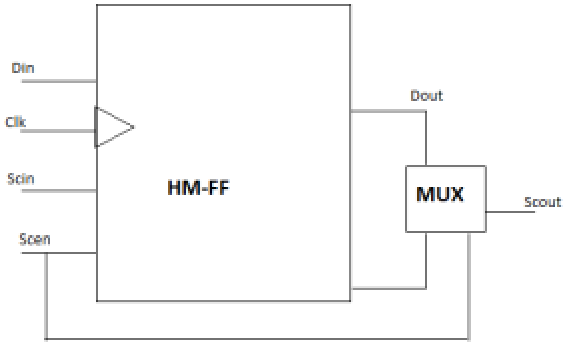

Fig.5 Proposed logic diagram of the Without Hold mode Flip flop

C. Shift Registers using HM-FF

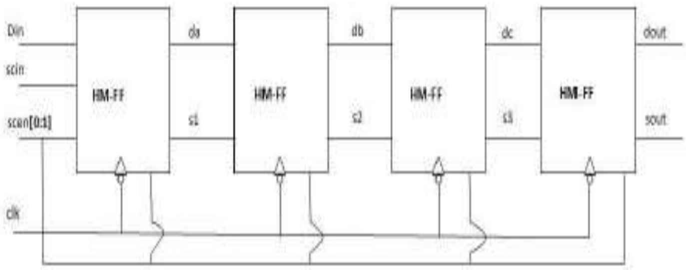

Fig.6 Proposed logic diagram of the Hold mode Shift register

In this proposed design, we have been using the input with scan enable and scan input and data can be shifted to the right. It consists of the input as hold enable for the architecture that can reduce the number of the gate count for its efficient design implementation. SISO register can be presented here. We have modified the scan out as shown if fig.4.

D. Shift Registers using WHM-FF

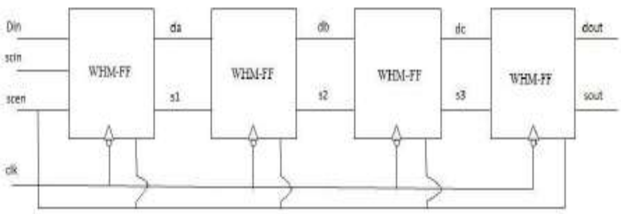

Fig.7 Proposed logic diagram of the Without Hold mode Shift registers

In this proposed design, we have been using the input with scan enable and scan input and data can be shifted to the right. SISO register can be presented here. We have modified the scan out as shown if fig.4

V. RESULTS & DISCUSSIONS

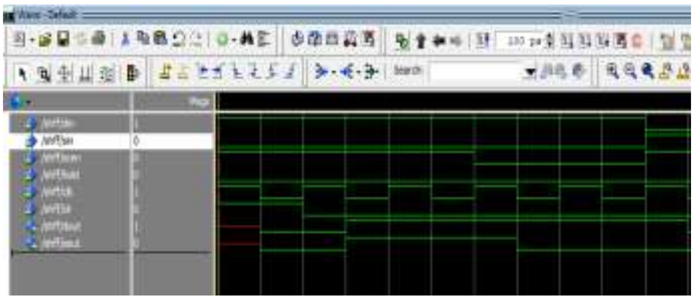
Fig.8 simulation result of the hold mode D-Flip flop

Figure 8 presents the simulation results of the D-flip flop using hold mode. The inputs are Din, Sin, Scen, hold and Clk. The output is Dout and Sout. Here, in the results, if Din = 1, Sin = 0, Scen = 1, hold = 0 and then we will get the Dout = 1, Sout = 1, but if hold = 1, Scen = 0, we will get the Sout = Sin.

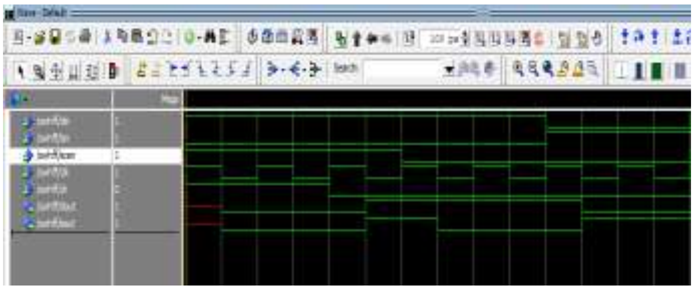
Fig.9 simulation result of the without hold mode D-Flip flop

Figure 9 presents the simulation results of the D-flip flop without using hold mode. The inputs are Din, Sin, Scen and Clk. The output is Dout and Sout. Here, in the results, if Din = 1, Sin = 0, Scen = 1and then we will get the Dout = Din, Sout = Sin, but if Scen = 0, Dout = Din and Sout = Dout.


Fig.10 simulation results of the hold mode Shift register

Figure 10 presents the simulation results of the shift register using hold mode. The inputs are Din, Sin, Scen and Clk. The output is Dout and Sout. Here, in the results, if Din = 1, Sin = 0, Scen = 1and then we will get the Dout = Din, Sout = Sin, but if Scen = 0, Dout = Din and Sout = Dout and the data shifts with every clock. Also, the Sout can simply bypass the input Data path and able to perform the direct data acess and thus reduces the delay of the propagation.

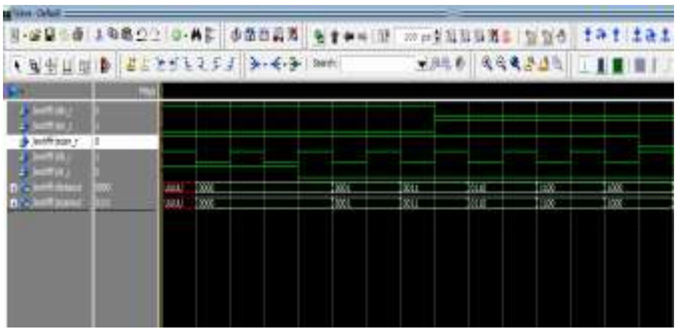
Fig.11 simulation result of the without hold mode Shift register

In figure 11, we have simulated the shift register without hold mode. The device has shifted the data as conventional register. But the scan enable in any time period, we were to scan the inputs to the next stage.

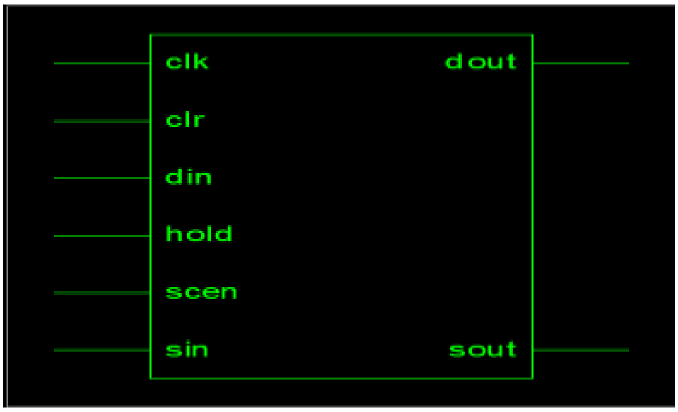

Fig.12 Block RTL of the hold mode D-Flip flop

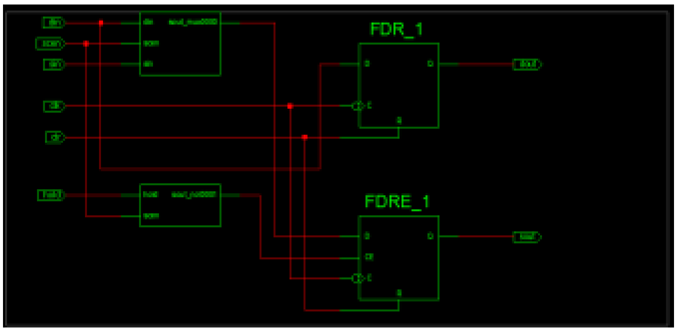

Fig.13 Detailed RTL of the hold mode D-Flip flop

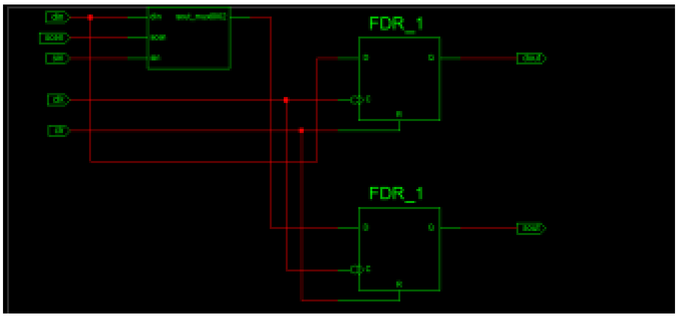

Fig.14 Detailed RTL of the without hold mode D-Flip flop

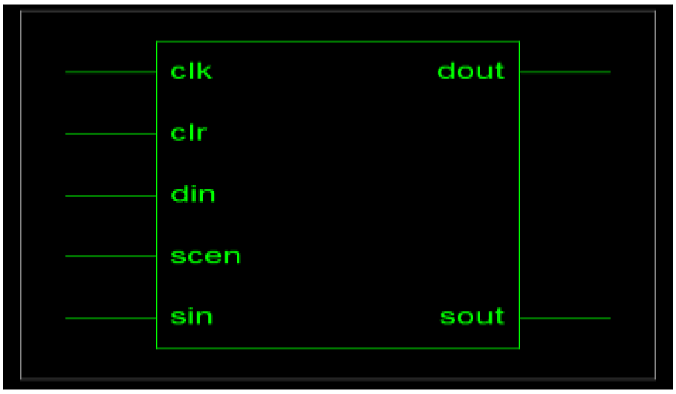

Fig.15 Block RTL of the without hold mode D-Flip flop

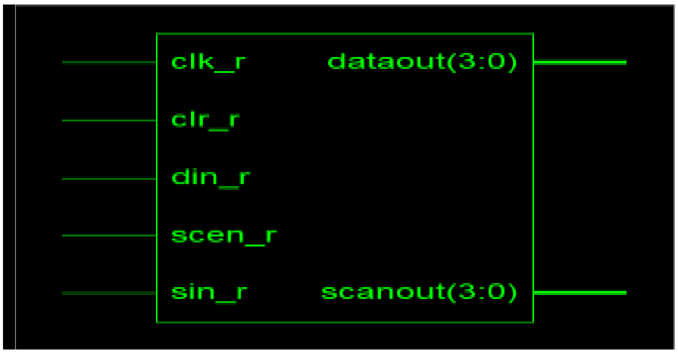

Fig.16 Block RTL of the without hold mode shift register

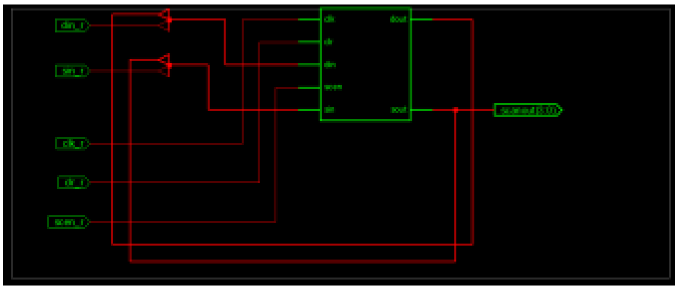

Fig.17 Detailed RTL of the without hold mode shift register

Fig.18 Block RTL of the with hold mode shift register

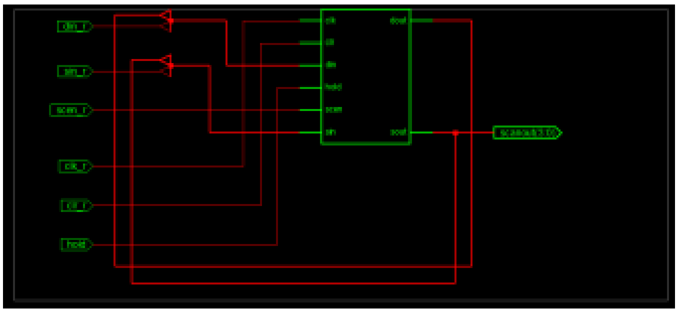

Fig.19 Detailed RTL of the hold mode shift register

```
                                 Gate     Net
Cell:in->out         fanout     Delay    Delay   Logical Name (Net Name)
----------------------------------------------   ------------
 FDR_1:C->Q               3     0.591    0.531   X3/dout (X3/dout)
 OBUF:I->O                      3.272            dataout_2_OBUF (dataout<2>)
----------------------------------------------
Total                           4.394ns (3.863ns logic, 0.531ns route)
                                         (87.9% logic, 12.1% route)
```

Fig.20 Delay report of the proposed shift register

In figure 20, we have shown the final delay of the proposed design. The total delay is shown to be 4.394ns as compared to the conventional design of the shift register [23] was reported to be 6ns. Thus 26.7% reduction in the delay has been reported here.

VI. CONCLUSION

Thus, in this work we have presented an efficient design for improved performances and reducing the gate count by reducing the need of the extra input multiplexer. Also, due to modified architecture in the scan flip flop we have achieved a speed efficient design of the device. Thus, we have presented designs of the proposed architecture and the simulation results. Also, the delay report has been presented. Thus, we can show that our proposed design has achieved the delay of the 4.394 ns as compared to the 6ns in the previous design [23].

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