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Dual-DC-Port Asymmetrical 5-Level H-Bridge Inverter With PI,PWM&SPWM Technique

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Abstract– *Improving the harmonics performance of H-Bride multilevel inverter through different modulation techniques has been researched in recent times. Several solutions were proposed for it. For most heavy and medium voltage applications, five level invertersare most used due to many advantages and it is easy to develop when compared to higher level (7 or 9) inverters. There are several modulation techniques and most popular among them is Sinusoidal Pulse Width Modulation.(SPWM).Dual-DC-port asymmetrical 5 level multi-level inverter (DP-AMI) using a new pulse width modulation (PWM) scheme and SPWM technique has been proposed. In this paper, a MATLAB/SIMULINK analysis using PI,PWM and SPWM for a 5 level HB MLI with reduced power switches is presented.*

Keywords- *Multi-Level Inverter, Asymmetrical, Dual Dc Port, DPAMI, SPWM, H-Bridge.*

I. INTRODUCTION

Multilevel power conversion has been used since 1980s. The concept of a basic Multi level inverter (MLI) is to add up several D.C sources with proper switching sequence to the switches so as to obtain stepped waveform which resembles much to A.C waveform. Hence D.C to A.C conversion is performed. The advantage of such a method is that it reduces voltage stress on load and quality of voltage and current waveforms is improved.

For various power electronics applications, it is necessary for AC to DC transformations and vice versa. Inverters has been used for transformation for applications in high and low voltage cases. Design multilevel inverters with less switching complexity is very important for interfacing power semiconductor equipment's to high voltage circuits. The concept for multilevel inverter (MLI) began in 1975[1]. A three-level inverter topology was introduced by Nabae in [2].

Following are the advantages in multi-level inverter compared to two level inverters
1. Lower voltage stress in electronic switching
2. Reduced harmonic distortion
3. Versatility of working in fundamental and high switching frequency
4. Reduced electromagnetic interference
5. Improved efficiency
6. Ability to operate from renewable DC sources

In terms of operation, MLI can be categorized to Diode clamped, Fly back and Cascaded H Bridge.

Multi-level voltages are provided in diode clamped design through interlinking the phases with cascaded capacitor banks. For a configured level n, the number of diodes needed is

$$(n-1)(n-2)$$

With the increase in level n, more diodes are needed. It can be found from the above equation and it becomes infeasible [3].
Fly back design requires more capacitors for voltage clamping. The number of capacitors needed in this design is given as

$$(m-1)(m-2)/2$$

Cascaded H bridge MLI [4] has comparable advantage than diode clamped and fly back. It can provide more output levels at a reduced cost. The cost reduction is due to reduction in size and number of clamping diodes. Multi-step stair case voltage waveforms are provided with amplification at different levels. Due to it, necessity of voltage balancing is removed.

MLI are categorized to symmetric and asymmetric based in the DC source used. Symmetric used sources with same amplitude whereas sources with different amplitude are used in Asymmetric MLI. Higher voltage levels improve output power quality and increases the number of switching devices in addition to gate triggering equipment's. Also reducing the number of switching equipment has voltage level downsides. Many researches indicate low power quality output for this case. More output levels increase the circuit complexity and also reduces the efficiency levels. Thus, it becomes to reduce the number of switches for practical deployments.

Multilevel pulse width modulation inverters operating at high frequency have many switching problems resulting in common mode voltage and high voltage change rate at the motor windings. To solve this problem, power conversion using multiple small voltages has been introduced. Many recent high-power applications apply these converters. Multi-level concept has become very common due to recent advances in power electronics. Inverters are classified as two level or multi-level based on output voltage levels. Multi-level inverters have 3 or more voltage levels [8].

II. LITERATURE SURVEY

Inverters use diodes to control the voltage stress in electrical power devices.A novel operational mode is proposed in [11]. It is for diode clamped multilevel inverters. This operational mode was able to restrict the imbalance problem of dc link capacitors when operated in multi-level configuration.
A multicarrier sub harmonic pulse width modulation (PWM) scheme is proposed in [12]. Multiple voltage levels can be produced in this method. The voltage harmonic spectrum is also improved across difference frequency range in this approach.
T. Noguchi, et al., proposed a carrier-based closed-loop control technique. Switching loss is lower in this approach. The reduction is achieved through a concept of "no switching" zone.A pulse width modulation inverter with 5 levels was proposed by Suroso. The configuration included chopper circuits as DC current power source circuits. The performance is measured through computer simulation and experimental results. The solution is able to achieve an arm balancing control on voltage under all operation conditions. Impact of connected load to cascaded H-bridge converter on voltage regulation is studied by Farid Khoucha in [13]. The work concluded that voltage regulation is achieved in limited operating conditions.

A voltage balancing scheme using two active capacitorisproposed by Suroso in [14]. It uses circuit equation of flying capacitors. It is very effective on capacitor voltage regulation. Also, the work developed multilevel hysteresis current regulation strategies.
José Rodríguez proposed a new switching strategy considering multilevel cascade inverters. The solution is based on space-vector strategy. A voltage vector with reduced harmonic distortion and lower switching frequency is achieved in this method.
A new PWM technique for induction motor is proposed by J. S. Lai, et al.in [15]. The solution is based on six concentric dodecagonal space vector structures. A switching strategy for multilevel cascade inverters using space vector strategy is proposed in José Rodríguez.

A new technique for selective harmonic elimination pulse width modulation (SHE-PWM) is proposed by lhamiColak, et al., in [17]. The scheme works multilevel cascaded inverters.
A voltage regulation control strategy for multilevel inverters is proposed byJorge Pontt. The control strategy is based on switching patterns of switches based on polarity of output current.

Work in [18] by J. Selvaraj proposed a control strategy. It is able to decrease the common mode voltage.The approach is based on 3D space vector modulation (SVM). A multilevel SVPWM technique is proposed in [18]. The technique is based on switching sequence with 5 segment. The common mode dc voltage is balanced using half wave symmetrical PWM voltage waveforms.

Work in [9] surveyed different inverter structures. Both symmetrical and asymmetrical are considered in this work. The study is focused on reducing the number of switches. The study concluded that multilevel configuration is able to decrese the THD and voltage stress on switching devices. The study experimented sinusoidal pulse width modulation and modified square pulse width modulation for switching. Experiments confirmed that multilevel structure is able to reduce the total harmonic distortion at output voltages. Asymmetrical structure and symmetrical structure are able to provide same output voltage level for reduced number of switching devices in asymmetrical configuration. The harmonic distortion for 9-level asymmetrical and 7-level symmetrical are found to to 15.22 and 16.45%. The study proved that output voltage levels can eb maintained by reducing switching devices in asymmetric and symmetric topologies.

Work in [10] analyzed the impact of nearest level control modulation on series connected MLI. The proposed configuration was able to provide more output level compared to basic multilevel inverters. The performance of the configuration was tested in terms of total harmonic distortion for both symmetrical and asymmetrical configuration. Asymmetric topology was able to provide more levels in inversion compared to symmetric topology.

III.ADVANTAGES AND DISADVANTAGES OF DIFFERENTMULTILEVEL INVERTERS

3.1 Diode Clamped Multilevel Inverter:

Advantages:
Harmonic content reduced with increase in the number of levels and thereby necessity of filter circuit is avoided.

Disadvantages:
The number of clamping diodes increases with increase in number of output level.

3.2 Improved Diode Clamped Multilevel Inverter:

Advantages: The method is able to solve the voltage sharing problem occurring in in DiodeClamped Multilevel Inverter
Disadvantages: The number of clamping diodes increases with proportionally with output level.

3.3 Flying Capacitor Multilevel Inverter

Advantages: Increase in number of storage capacitors
Disadvantages: With increase in output level the number of storage capacitors increases and the solution becomes costly.

3.4 Cascaded H-Bridge Multilevel Inverter

Advantages: Avoids the need for flying capacitors and clamping diodes.
Disadvantages: With output level increments, the DC sources also increases.

IV.PROPOSED TOPOLOGY

Cascaded H Bridge multilevel inverter:

It is also a multi cell inverters. Multiple H-bridges are connected serially in this inverter. Identical dc sources with same value are connected in dc side and connected in series on ac side.Following DC sources can be connected to this inverter

1. Fuel cell
2. Ultra capacitors
3. Batteries.

The voltage produced by each H-bridge is added to get the total output voltage. Each cell produces three voltage levels (+,0, -) by joining dc source to ac output with varied switch arrangements. Totally four switches are used.

MPPT:

Wind turbines and photovoltaic (PV) solar systems use Maximum power point tracking (MPPT) technique. It is designed to maximize power extraction under all conditions.
The principles used in MPPT applies not only to solar power but also to sources with variable power such as optical power transmission and thermo photo voltage.

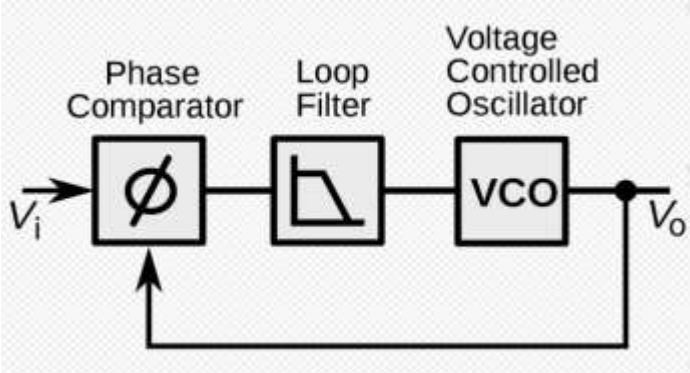
There are multiple different configurations of PV solar systems catering to inverter systems, external grids, battery banks or other electrical loads. The efficiency of power transfer in solar cell is dependent on the exposure of sunlight falling on pane and the electrical characteristics of load. In this exposure of sunlight varies over day time, MPTT is optimized to work on this condition to maximize the power transfer efficiency and optimize the system efficiency. The load characteristics is referred as maximum power point (MPP). MPTT is basically a process to find the MPP and keep the load characteristics at this point. Electrical circuits are designed to convert the voltage, current or frequency to suit the load characteristics. The problem of selecting the best load to be given to cells for maximizing the power out is solved by the MPTT.

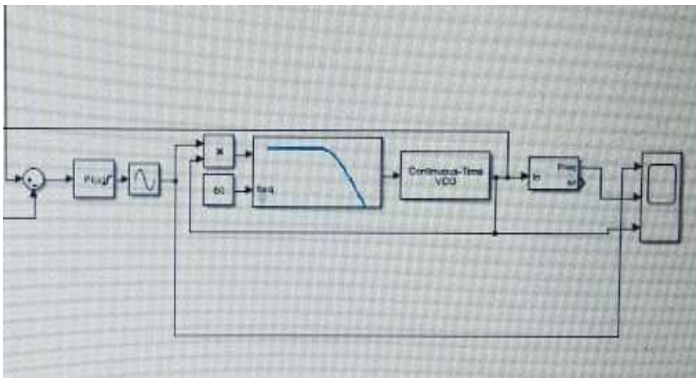
PI Controller:

PI (Proportional-Integral) controller is a mix of proportional controller and integrator. Proportional gain is offered by this controller. Fast error response is provided by this proportional gain. Zero steady state error is driven by the integrator.

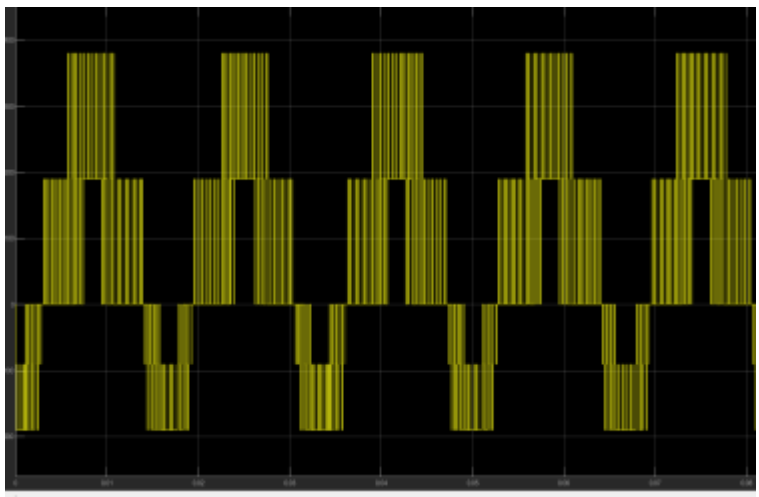
PLL:

An output signal proportional to the input signal phase is provided by the phase locked loop (PLL). There are different types of PLL and among them a circuit with variable frequency oscillator and phase detector in feedback loop is the simplest.
Oscillator generated signal is matched against input signal to keep synchronous phase.





The phase detector takes the input signal frequencyand matches against feedback frequency. An error DC voltage is given as output.. This voltage passes to a low pass filter (LPF). High frequency noises in the output is removed and a steady DV level is provided as final output by the LPF. The dynamic characteristics of PLL is given by Vf.



5 Level Simulations:

DC voltage magnitude from different source are varied in the asymmetric multilevel inverter. Two topologies are discussed in the following section which are capable of working in asymmetrical topology.proposed an optimal topology derived from the cascaded multilevel inverter. Unidirectional switches are used.It consists of 2n dc voltage sources (n is the number of dc voltage sources on each leg) and 4n+2 power switches for N level (22n+1 - 1). Voltage levels from positive to negative are provided as output. This topology includes the H-bridge structure within the main structure instead of keeping it separately thus minimizing the usage of two switches. Working The simultaneous switching ON of switches Sa and Sb should be avoided. It is to be noted that the DC sources connected on either sides have different polarity. As many of the multilevel inverters proposed now a days are derived from classical cascaded inverter, its comparison with those newly proposed is found to be essential. This basic topology consist of series connected H-bridges supplied from several DC sources.

SPACEVECTOR PULSE WIDTH MODULATION (SVPWM):

SVPWM modulation generate load as average or equal to reference load line voltage. It mimics a 3 separate push pull driver stages. Each phase waveform is operated independently.
The inverter is considered as single unit and it can be driven to eight unique states by the SVPWM. Through switching the state of the inverter, modulation is achieved. SVPWM is implemented by proper selection of switch state and switching duration.

Proposed Circuit:

The following proposed circuit topology is given below:

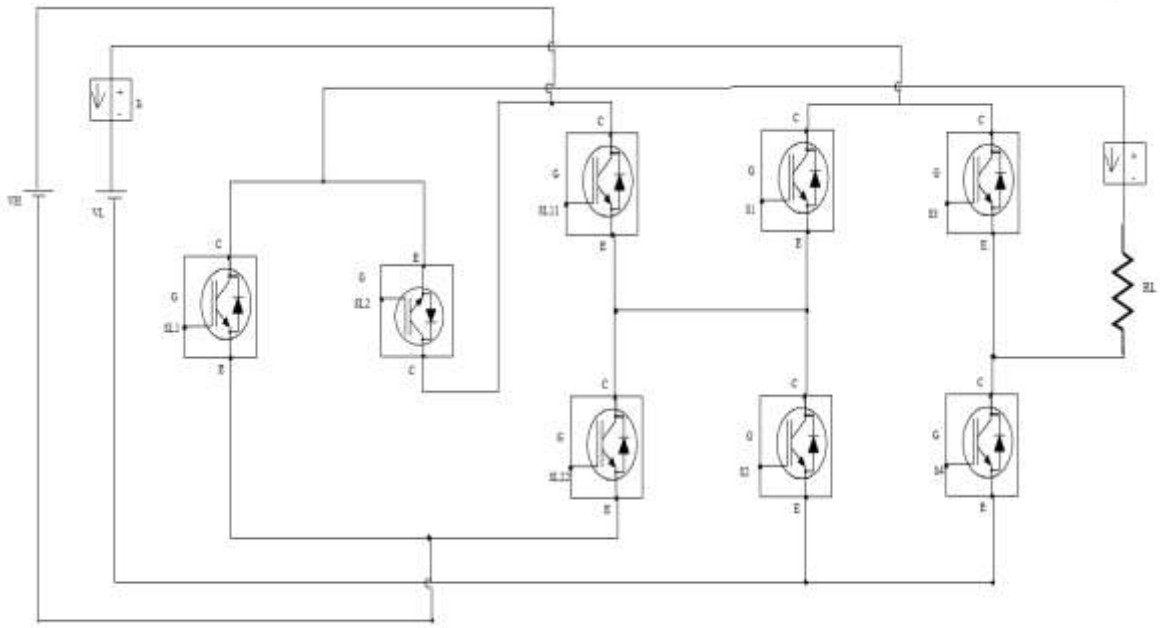


Fig 1. Proposed Circuit

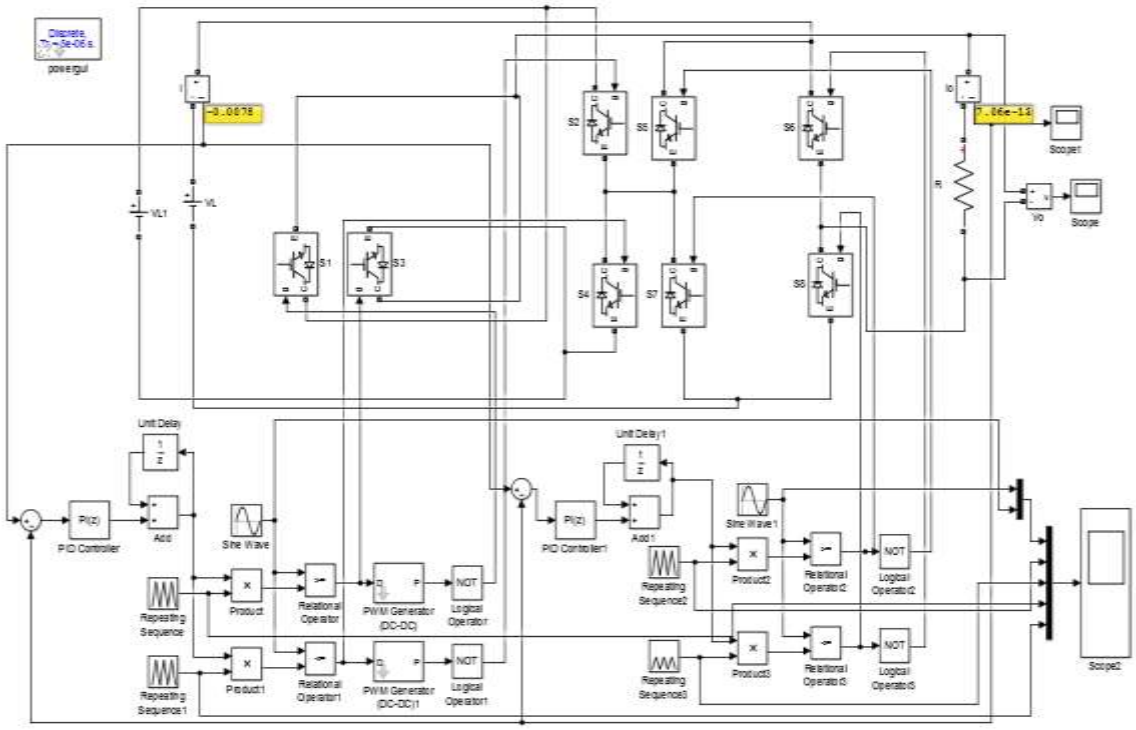


Fig 2. Simulink Model of Dual-DC-port asymmetrical 5 level multi-level inverter with PI,PWM& SPWM Technique

V.SIMULATION RESULTS

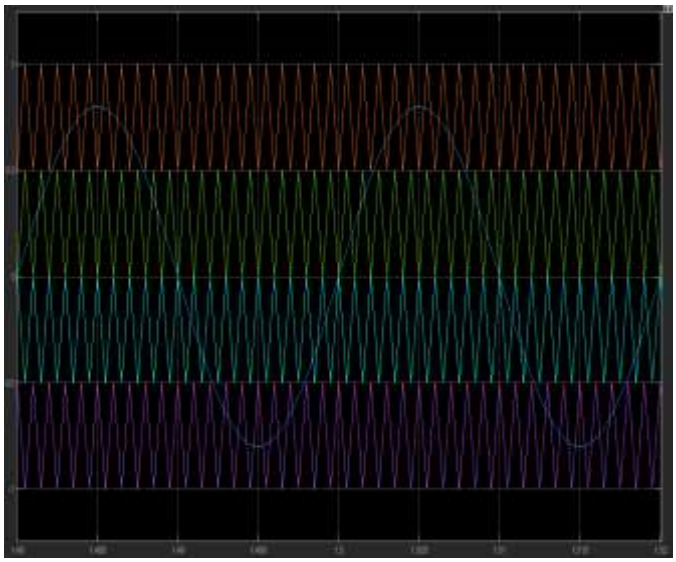


Fig 3. Five Level H-Bridge Inverter Output Waveform using PI,PWM and SPWM

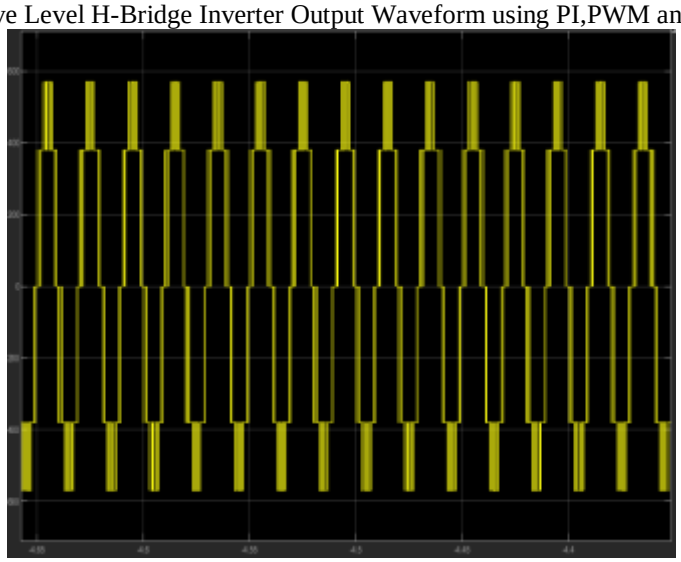


Fig 4. Five Level H-Bridge Inverter Voltage Output

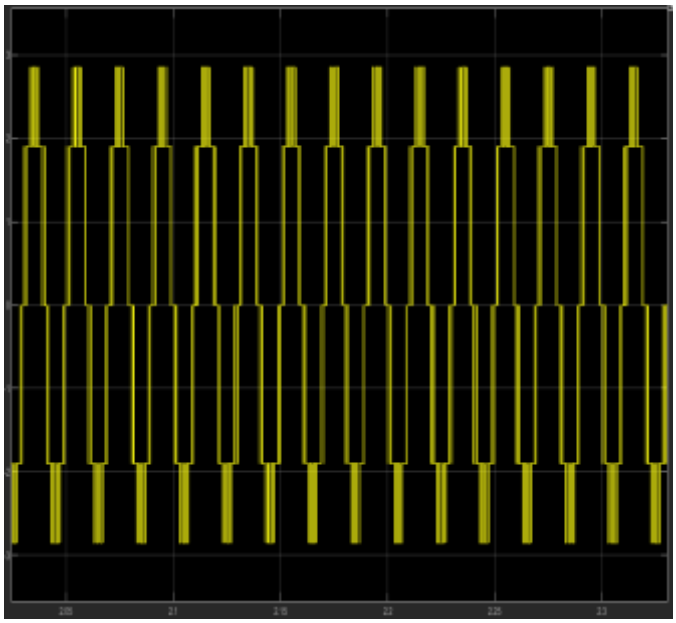


Fig 5.Five Level H-Bridge Inverter Output using PI,PWM and SPWM

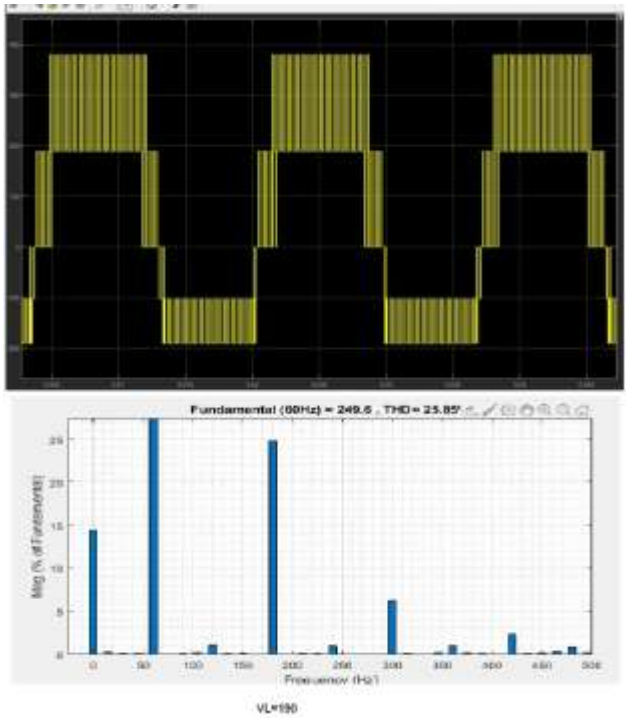


Fig 6. The Outputwaveform and Related THD=25.85%for VL=190V

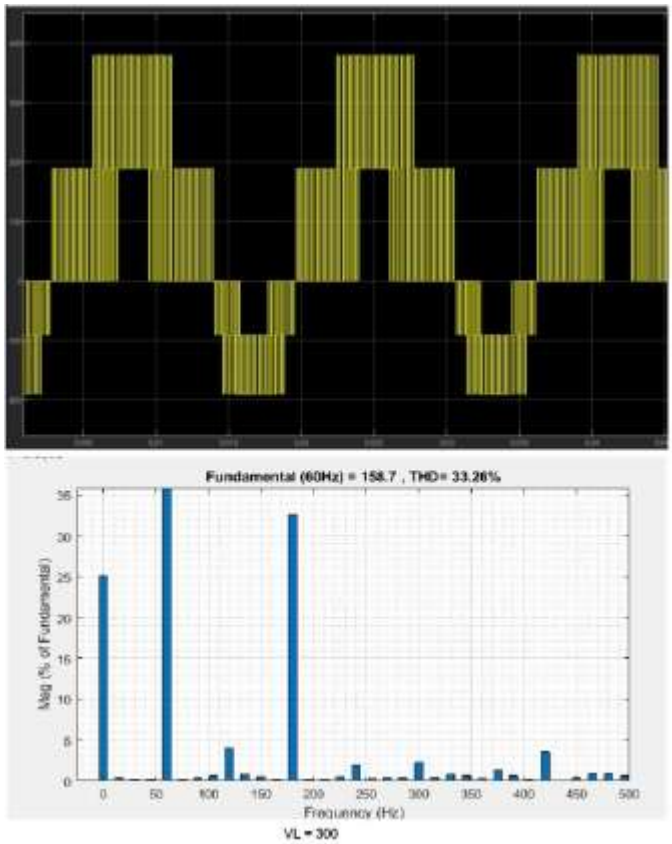


Fig 7.The Output waveform and Related THD=33.26% for VL=300V

VI.ADVANTAGES

- **Input current:** Can operate on low current without distortion.
- **Switching frequency:** Versatility of operating in different switching frequency with lower switching loss.
- **Reduced harmonic distortion.** Total harmonic distortion is reduced without any necessity for a filter circuit.
- **Staircase waveform quality:** Multilevel inverter produces low voltage change stress due to which problems due electromagnetic compatibility (EMC) are reduced.

VII.APPLICATIONS

- Multi range traction systems
- High power propulsion systems.
- In power filters
- Solar photo voltic cells
- Storage batteries

VIII. CONCLUSION

The output voltage is synthesized from several dc voltages as input. The performance of asymmetrical five level H-bridge multilevel inverter using PLPWM and SPWM is analysed in this work. The modified multilevel inverter topology proposed in this work can be used in industrial drive applications. The voltage and current level at each stage of the inverter is analysed. Different from existing conventional five level inverter witheight switches the proposed solution has only six switches, reduced switching loss, cost and circuit complexity. Also, the proposed work has reduced lower order harmonics.

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