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PULSE TRIGGERED FLIP FLOP DESIGN BY USING ADIABATIC LOGIC

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ABSTRACT: *In pulse triggered flip flop design there is the delay discrepancy in latching data "1" and "0", the design manages to shorten the longer delay by feeding the input signal directly to an internal node of the latch design to speed up the data transition. But Half of the injected energy from the power supply is dissipated in the PMOS network while only one half is delivered to the output node. (0 to VDD transition) Energy stored in the load capacitance is dissipated in the NMOS network (VDD to 0 transition). There are many methods to reduce power dissipation. Of all these methods Adiabatic logic is the efficient one to reduce power dissipation. In this document, the pulse triggered flip-flops are implemented using* ***Positive Feedback Adiabatic Logic****. By using the positive feedback adiabatic logic (PFAL) the power consumption can be reduced to an extent.The design was simulated was by using Mentor Graphics tool 180nm Technology,by using this the power will be reduced 13.034mw to 3.0372mw.*

Keywords: *Low power, flip-flop, CMOS, Adiabatic, PFAL.*

I.INTRODUCTION

The power consumption is important factor in modern VLSI design. The significant amount of the total power is dissipated over the clock system in any synchronous circuit. Latches and flip-flops are the radical storage elements that are employed in many digital designs. In any system, 30% to 60% of the total power is consumed by the clock distribution network and storage elements only. Hence, a notable portion of the chip area and power consumption are imparted by these flip-flops[1].

The term pulse triggered means that the data is entered onto the flip-flop on the rising edge of the clock pulse, but the output does not change the input state until the falling edge of the clock. These pulse triggered flip-flops(P-FF) are sensitive when the input levels change amid the clock pulse is HIGH. Hence the inputs must be set up before the rising edge of the clock and must not be changed until the negative edge of the clock. Otherwise, ambiguous results may appear.

A P-FF consists of a pulse generator and a latch. Pulse generator is used to generate strobe signals and latch is used to store the data. The P-FFs are similar to the master-slave flip-flops except that there is only one latch in former one whereas the latter one has two latches. Their internal construction consists of two sections. The slave section is basically the same as the master section except that it is clocked on the inverted clock pulse and is controlled by the outputs of the master section rather than by the external inputs. As the P-FFs consists of single latch, they are more prominent than conventional transmission gate and master-slave based flip-flops in high speed applications[2],[3].

The conventional pulse triggered flip-flops are described in section II. The fundamental principles of Adiabatic logic, different types of Adiabatic logics, and the P-FF designs based on Positive feedback Adiabatic Logic are described in section III. The simulation results for all the designs implemented using Pyxis Schematic Editor 180-nm technology are discussed in section IV.

II.BACKGROUND (OR) RELATED WORK

The P-FFs can be categorized into two types based on the pulse generator. First one is implicit type P-FF and the other is explicit type P-FF. In an implicit type P-FF, the pulse generator is a part of the flip-flop and the strobe signals are generated implicitly. As a result these type of flip-flops are more power efficient. But these flip-flops have a disadvantage that they have long discharging paths. Due to this the timing characteristics deteriorate[4].

In explicit type P-FFs, the pulse generator and the latch that stores the data are separate that is the strobe signals are generated externally. As the logic and latch design are separated these flip-flops consume more power. But this separation of logic and latch provide a unique speed advantage to these flip-flops. The power consumption can be reduced by sharing a group of flip-flops to a single pulse generator. These are more advantageous due to its speed and reduced circuit complexity. Hence in this paper, we will consider explicit type flip-flops only.

A)Conventional Explicit Pulse -triggered Flip Flop Design

Some conventional P-FF designs are reconsidered for providing comparison. In [4],explicit data-close-to-output flip-flop , the strobe signals are generated by using NAND gate and inverter logic based pulse generator. The latch design is in the form of semi dynamic true-single-phase-clock (TSPC) structure. The inverters I1 and I2 forms logic restorer circuit and hold the data that is stored in the internal. node X and the inverters I3 and I4 are used to latch the data. The main drawback of this circuit is the internal node X charges and discharges during every clock cycle that is the node X discharges when the clock is high even though the input data is always 1. Due to this switching power dissipation occurs and also glitches may appear at the output.

To overcome this drawback, many techniques such as conditional capture, conditional precharge, conditional discharge, and conditional pulse enhancement scheme have been proposed in[5][6]. P-FF employed with conditional discharge technique is represented in [4] [6]. It consists of an extra NMOS transistor MN3 which is driven by the Q-fdbk signal. Whenever the input data is HIGH and Q-fdbk is low the transistor MN3 is OFF and there will be no discharging path for node X at every clock cycle. Hence the switching power dissipation can be reduced and also the logic restorer at the node X is removed. It is replaced by a PMOS driven by inverter.

In [4], Static conditional discharge flip-flop is analyzed. The structure is same as that of conditional discharge flip-flop except that both the data and clock are interchanged in static conditional discharge flip-flop. It has static latch structure. Both conditional discharge and static conditional discharge P-FFs exhibit worst case delay due to the discharging path i.e., from the transistor MN1 to MN3. But the static conditional discharge P-FF exhibits longer data-to-Q delay compared to conditional discharge P-FF.

To overcome this drawback modified hybrid lath flip-flop is proposed in [4]. It consists of a weak pull-up transistor MP1 which is driven by the output signal Q. The node X is HIGH whenever Q is low. Instead of using pulse generator, the strobe signal is generated by an NMOS transistor which is driven by three inverters. It has a drawback that the node X is floating node in certain cases.

B)P-FF Design based on Signal Feed Through Scheme

All the conventional circuits that are mentioned former are compared with the P-FF based on signal feed through scheme. All these circuits face worst case when input data changes from 0 to 1. The circuit P-FF based on signal feed through scheme has three modifications when compared to the former circuits. First, a weak pull-up PMOS transistor MP1 is used. Its gate terminal is connected to ground so that the internal node X is always charged. This design represents pseudo-NMOS logic style. The main advantage of this design style is it provides high speed and low transistor count. The logic restorer at the node X is also removed.

Secondly, pass transistor logic is used i.e., a pass transistor MNX is used. It is controlled by the clock pulse. The input data D is directly leaded to the output Q so that the data-to-Q delay can be reduced. It refers to the signal feed through scheme. Third, the pull down network of the second stage is eliminated and the discharging path is provided by the pass transistor MNX.

The working principle of the P-FF based on signal feed through scheme is as follows. When the clock pulse is applied to MN3, and there is no change in the input data, then the output Q is same as the input data. It is due to the pass transistor MNX, which transfers the signal to the output without any delay. There is no discharging path for the node X as the transistors MN3 and MN1 are OFF. When the input data transition occurs from 0 to 1, the node X is discharged to ground through the transistors MN1, MN2, and MN3. When the node X is discharged, MP2 is on and Q becomes 1.

III.P-FF DESIGN BY USING ADIABATIC LOGIC

A)Adiabatic Principle

Full swing voltage CMOS logic styles have been most successful in terms of both technically and market share. The lower limit of the Switching power dissipation of a CMOS circuit with capacitive load is $C_L V_{DD^2}/2$ where as in Adiabatic circuits, the switching power dissipation is below this limit. The term "Adiabatic" explains the thermodynamic processes. These processes does not exchange heat with the environment. The power dissipation can be reduced only if the operation of the circuit is slowed down. The energy is recycled so that the total energy drawn from the power source is reduced. Hence these circuits are also known as reversible logic circuits [7].

In contrast, Adiabatic logic do not switch suddenly from 0 to VDD. In Adiabatic switching, the potential across the switching devices is maintained as small. It is possible by charging the capacitor from a time varying voltage source or constant current source. The overall dissipation in Adiabatic logic circuit is shown in the equation.

$$Ediss = 2(RC/T)CV_{DD}{}^2$$

There are different types of Adiabatic families [8]. One such type is Positive Feedback Adiabatic Logic (PFAL). It show minimum energy consumption when compared to other families. It consists of a latch made by two cross coupled inverters. The latch avoids logic level degradation on the output nodes. The general schematic of PFAL circuit is illustrated in [9]. The functional blocks are in parallel with the PMOS of the latch. PFAL uses four phase power clock. In Evaluate phase, the outputs are evaluated from stable input signal. During Hold stage, the outputs are kept stable and in Recovery stage, the energy is recovered by transferring the charge back to supply. Final stage is the Wait stage which is used for cascading[9].

B)P-FF Design By Using PFAL

The schematics of the various pulse triggered flip-flops based on positive feedback adiabatic logic are discussed below. Figure 5.1 illustrates the Explicit data-close-to-output flip-flop based on PFAL. It consists of Explicit data-close-to-output flip-flop and its complement are placed in parallel to the PMOS devices of the two back to back connected inverters. It constitutes positive feedback adiabatic logic. All the other Pulse triggered flip-flops are implemented in this similar fashion only and are illustrated below in this paper.

IV.EXPEREMENTAL RESULT

The performance of the proposed pulse triggered flip-flop designs are evaluated against the conventional designs. Figure5.7 illustrates the simulation result for Explicit data close to output flip. The sinusoidal signal is applied as a clock at a frequency of 10MHz. Similarly, all the other pulse triggered flip-flops are simulated at 10MHz and the results are tabulated in Table I. The results illustrate that the average power for P-FF based on signal feed through scheme has been reduced both for adiabatic logic and without using adiabatic logic. The target technology is the Mentor Graphics Pyxis Schematic Editor 180-nm technology.

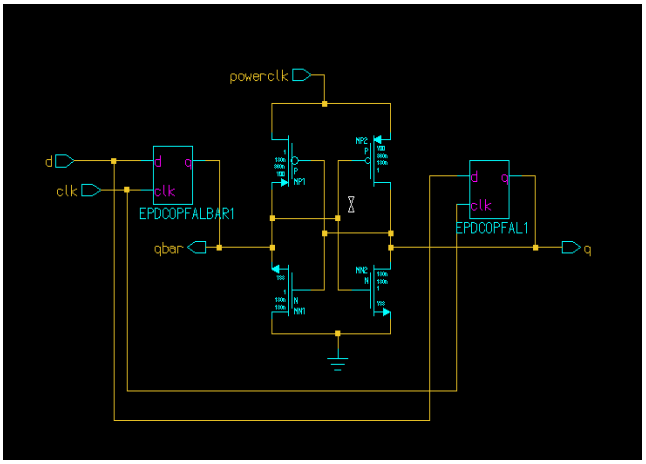

Fig5.1: EPDCO flip flop based on PFAL

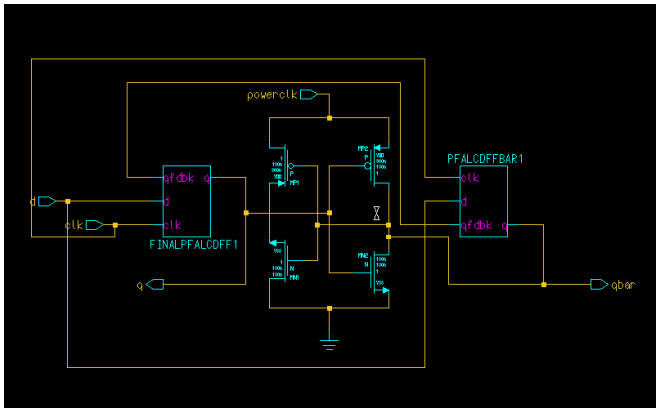

Fig5.2:CDFF Based On PFAL

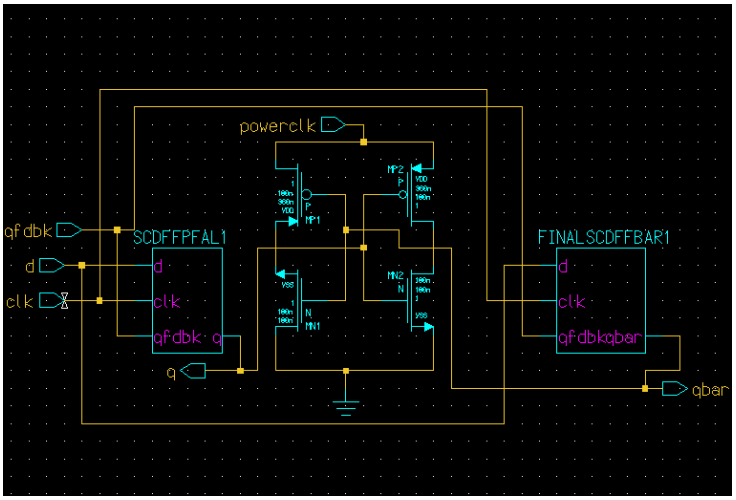

Fig5.3:SCDFF Based on PFAL

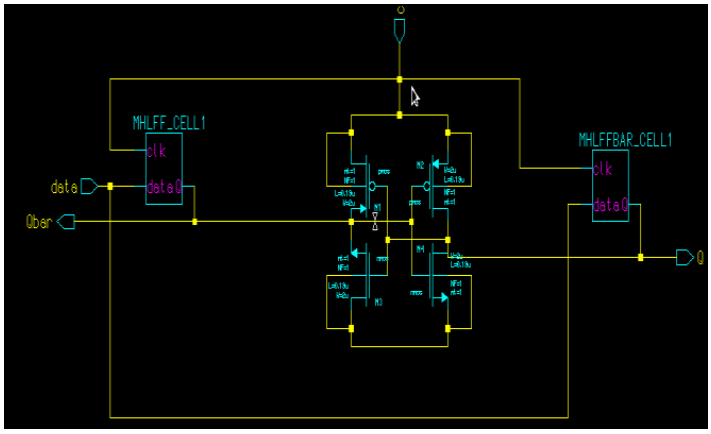

Fig5.5:MHLF Based on PFAL

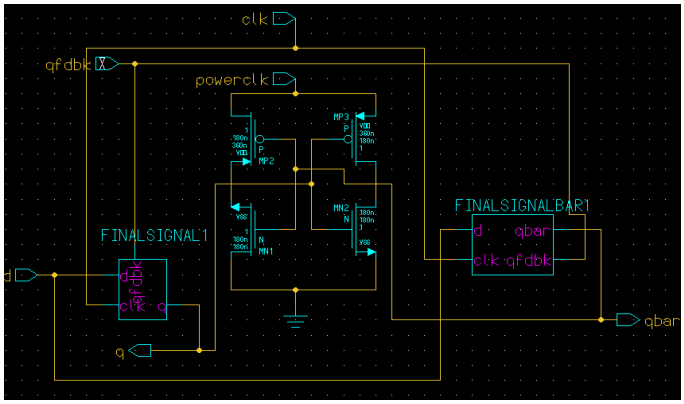

Fig5.6:P-FF design based on signal feed through scheme by using PFAL

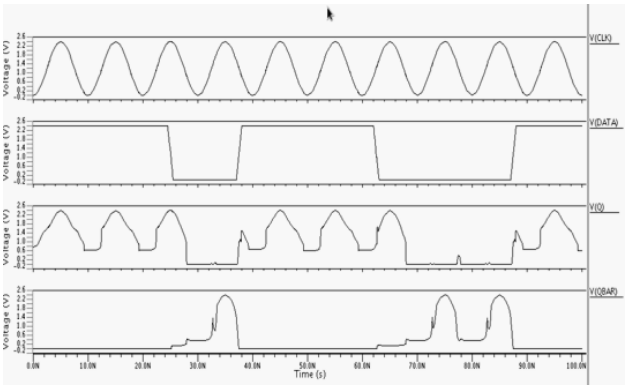

Fig5.7:Simulation Result Of Epdco

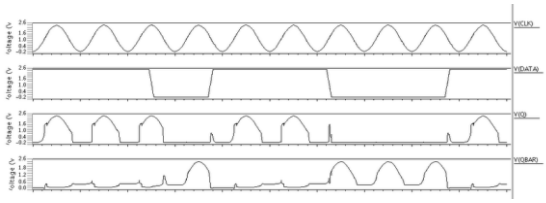

Fig5.8:Simulation Result Of CDFF

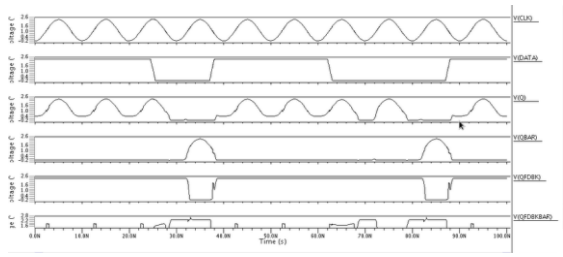

Fig5.9:Simulation Result Of SCDFF

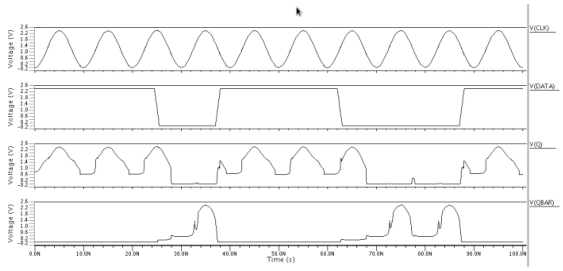

Fig5.9:Simulation Result Of MHLF

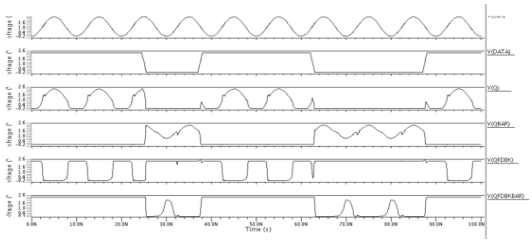

Fig5.10:Simulation Result Of Pff Based On Signal Feed Through By PFAL

Table: Comparision Of Conventional FF

Flip flop design	Total power dissipation (without adiabatic logic)	Total power dissipation (with adiabatic logic)
EPDCO	44.8099mw	3.7917mw
CDFF	10.2992mw	3.7341mw
SCDFF	10.074mw	3.7191mw
MHLF	10.062mw	3.89mw
SIGNALFEED THROUGH SCHEME	9.126mw	4.050mw

VI.CONCLUSION

In this paper, the comparison is made between the conventional P-FF designs with and without adiabatic logic in 180-nm technology. The power is considerably reduced which enhances power performance. The proposed P-FF designs are implemented by employing Positive Feedback Adiabatic Logic in which P-FF based on signal feed through scheme has considerable power reduction when compared to remaining P-FFs if the time charging constants are large.

VII.ACKNOWLODGEMENT

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