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Implementation and Performance analysis of Digital to Analog Convertor Using Custom Designer

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ABSTRACT: *Digital to Analog Converter (DAC), are the most complex structures and having digital input and analog output, it much more useful to found in almost all Analog and Mixed Signal Design today. There are different types of DACs currently on the market. The goal of this paper is to implement 4-bit Resistor String D/A converter using 4-bit AND gate and 4 to 16 Decoder with the help of 4 numbers Inverter. Binary (digital) coded 4-bit data was input to the converter. The data converter will convert all 4-bit binary coded data into correspondent different level of "staircase" voltage.*

KEY WORDS: *D/A Converter, AND gate, Inverter, NMOS, 4-to-16 Resistor String Decoder*

1. Introduction

In Analog and Mixed Signal circuit Design, there will always be more than one way to design the D/A converter. In the design of D/A converters mainly three types: Decoder Based DACs, Binary weighted DACs, Thermometer code DACs. It also provides several alternatives to the designer as to how to accomplish a same task.

So it is up to the designer to design Decoder based Resistor string digital to analog converter in an efficient way that result in optimal performance and minimum resource utilization.

In this paper, tool used for the design schematic of D/A converter is Galaxy Custom Designer schematic editor and Galaxy Custom Waveview for see the simulation results. It has own advantages and disadvantages so it is up to designer to choose appropriate design based on application. There is negligible effect on output waveform due to without use of the unity gain op-amp at output side and also use of the NMOS replace with transmission gate, increased the width of this NMOS and also increased the resistor string resistor value all this things are discussed in the paper.

2. Types of D/A Converter

There are mainly three types of D/A converter.

1. Decoder based
2. Binary weighted
3. Thermometer code

In this paper we are focus on the Decoder based D/A converter. Figure 1 shows the schematic of the high speed 4-bit Decoder based digital to analog data converter.

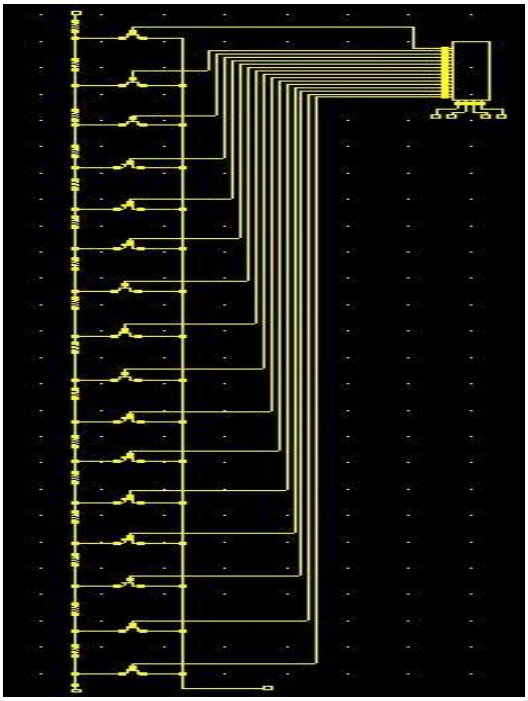

Figure 1 4-bit Decoder based DAC

As can be seen from Figure 1 in Decoder based DAC consists of an independent decoder that drives one of the 2^N transistors that are connected to the resistive string divider. A resistor string (acting as a voltage divider) that provides taps for the different voltage levels for digital to analog data conversion. One of these voltage taps is selected by a decoder network to connect appropriate voltage tap to the output node. The decoding network consists of a number of NMOSs that form a switching network. The switching network is connected in the form of a tree; only one low impedance path connecting one of the resistor string voltage tap point to the output node exists. The resistor string tap points ensure that monotonicity is maintained in the tapped voltage and therefore for the DAC. The accuracy of the DAC depends on the matching of these resistors.

3. Process Diagram of DAC

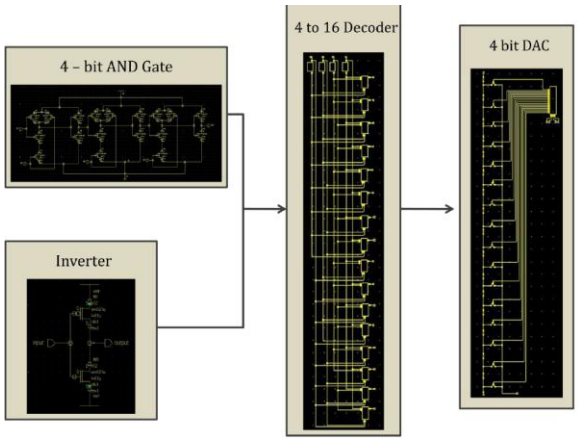

Figure 2 Process diagram of DAC

As can be seen from Figure 2 complete process diagram of Decoder based resistor string DAC with using of the Galaxy Custom Designer schematic editor tool. In this tool first we have to design schematic diagram at transistor level and design its test bench for the its simulation then finally shows the waveforms of the simulation of that schematic using of the Galaxy Custom Waveview.

4. Design of Inverter

Schematic

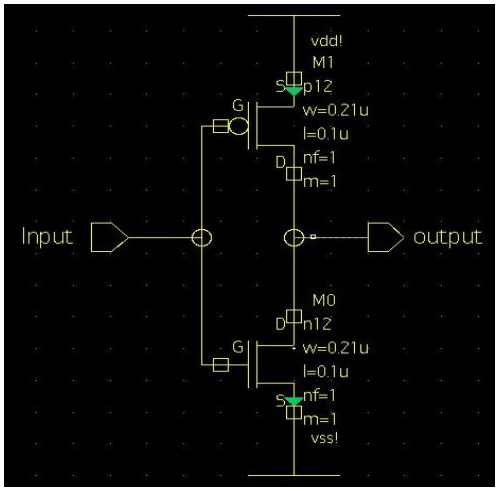

Figure 3 Schematic of Inverter

Figure 3 schematic diagram of inverter at the transistor level.

Test Bench

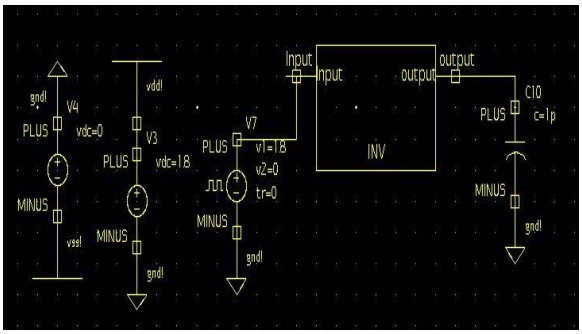

Figure 4 Test Bench of Inverter

Figure 4 give the details about the test bench of the Inverter. In that used Vdd=1.8V, Vss=0V and pulse given at the input of the inverter and also measure the output of the inverter by using the capacitor connected to the output side of the test bench of the inverter.

Waveform

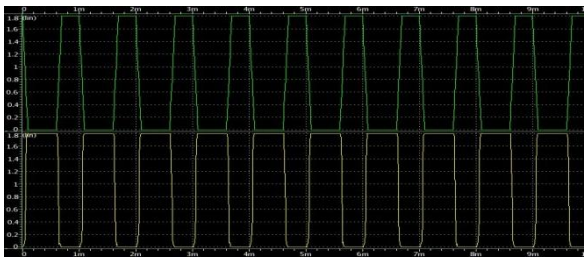

Figure 5 Waveform of Inverter

Figure 5 give the output waveform of the inverter with using pulse input to the test bench.

5. Design of 4-bit AND gate

Schematic

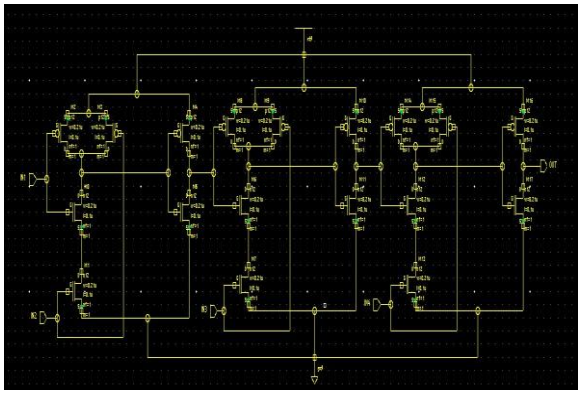

Figure 6 Schematic of 4-bit AND gate

Figure 6 schematic diagram of 4-bit AND gate at the transistor level.

Test Bench

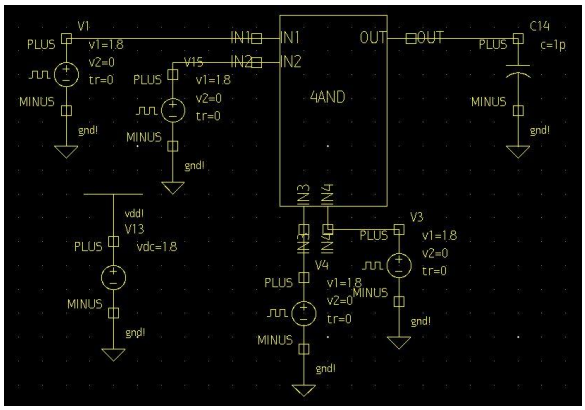

Figure 7 Test Bench of 4-bit AND gate

Figure 7 give the details about the test bench of the 4-bit AND gate. In that used Vdd=1.8V, Vss=0V and pulse given at the both input of the AND gate and also measure the output of the AND gate by using the capacitor connected to the output side of the test bench of the 4-bit AND gate.

Waveform

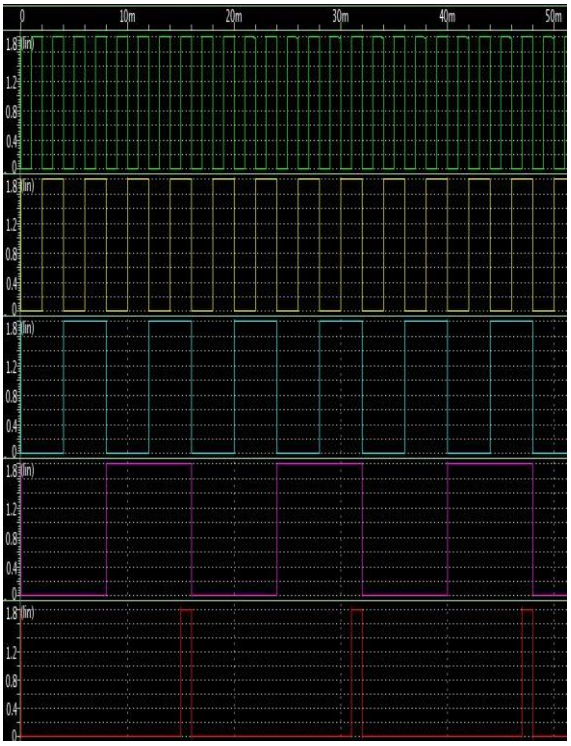

Figure 8 Waveform of 4-bit AND gate

Figure 8 give the output waveform of the 4-bit two input AND gate with using pulse input to the test bench.

6. Design of 4-to-16 Decoder

Schematic

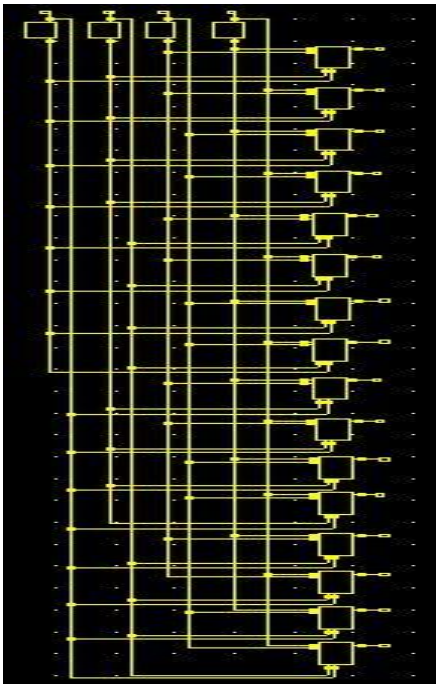

Figure 9 Schematic of 4-to-16 Decoder

Figure 9 schematic diagrams of 4-to-16 Decoder using inverter and 4-bit AND gate at the transistor level symbol.

Test Bench

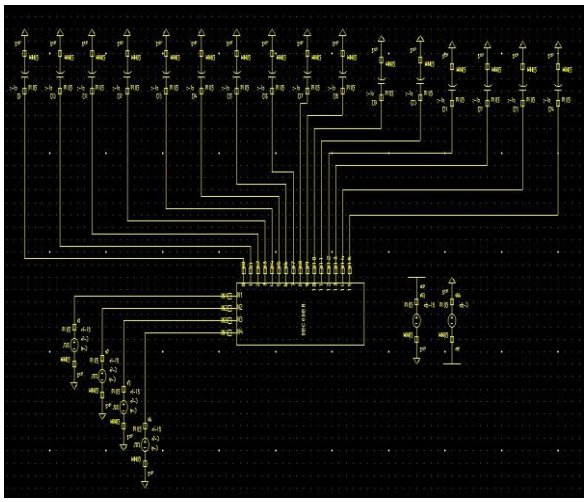

Figure 10 Test Bench of 4-to-16 Decoder

Figure 10 give the details about the test bench of the 4-to-16 Decoder. In that used Vdd=1.8V, Vss=0V and pulse given at the all four inputs of the Decoder and also measure at all the sixteen outputs of the Decoder by using the capacitor connected to the output side of the test bench of the 4-to-16 Decoder.

Waveform

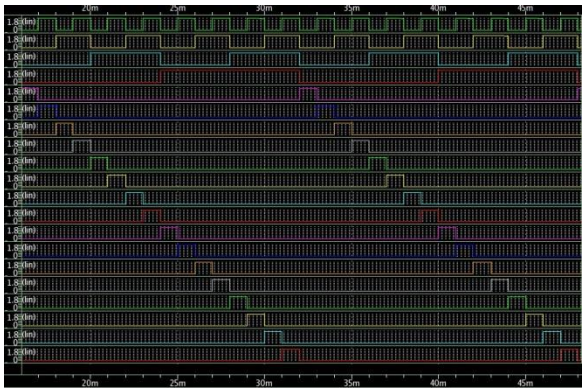

Figure 11 Waveform of 4-to-16 Decoder

Figure 11 give the output waveform of the 4-to-16 Decoder with using pulse input to the test bench.

7. Design of 4-bit Decoder based DAC

Schematic

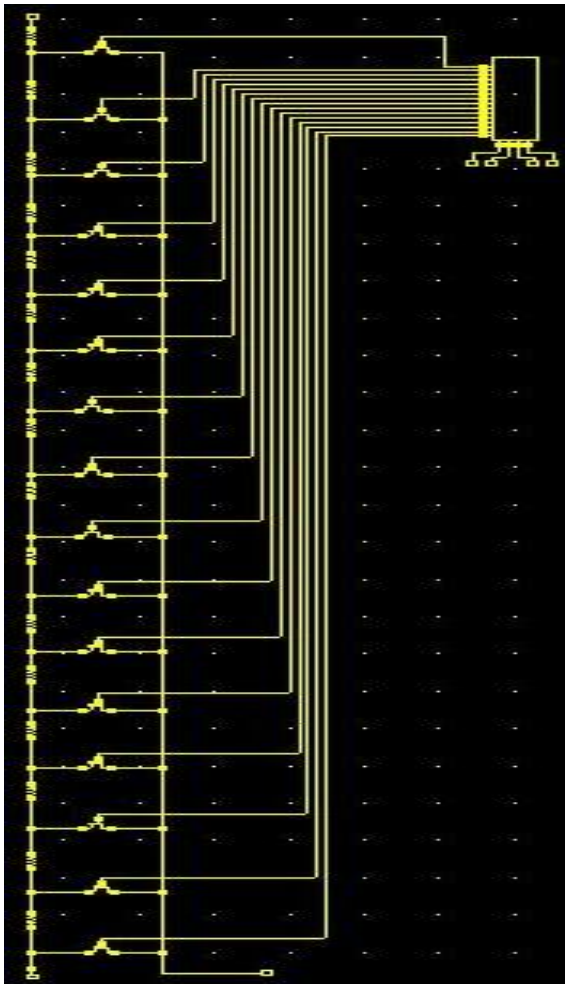

Figure 12 Schematic of 4-bit Decoder based DAC

Figure 12 schematic diagrams of 4-bit Decoder based DAC using 4-to-16 Decoder, Resistor string and NMOS transistor.

Test Bench

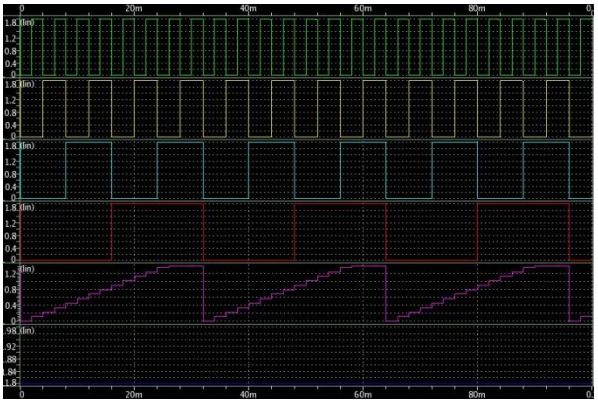

Figure 13 Waveform of 4-to-16 Decoder based DAC

Figure 13 give the output waveform of the 4-to-16 Decoder based DAC all inputs through resistor string using NMOS transistor pulse input to the test bench.

7. Conclusion

In this paper 4-bit resistor string decoder based digital to analog converter are design and simulate. In 4-bit resistor string type decoder based DAC, we had to use op-amp at the output of the DAC. However by using op-amp, the output observed lower than applied reference voltage. The expected output was achieved without any use of op-amp.
Instead of transmission gates, we can use a NMOS transistor based decoder; this results in reduced value of voltage swing at the output node.
We used 1MΩ resistance instead of 1KΩ but there was negligible difference in output waveform. We also increased width of NMOS by 5µm and 10µm but the output difference was very small.

8. Reference:

1. IEEE standard Verilog Reference Manual ,
   IEEE standard 2001
2. Verilog FAQ by Shivkumar Chanod , Needamangalam Balachandar
3. Galaxy Custom Designer User guide from Synopsys
4. Verilog HDL by Samir Palnitkar

