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Boostable Repeater Design with Dual Adaptive Supply Voltage for VLSI Interconnects

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Abstract — In general interconnects in vlsi circuit causes many variations and delay in the circuit. Process variations and circuit aging continue to be one of the main challenges to the power-efficiency of VLSI interconnect circuits. Not only Power efficiency, circuit delay and area also causes major effect in the vlsi interconnect circuits. To overcome these effects repeaters are used in the vlsi circuit to provide a better performance. Boostable Repeater design can transiently and autonomously raise its internal voltage rail with its boost switching speed. It achieves fine-grained voltage adaptation without stand-alone voltage regulators or an additional power grid and has plenty of chances to improve system robustness. The boosting can be turned on/off to compensate variations. There are mainly two approaches for variation compensation: Adaptive body bias(ABB) and supply voltage adaptation .An adaptive design provides a power-efficient approach to variation tolerance. The proposed technique is the Boostable Repeater design with Dual ASV(Adaptive supply voltage).The dual ASV can simultaneously provide adaptive supply voltage at both coarse-grained and fine-grained level, and has limited power routing overhead. The existing technique provides only fine-grained voltage adaptation where as the proposed technique provides both fine-grained and coarse-grained voltage adaptation

Keywords*-Dual Adaptive supply voltage,Fine-grained adaptation,Coarse-grained adaptation,Mini Programmmable Regulator,Boostable repeatercomponent;*

I. INTRODUCTION

As the VLSI technology scales to 45nm and beyond,manufacturing process variations and aging effects[1] cause remarkable uncertainty which must be considered in designs.A straightforward approach for variation tolerance is over-design. That is, the circuit is designed to meetperformance target with anticipation of the worst case variations. However, the worst case rarely occurs in reality andthe power increase resulted from the over-design is largely wasted. Statistical techniques merely reduce the pessimism inthe estimation of variations and do not solve the fundamental inefficiency of the over-design. A necessary condition for power-efficiency is to spend power only when it is needed.Since the need for variation compensation is clear only after chip fabrication, adaptive circuit (or post-silicon tuning) is an arguably efficient approach.

In this work, we propose a new Adaptive Supply Voltage (ASV) system for circuits with many timing critical paths. In typical design flows, circuits are optimized to suppress the delay of timing critical paths and reduce the power on non-critical paths. Consequently, path delays tend to be equalized and there are many paths with similar timing criticality. This phenomenon implies a wide range of possibilities for variation-induced timing degradation:from a few paths to many paths. This wide range makes ASV very difficult to implement. If one adopts coarse-grained ASV, there could be considerable power waste when the degradation actually occurs only on a few paths. If one chooses fine-grained ASV and prepares for degradations on many paths, a large overhead on power routing or voltage regulators is usually incurred.

Our system solves the aforementioned difficulty by simultaneously providing coarse-grained and fine-grained ASV. In this dual-level ASV system, power routing overhead is largely avoided by a new technique of voltage tapping in the context of voltage island based designs[2,3]. We also considered the impact of the variation on the dual-ASV system itself embedded in the circuits. A weakness of our approach is that it is limited to voltage island based designs. However, multi-supply-voltage designs become increasingly popular for the sake of power management.Therefore, the limitation of our approach will become less severe.

The boostable repeater design enables fine-grained circuit adaptation, and therefore, power-efficient resilience to variations.. When the variations on a fabricated circuit are widespread, a global supply voltage tuning will be more effective. Hence, the boostable repeater design is a complement rather than a replacement to coarse-grained adaptation. Since interconnect is a well-known bottleneck for chip performance and a modern chip design may contain hundreds of thousands of repeaters [17], there are plenty of opportunities for boostable repeaters to find critical places and exert significant impact.

We composed an adaptive system, which combines the proposed boostable repeaters with Dual ASV system. This is because we propose boostable repeater to compensate finegrained and coarsegrained variations, in other words, severe degradations on a limited number of critical paths. The proposed adaptive system with boostable repeaters integrated with Dual ASV system is simulated in Mentor Graphics and the power and delay calculations are calculated.

II. PROPOSED DESIGN

The proposed design is the boostable repeater design with dual adaptive supply voltage(which is going to produce both fine-grained and the coarse-grained voltage adaptation).The proposed design is shown below in the following figure.1 which is boostable repeaters and Dual ASV are explained in detail in section 2 & 3.

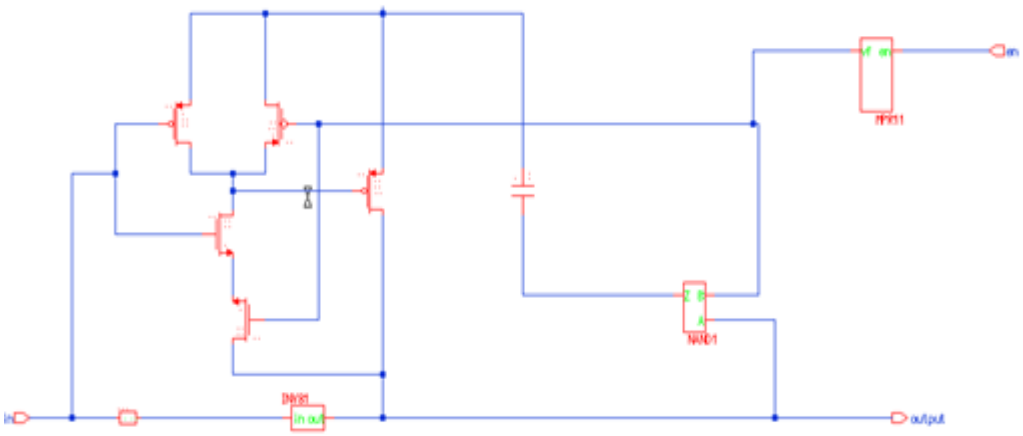

Figure.1. Boostable Repeater Design with Dual adaptive supply voltage

III. BOOSTABLE REPEATER DESIGN

3.1. Main Idea and Overview

An overview of our boostable repeater design is depicted in Fig. 2. It is composed of three parts: a conventional repeater, booster, and control circuit. The core part is the booster, which is a capacitive charge pump. When the repeater is in steady state, the pump is charged. When the repeater has a rising switching, the pump discharges and provides a transient voltage that is higher than *V*DD. This high voltage is applied together with the *V*DD to the repeater, and therefore, boosts the switching speed.The control circuit activates or disables this boosting function according to an enable signal, which is usually obtained from variation detection circuit.The booster adds extra load capacitance to the input and output node

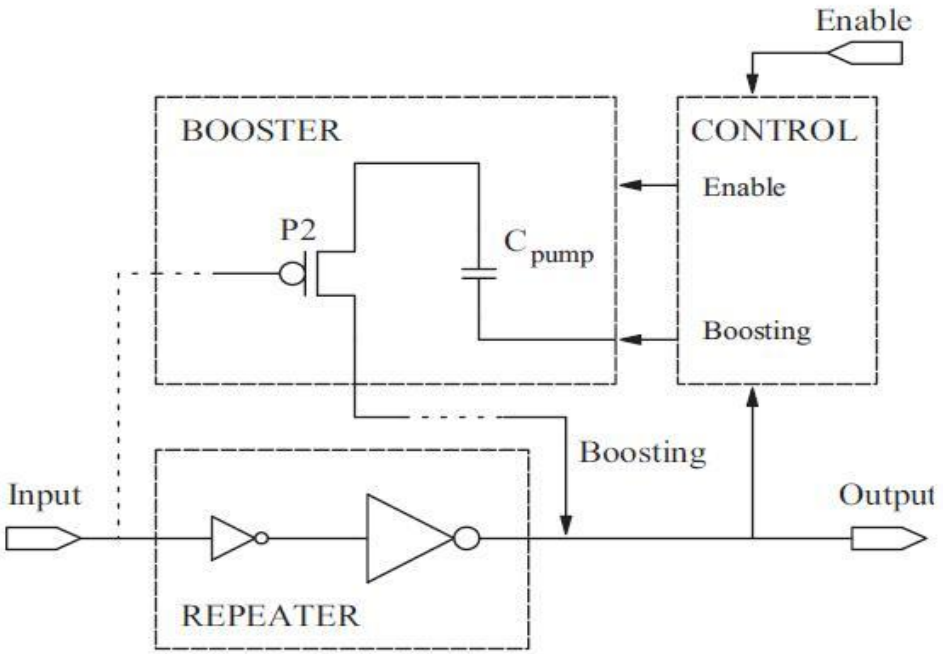

Fig. 2. Overview of boostable repeater

3.2. Design and Operations

3.2.1.Boosting On:

If the boosting feature is always on and cannot be turned off, i.e., it is not programmable, the design is a simplified version shown in Fig. 3(a). Transistor P2 is the pass transistor that delivers current from *C*pump to the output node. Transistor P1, N1, and the inverter between the output and node 3 coordinate the operations. The operations mainly include two phases: charging and boosting.

3.2.2. Charging Phase:

Charging to the capacitor *C*pump takes place when both the input and the output are stabilized to high, or *V*DD. When the input and the output are high, P1 is off, N1 is on, and V3 (voltage at node 3) is low.

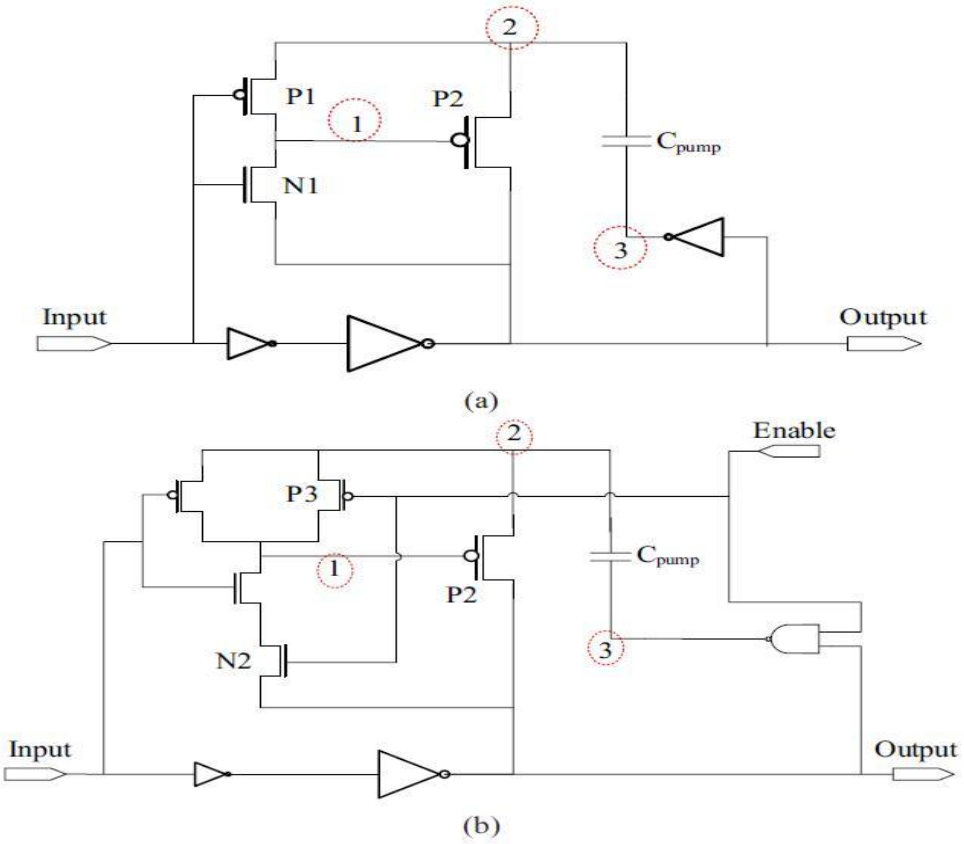

Fig. 3. Schematics of boostable repeater.(a) Simplified schematic.(b) Complete schematic

3.2.3. Boosting Phase:

The boosting occurs when there is a rising switching at the input.Due to the gate delays between the input and the output, there is a short time period when the output is still low even the input goes high. During this period, N1 is turned on and pulls V1 toward low. The low voltage at node 1 turns on pass transistor P2 and *C*pump starts to discharge and pull up the output voltage, i.e., the boosting starts. At the same time, the input rising is propagated to the output and the output is pulled up by *V*DD as well.

3.2.4. Boosting Off:

In Fig. 3(a), the boosting function cannot be turned off, i.e., not programmable. In order to allow it to be turned off, additional transistors must be added. The complete design with programmability is shown in Fig. 3(b). When the Enable signal is high, the circuit operates in the same way as that in Fig. 3(a). When Enable is low, the NAND2 gate outputs

constant high. At the same time, transistor N2 is off and P3 is on. Therefore, pass transistor P2 is turned off. The booster part is disconnected from the output node.

IV. DUAL LEVEL ADAPTIVE SUPPLY VOLTAGE (ASV) SYSTEM

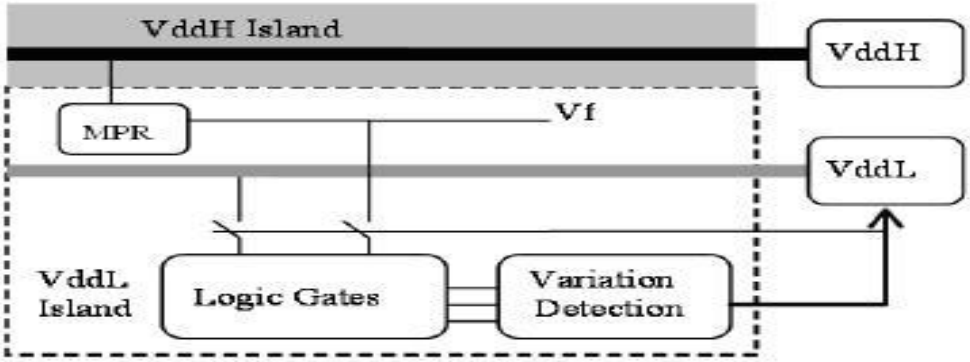

Figure 4: Overview of dual-ASV system. MPR is the proposed Mini Programmable linear voltage Regulator

Overview of dual-ASV is illustrated in Figure 4. It is in the context of voltage island based designs.In the low VDD island, an additional power supply is obtained by tapping off an intermediate voltage level Vf from VDD,H of its neighboring high VDD island. The level of Vf is somewhere between VDD,H and VDD,L. Vf is supplied only to the critical paths in the low VDD island. The difference of Vf – VDD,L is small so that Vf and VDD,L can be applied to the same circuit block without using level shifters.A delay variation prediction circuit[12] is employed. It can generate a warning signal if a delay variation is large and close to timing error. When only a few paths receive variation warnings, these paths are switched from VDD,L to Vf. If the majority of critical paths have warnings, VDD,L is raised like in conventional ASV.

Therefore, we can achieve ASV at two levels: VDD,L at coarse-grained level and Vf at fine-grained level. When tapping Vf from VDD,H, we use linear regulators .

We choosed a Mini Programmable linear voltage Regulator (MPR) for a relatively small load current. The transistor level schematic of MPR is depicted in Figure 5. This circuit consists of 3 stages. The first stage is a voltage divider which generates the reference voltage, the reference voltage generator is greatly simplified. The middle stage of MPR is an opamp-based voltage follower. The last stage includes an output driver Mdr and a decap. The driver provides current to load and the decap is to reduce supply voltage noise.

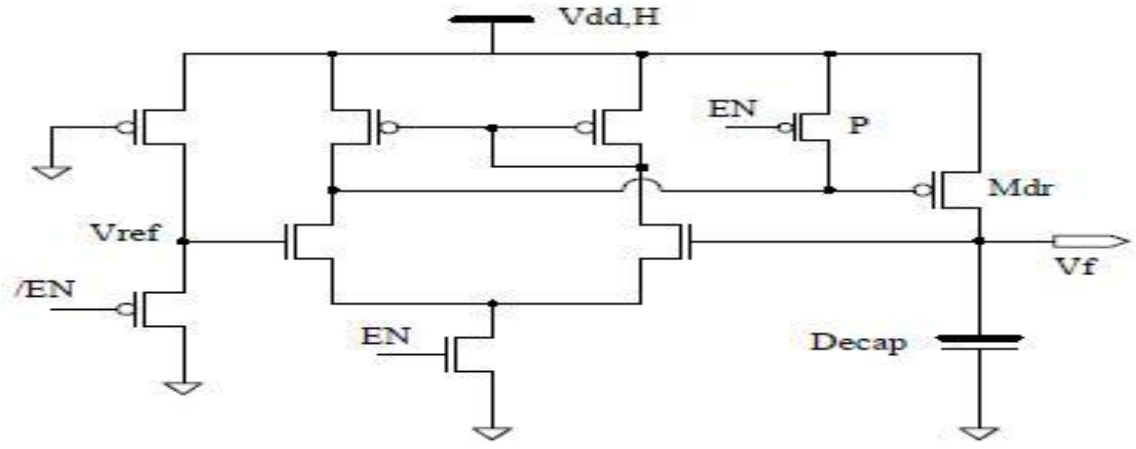

Figure 5: Circuit of Mini Programmable linear voltage Regulator (MPR)

The EN signal and a control transistor P in Figure 5. MPR is turned off when EN is low. By applying the EN signal, one does not need to worry about the standby current like in the conventional regulator designs . This is one reason that we use such simple design. In the dual-ASV system, the EN signal is not an overhead since we need to have it to control the power supply switching between Vf and VDD,L anyway, i.e., the EN signal is already in our system regardless of the design of the regulator. Additional benefit of the EN signal is that the switch between Vf and the logic circuit in Figure 4 can be skipped. Usually such switch is implemented by pMOS sleep transistors. Removing the sleep transistors not only reduces area/power overhead but also allows performance improvement. This is because the voltage drop across the sleep

transistor is avoided and the logic circuit can be powered by Vf directly instead of degraded Vf. Although the design of the regulator MPR here is simple, it works very well for the voltage tapping where the typical current is around 1mA.

V. **EXPERIMENTAL RESULTS**

The proposed design circuit is simulated by using mentor graphics and the results of the proposed design is given in the below tabular form .

Table 1. Comparison of Testing circuits with and without boostable repeater design with Dual ASV System

NAME OF THE CIRCUIT	TOTAL POWER DISSIPATION	DELAY
BOOSTABLE REPEATERS	112.21pW	482.12pS
D-ASV+BOOSTABLE REPEATERS	94.56pW	232.73pS
SCAN CELL	383.25nW	100.87nS
D-ASV+BOOSTABLE+SCAN	8.34nW	100.46nS
GATING SCAN CELL	30.873uW	2.033nS
D-ASV+BOOSTABLE+ GATING SCAN CELL	23.819uW	1.648nS
SRAM	1.508nW	3.097nS
D-ASV+BOOSTABLE+ SRAM	1.603nW	893.45pS
DRAM	10.2pW	911.98pS
D-ASV+BOOSTABLE+DRAM	98.0pW	866.01pS
BIST SCAN	169.23uW	14.577nS
D-ASV+BOOSTABLE+BIST SCAN	65.144uW	14.344nS
BILBO		
00	480.31pW	643.72pS
01	420.14pW	1.84nS
10	586.52pW	2.9nS
11	498.00pW	736.51pS
DASV+BOOSTABLE+BILBO		
00	434.45pW	807.67pS
01	348.84pW	1.28nS
10	491.61pW	1.4nS
11	391.89pW	778.43pS

VI. CONCLUSION

The technique of boostable repeater design, can transiently boost its switching speed. This technique can be applied to achieve variation tolerance and aging resilience in a power efficient manner. The dual-level adaptive supply voltage system allows fine-grained and coarse-grained adaptive supply voltage with simple regulator designs and low power routing overhead. The Proposed design is the boostable repeaters is combined with the Dual ASV for getting better performance in terms of the power and delay calculations. The proposed design is verified with different testing circuits like Sequential circuits, Combinational circuits, Memory circuits and BIST Scan circuits.The performance of the testing circuits with and without the proposed design is observed .By comparing the results between the testing circuits with and without the proposed design, the testing circuits which are applied to the proposed design provides the better performance than the performance of the normal testing circuits.

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