Scientific Journal of Impact Factor (SJIF): 4.72

e-ISSN (O): 2348-4470
p-ISSN (P): 2348-6406

International Journal of Advance Engineering and Research Development

Volume 4, Issue 10, October -2017

Two level Half bridge dc-dc converter with Reducing circulating losses

[1]P. PragnaSree, [2]J.Siva Vara Prasad

[1]M.tech student, EEE, LBRCE, LBRCE, Mylavaram, India.
[2]Associate professor, EEE, LBRCE, LBRCE, Mylavaram, India.

Abstract— *The paper presents a Two level half bridge dc- dc converter with reducing circulating losses. The proposed converter can have the rectifier stage which is composed of four diodes in the center-tapped rectification. On the primary side of the transformer, the two transformers are connected in series and the middle node of the two transformers is connected to the neutral point of the split flying capacitors. Because it cooperates with the four-diode rectifier stage, the circulating current on the primary side of the transformer decays to zero during the freewheeling period. The zero-voltage switching (ZVS) of the leading switches is it stores energy in the output filter inductor and the lagging switches is it stores energy in the magnetizing inductor of a transformer, rather than the energy stored in the leakage inductor. This proposed technique is ideal for an application which requires good performance and improves the efficiency. This paper discusses the brief analysis along with simulation results.*

Keywords—*Reduced circulating current, two-level (TL), zero voltage switching (ZVS).*

I. INTRODUCTION.

High input voltage dc–dc converters are required for many specific uses, such as battery chargers, industrial power supplies, and solid-state transformers. For three-phase diode rectifiers, the output dc voltage reaches above 500 V. Because the voltage stress is decreased to half of the input voltage and the switches can work in zero-voltage switching (ZVS), the three-level (TL) dc–dc converter can be used in high-input voltage applications.[1].

The essential relationships among the family of the TL dc–dc converter have been revealed in [2], and the phase-shift controlled manner is employed in TL dc–dc converters. However, it is difficult to achieve ZVS for lagging switches especially at light loads. The switching noise and electromagnetic interference caused by hard switching degrades the performance of the converter. Moreover, the circulating current reduces the efficiency as the input voltage increases.

In order to reduce the circulating current and conduction loss, a blocking capacitor is used to reset the primary winding current. In order to avoid the current flowing to the reverse direction during the freewheeling period, two diodes are series connected with the lagging switches [3].

In order to reduce the output filter inductance, hybrid TL dc–dc converters with more than one transformer have been proposed [4].

The design guidelines of the converter are presented. The experimental prototype with 550 ~600 V input voltage and 50V output is built to verify the performance of the proposed converter.

II. PROPOSED HYBRID TL PLUS HALF BRIDGE DC–DC CONVERTER.

Fig. 1 shows the circuit for the proposed converter, which is composed of a TL dc–dc converter and HB dc–dc converter. The split capacitors of C_{m1}, Cm_2, and the flying capacitor C_{rr1} and C_{rr2} are large enough to be treated as voltage sources, i.e.,$V_{Cm1} = V_{Cm\ 2} = V_{in}/2$, $V_{C\ rr1} = V_{C\ rr2} = V_{in}/4$. Q_1 and Q_4 are leading switches; Q_2 and Q_3 are lagging switches. The TL converter shares the lagging switches Q_2 and Q_3 with the HB dc–dc converter. $C_1 - C_4$ are junction capacitors of the switches, and $C_1 = C_2 = C_3 = C_4 = C$. $T_{r\ 1}$ is the transformer of the TL converter and $T_{r\ 2}$ is the transformer of the HB converter. The turns ratio of the two transformers T_{r1} and $T_{r\ 2}$ are n_1: 1: 1 and n_2: 1: 1, respectively. $L_{f\ 1}$ and $L_{f\ 2}$ are the leakage inductors of T_{r1} and T_{r2}. The magnetizing inductor of T_{r1} is designed large enough, thus the magnetizing current during the switching period can be ignored. $L_{m\ 2}$ is the magnetizing inductor of T_{r2}. Fig. 2 shows the key waveforms of the proposed converter. There are eight working modes of operation each having half-switching period.

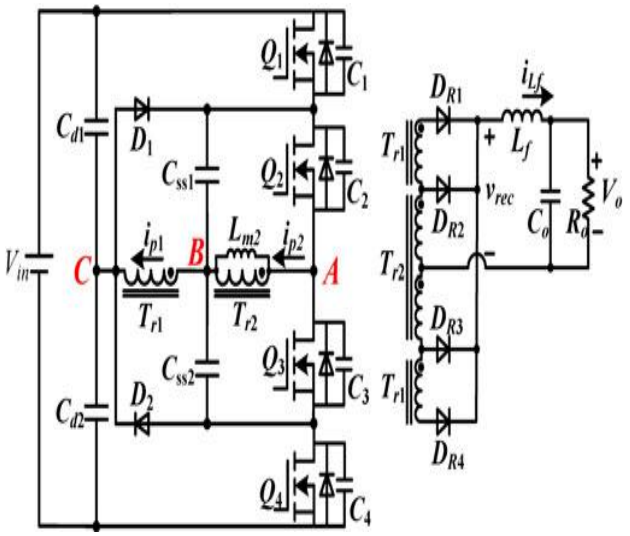

Fig. 1. Proposed Two Level HB converter

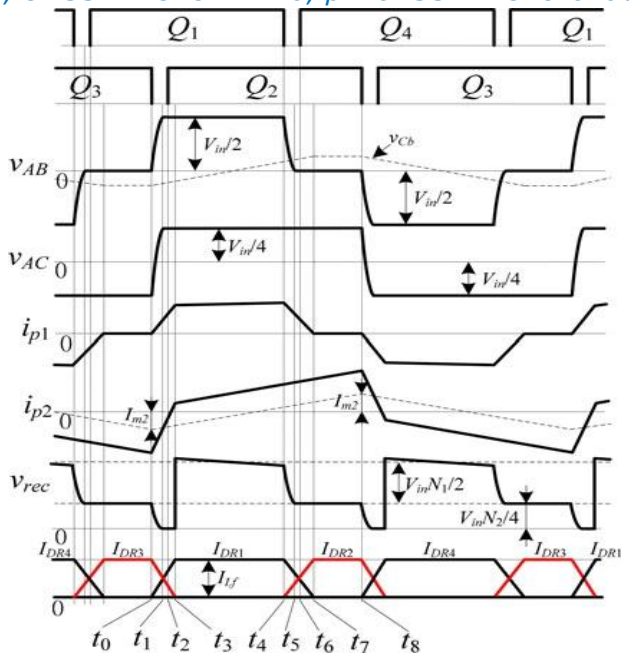

Fig. 2. Wave forms of the proposed converter

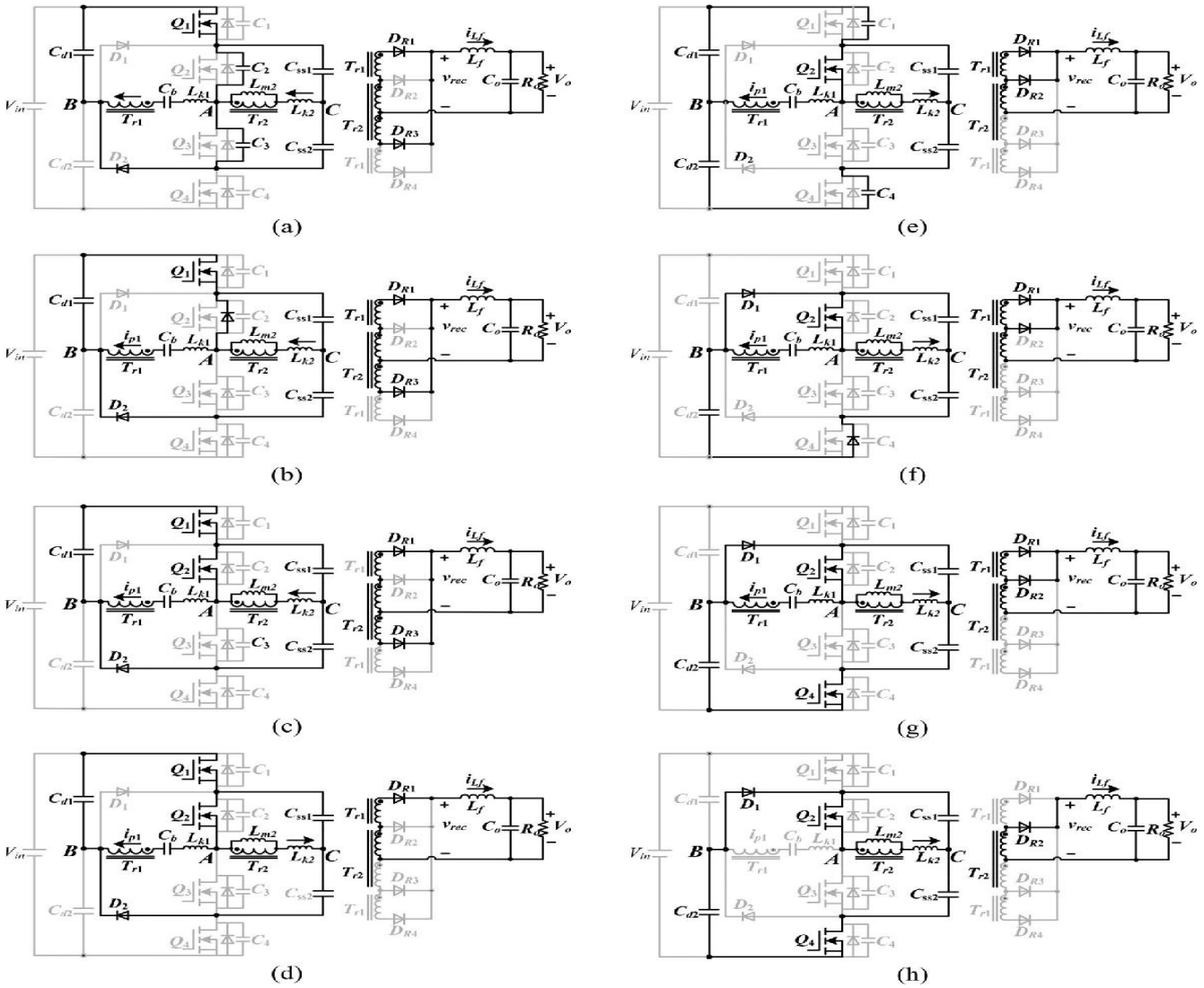

Fig. 3. Half-switching cycle: (a) [t_0 , t_1], (b) [t_1 , t_2], (c) [t_2 , t_3], (d) [t_3 , t_4], (e) [t_4 , t_5],(f) [t_5 , t_6], (g) [t_6 , t_7],(h) [t_7, t_8]

Stage 1([t_0, t_1]) [see Fig. 3(a)]

Prior to t0, Q1 and Q3 are ON, and Q2 and Q4 are OFF. The primary winding current in Tr1 stays at zero, and the primary winding current in Tr2 is negative. The output filter inductor current flows through DR3. At time t0, Q3 is turned OFF. The junction capacitors of Q3 and Q2 are charged and discharged by the primary winding current in transformer Tr2, which includes the leakage inductor current and magnetizing current of Tr2. At t0, the primary winding current in Tr1 starts to increase. The current for charging flying capacitors Crr1 and Crr2 flows through Q1 and D2. Since DR1 and DR3 are forward biased and DR2 and DR4 are reverse biased, the current in DR1 starts to increase and the current in DR3 starts to decrease. The amplitude of the magnetizing current of Im2 is expressed as

$$\mathrm{Im}2 = \frac{VinTs}{16\mathrm{Im}2} \tag{1}$$

Where Ts is the switching period.

Stage 2 ([t_1, t_2]) [see Fig. 3(b)]

At time t1, the drain-source voltage of Q2 reaches zero, and ip2 flows through the body diode of Q2. The voltage across the primary winding of Tr2 is Vin/4. ip1 and ip2 increase linearly. Q1 and D2 still conduct to charge the flying capacitors Crr1 and Crr2.The filter inductor current iLf flows through DR1 and DR3.The current in DR1 continues to increase, and the current in DR3 continues to decrease. ip1 and ip2 in this stage are expressed as

$$ip1(t) = ip1(t1) + \frac{Vin - 2Vcb(t)}{2Lk1}(t - t1)$$
$$ip2(t) = ip2(t1) + \frac{Vin}{4Lk2}(t - t1) \tag{2}$$

Stage 3 ([t_2 , t_3]) [see Fig. 3(c)]

At time t2, Q2 is switched ON with ZVS. iLf keeps on freewheeling through DR1 and DR3. The current in DR1 continues to increase, and the current in DR3 continues to decrease. Ip1 and Ip2 still increase linearly as expressed in (2).

Stage 4 ([t_3, t_4]) [see Fig. 3(d)]

At time t3, the current in DR3 decays to zero, and DR3 is reverse biased. The filter inductor current flows through DR1. The two transformers start to transfer energy to the output. The secondary winding current in Tr2 is equal to that in Tr1. Ignoring the ringing of the rectifier diodes, the average voltage of Vrec in this stage is Vin/2n. Neglecting the output current ripple, ip1 and ip2 in this stage is expressed as

$$vrec(t) = \frac{Vin/2 - vcb(t - t3)}{n1} + \frac{Vin}{4n2}$$
$$ip1(t) = \frac{I_{Lf}}{n1} \tag{3}$$
$$ip2(t) = \frac{I_{Lf}}{n2} - \mathrm{Im}2 + \frac{Vin}{4Lm2}(t - t_0)$$

Stage 5([t4, t5]) [see Fig. 3(e)]

When Q1 is turned OFF at t4, the voltages across the junction capacitors C1 and C4 are charged and discharged linearly by the energy stored in the output filter inductor Lf. The voltage across the primary winding of Tr1 starts to decrease. Ip1 starts to decrease. At the same time, the current in DR1 decreases, and the current in DR2 increases. The magnetizing inductor current in Tr2 is still linearly increasing.

Stage 6 ([t5, t6]) [see Fig. 3(f)]

When the voltage across C1 reaches Vin/2 and the voltage across C4 reaches zero, the body diode of Q4 is forward biased. At this time, the voltage across the primary winding of Tr1 is −Vin/4. Due to the negative voltage, the primary winding current in Tr1 decreases linearly. Simultaneously, the current in DR1 continues decreasing and the current in DR2 continues increasing.

Stage 7 ([t6, t7]) [see Fig. 3(g)]

At time t6, Q4 is turned ON With ZVS. The primary winding current in Tr1 continues decreasing. D1 and Q4 start to charge the flying capacitors Css1 and Css2. The current in DR1 continues decreasing, and the current in DR2 continues increasing.

Stage 8 ([t7, t8]) [see Fig. 3(h)]

Stage 8 starts when ip1 is reset to zero. The voltage across the primary winding of Tr1 is negative, so DR1 is reverse biased. Therefore, the flowing path of the secondary current in Tr1 is blocked. DR2 carries all the filter inductor current. D1 and Q4 still conduct to charge flying capacitors Crr1 and Crr2. The circulating current in Tr1 is reduced. Ignoring the ringing of the rectifier diodes, the average voltage of vrec in this stage is Vin/4n. ip2 in this stage is expressed as

$$vrec(t) = \frac{Vin}{4n_2}$$
$$ip_2(t) = \frac{ILf}{n_2} - \mathrm{Im}2 + \frac{Vin}{4Lm_2}(t - t_0) \qquad (4)$$

Table 1. values of Proposed Converter

Components	Volume
Input voltage Vin	550v
Output voltage Vout	50v
n1	5.5
n2	9
Cm1=Cm2	20µF
Crr1=Crr2	4.7µF
Magnetizing inductance Lm2	170µH
Lf	130µH
C o	200µF
Switching frequency	100KHz

III. ZVS Condition of Switches.

During the commutations, the leading switches are charged and discharged by the primary currents in Tr1, which are all reflected from the energy stored in the output filter inductor. It is similar to conventional TL dc–dc converters. Therefore, the leading switches are easy to achieve ZVS at both the heavy load and light load..

For the conventional TL dc–dc converter, the ZVS of lagging switches is determined by the energy stored in the leakage inductor. In the proposed converter, the ZVS for lagging switches is determined by the energy stored in magnetizing inductor of Tr2, independent of the load power. The magnetizing inductor current should be large enough to charge and discharge the junction capacitors of the lagging switches. In order to guarantee soft switching at light loads, the converter should meet the following condition:

$$i_{p1} = I_{m2} - I_{m2}\cos[\omega_m(t - t_0)]$$
$$v_{c2}(t) = \frac{V_{in}}{2} - \frac{I_{m2}}{2C\omega_m}\sin[\omega_m(t - t_0)]$$
$$v_{c3}(t) = \frac{I_{m2}}{2C\omega_m}\sin[\omega_m(t - t_0)]$$

I. Simulation Results.

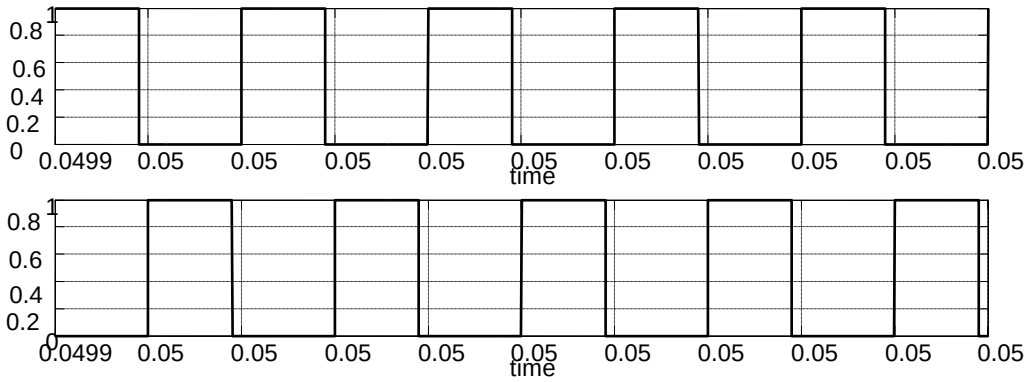

Fig.4. Gate Switching pulses of Q1,Q4

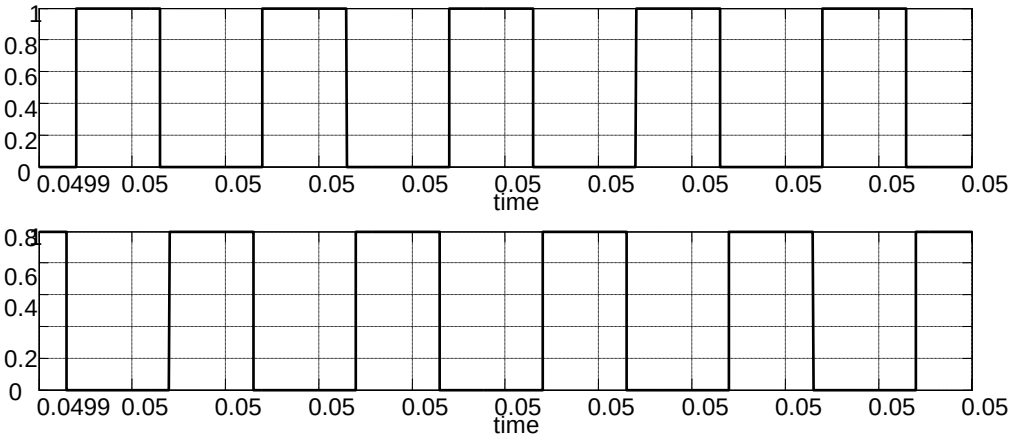

Fig.5. Gate Switching pulses of Q2,Q3

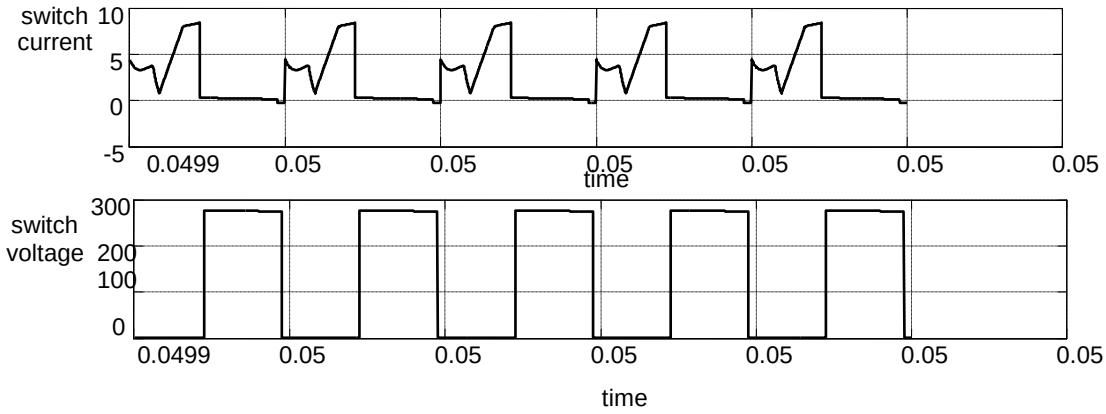

Fig.6.ZVS Of Q1 switching current and voltage

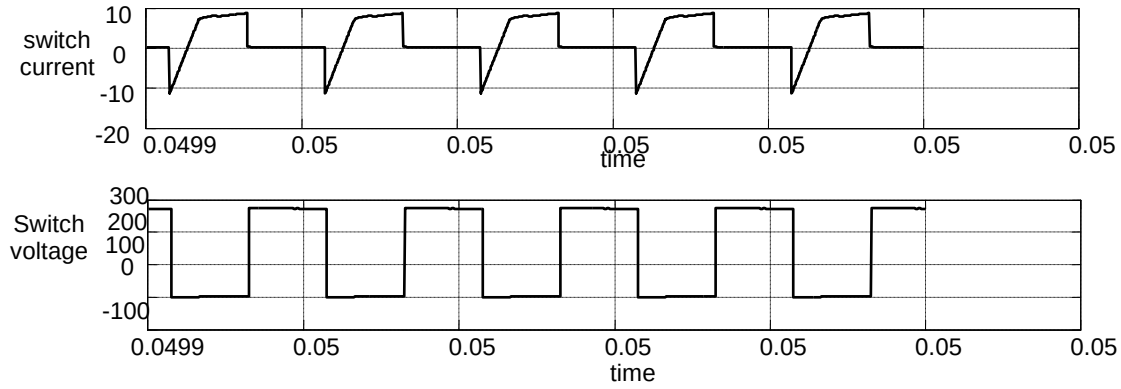

Fig.7. ZVS Of Q2 switching current and voltage

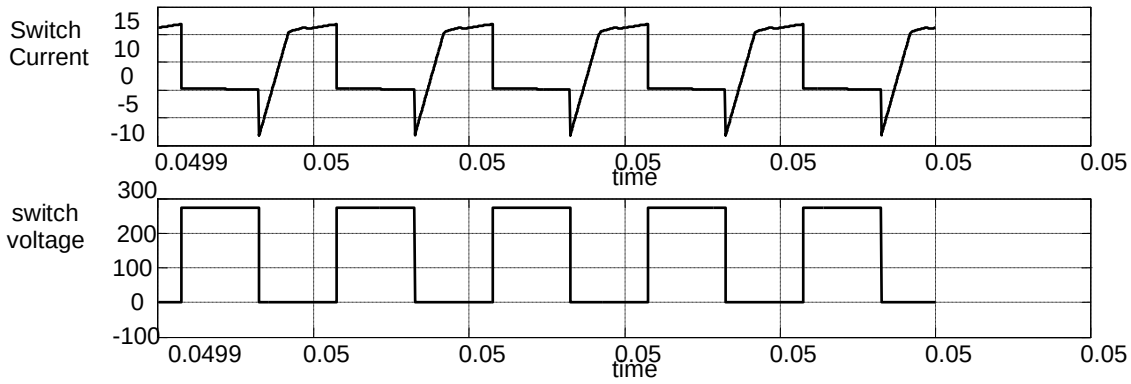

Fig.8.ZVS Of Q3 switching current and voltage

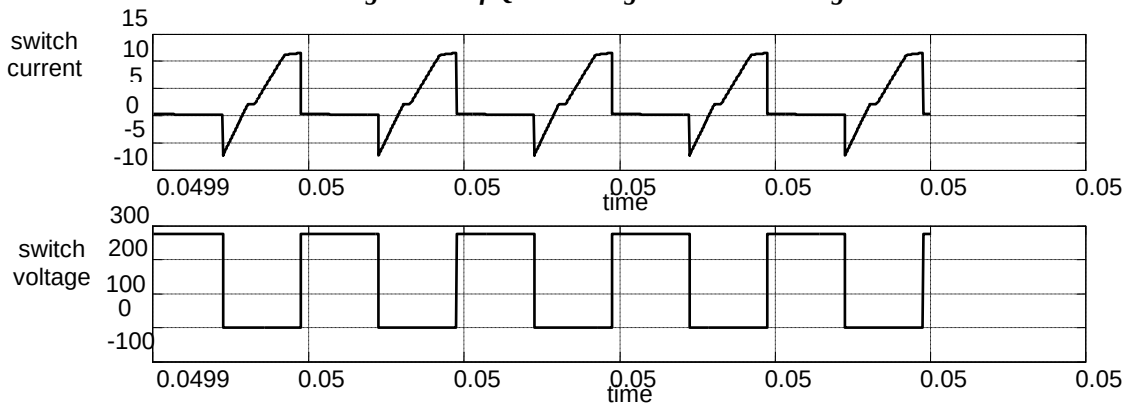

Fig.9.ZVS Of Q4 switching current and voltage

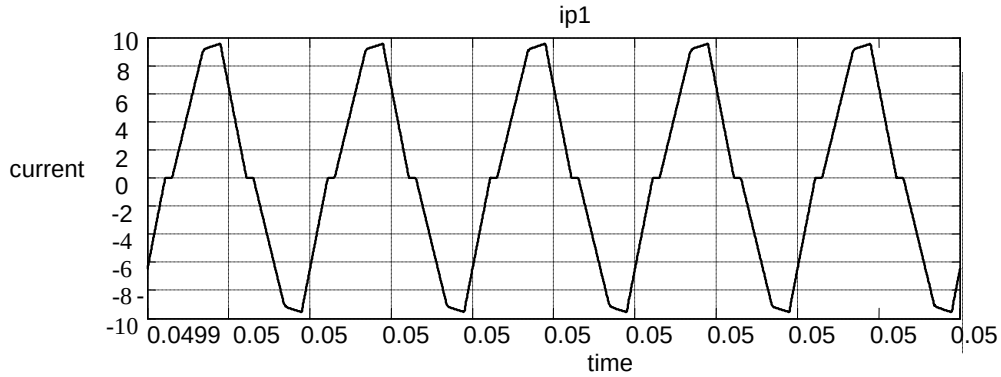

Fig.10. Primary transformer of Tr1 current at Ip1

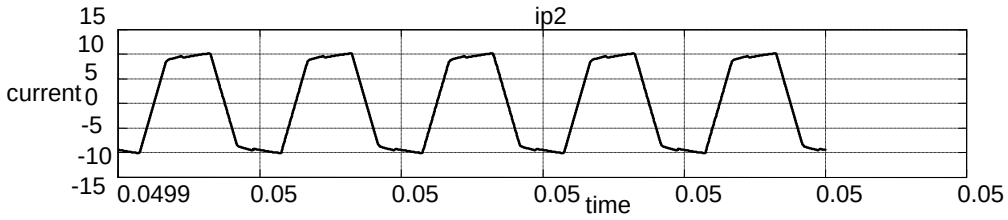

Fig.11. Primary transformer of Tr2 current at Ip2

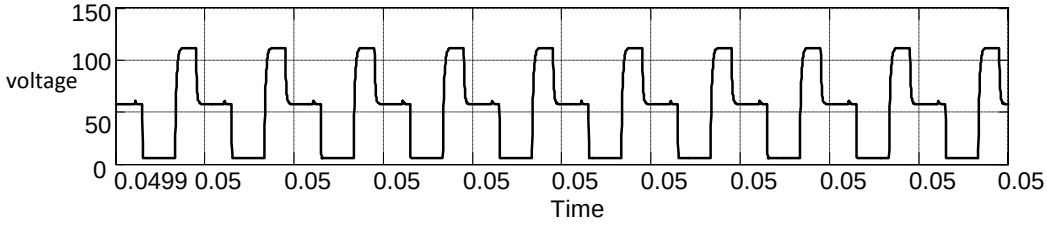

Fig.12. Secondary Transformer voltage of Tr2 at voltage Vrec

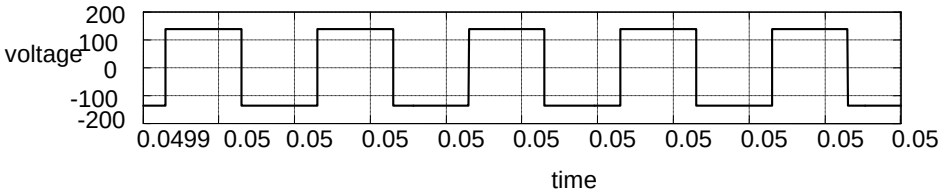

Fig.13. Primary Transformer voltage of Tr1 at voltage Vab

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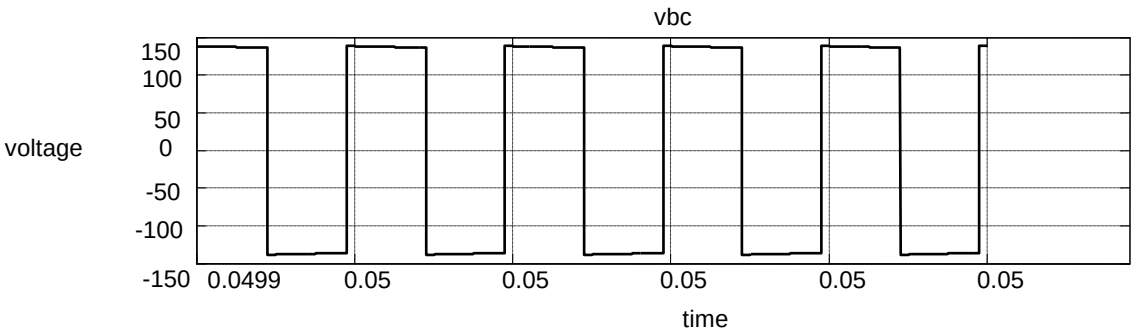

Fig.14. Primary Transformer voltage of Tr1 at voltage Vbc

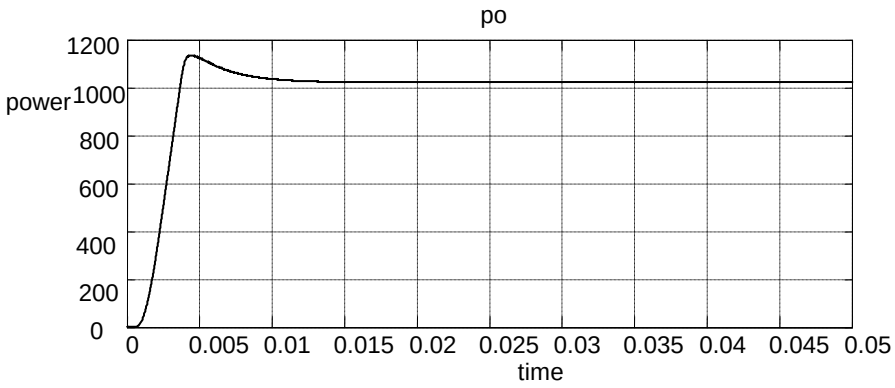

Fig.15. Proposed Converter Output Power Vs Time

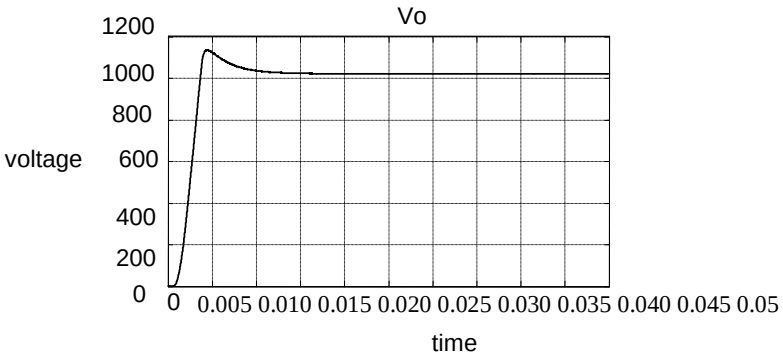

Fig.15. Proposed Converter Output Voltage Vs Time

II. CONCLUSION.

In this paper, Two Level HB dc–dc converter by sharing the lagging switches to reduce the circulating current and improves higher efficiency. Since the switches only undergo half of the input voltage, the proposed converter is suitable for high input voltage applications. The magnetizing inductor of the HB transformer can extend the ZVS of the lagging switches. Compared with the conventional T L dc–dc converter, the current stress of the switches and clamping diodes are all reduced, resulting in lower conduction loss.

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AUTHOR PROFILES

P.PragnaSree, M.Tech. student, lakireddyBali reddy College of engineering, Mylavaram, Krishna dist. Andhra Pradesh, India. Interesting area in Power Electronics and Drives.

J.Sivavaraprasad obtained EEE from AITS, Rajampet(2001-05), M.tech. JNTU College of Engineering,

Anantapur (2006-08),PhD(2010) ,working as Associate Professor in lakireddyBali reddy College of engineering,

Mylavaram Krishna dist,Andhra Pradesh, India. Interesting area IN Industrial and Drives.

