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Survey: Design Procedure of VLSI, FPGA & ASIC Life Cycle's

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Abstract — *In real time world VLSI plays a prominent role. The paper presents a survey of VLSI, FPGA & ASIC life cycles and its design procedure. The present portable electronic devices like smart phones, Laptops etc., are capable of multi-functional and multi domain application areas. These types of applications are possible due to the Integrated Circuit (IC) technology and changes in the design takes place in terms of reduction in transistor size, supply voltage, time to market etc. These types of complex system on Chip (Soc) devices are designed by using Electronic Design Automation (EDA) tools to meet all nonfunctional IC design constraints. The selection of EDA tool is based on the type of design analysis, IC design flow, designer domain knowledge, nonfunctional optimization constraints etc. This paper gives an overview of VLSI, FPGA & ASIC design flow, advantages, applications and few manufacturing companies of FPGA and ASIC.*

Keywords *- VLSI, IC, Mosfet, Fpga, Asic, Verilog*

I. INTRODUCTION

In today's world ,VLSI technology is playing an important role in the development of chips of small size and with less power consumption. Generally,Very Large Scale Integration (VLSI) is the process of creating an IC by combining or assembling thousands of transistors into a single chip[1]. An IC is defined as the circuit in which all the elements are inseparably associated and electrically interconnected to each other. TRANSISTOR defines transfer of resistance i.e., it is an electronic device that controls or regulates the flow of voltage or current and used to amplify or switch electronic signals.The first transistor is invented as shown in figure 1. The first IC was built by Jack Kilby in 1958 at Texas instrument with two transistors as shown in figure 2. Jack Kilby received the Nobel Prize in physics in 2000 for the invention of the IC [2].

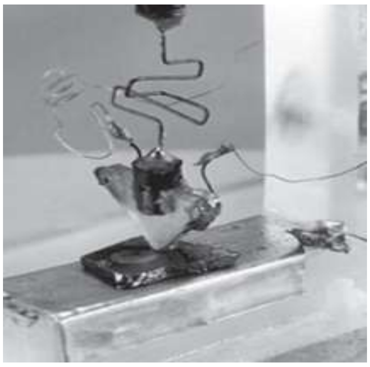

Fig 1. First Transistor

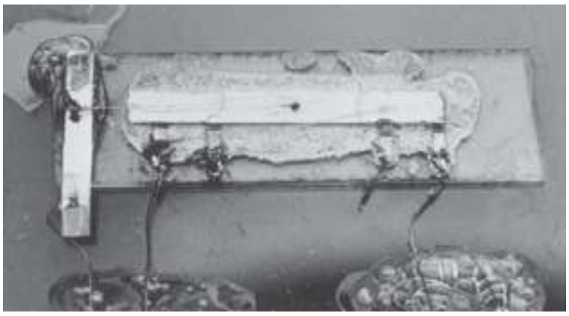

Fig 2. First IC

Basically, there are two types of transistors. They are BJT and FET. BJT's are current control devices whereas; FET's are voltage control devices. Generally, FET's are preferred over BJT's because they are cheaper, easy to manufacture and occupy less area compared to BJT's. Again FET's are classified into two types. They are JFET (Junction Field Effect Transistor) and MOSFET (Metal-Oxide-Semiconductor Field Effect Transistor). In FET's MOSFET's are preferred over JFET's because of its high input impedance. According to Moore's law as shown in figure 3, for every 18-24 months the transistor count will be doubled. Thus, in VLSI technology, the thousands of MOSFET's are combined on to a single chip thereby it reduces the size, power Consumption & area and speed increases gradually.

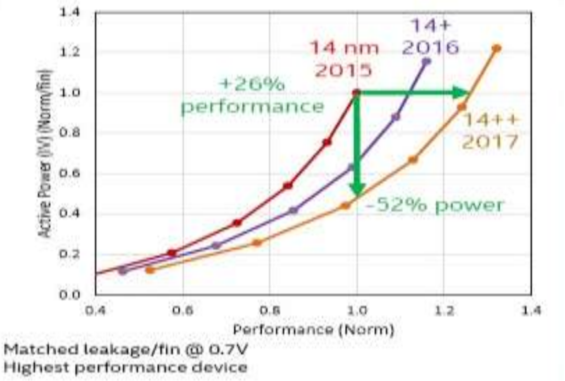

Fig 3. Moore's law graph

Advantages of VLSI

- Reduce the size of circuits.
- Reduce the cost of device.
- Increases the operating speed of circuits.
- Less power consumption.
- Occupies smaller area.
- Higher reliability.

Applications of VLSI

- Digital Signal Processing.
- Digital Image Processing.
- As memory element in computers.

A. Field Programmable Gate Array (FPGA)

- By contemporary standards a logic circuit with 20,000 gates is not large. To perform large circuits, it is easy to use a new type of chip that has larger capacity.
- Field Programmable Gate Arrays (FPGA's) accomplished in 1984 as an alternate choice to Programmable Logic Devices (PLD's) and ASIC's.
- As the name implies, FPGA offer the benefit of being readily programmable.
- FPGA's field gap between discrete logic and PLD's the lower end of complexity scale and costly custom ASIC's on the higher end.
- Just a few years ago the largest FPGA was measured in tens of thousands of system gates and operated at 40 MHZ. Older FPGA often cost more than $150 for the most advanced parts at the time.
- FPGA's needed to implement most complex designs.
- FPGA is a programmable logic device that supports performing of relatively large logic circuit.
- FPGA is termed as field programmable flexible to program functions of FPGA product even it has FPGA based product present initially.
- It can be reprogrammable according to the user specifications. FPGA structure is shown in figure 4. [3]

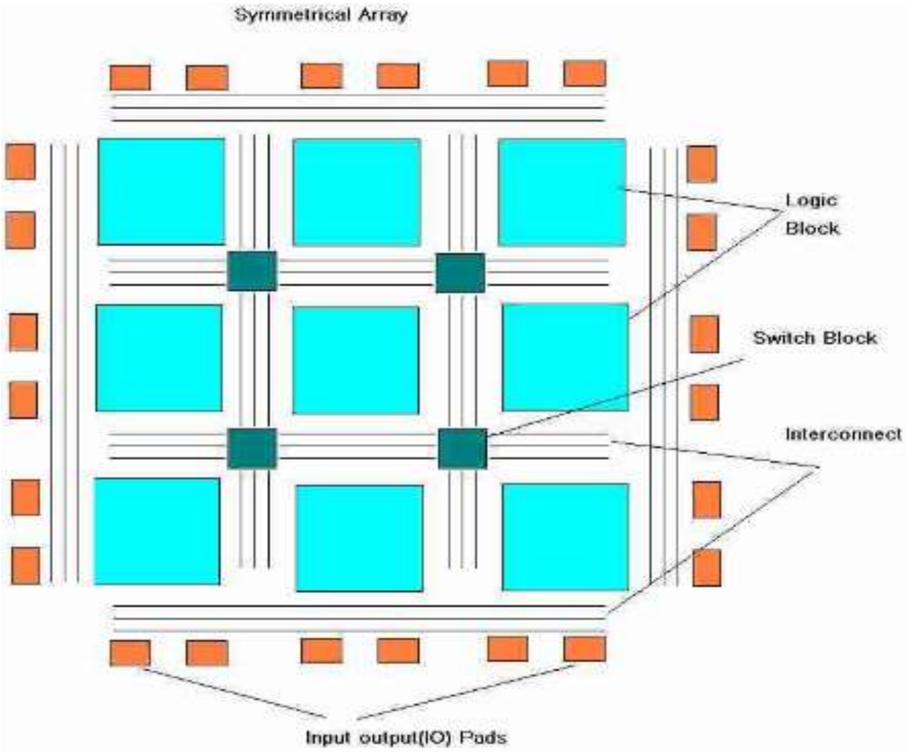

Fig 4. Design Structure of FPGA

Advantages of FPGA

- Design cycle is significantly reduced. A user can program an FPGA design in a few minutes.
- High gate density. i.e., It offers large gate count compared with PLD's**.**
- No custom masks tooling is required saving thousands of dollars (low cost).
- Re-programmability for some FPGA (design can be altered easily).
- Suitable for proto typing.

Applications of FPGA

- Low cost customizable digital circuitry.
- High performance computing performance.
- Evolvable hardware.
- Digital signal processing.
- Real time usage.
- Security systems.
- Video Image Processing.
- Wireless communications.

B. Application Specific Integrated Circuit (ASIC)

- ASIC can be defined in encyclopedic sense as an IC designed for a peculiar application or end-use.
- ASIC also define a design style or standardization which is based on the considerable use of CAD tools and systems. Classification of ASIC's is shown in the figure 5. [5]

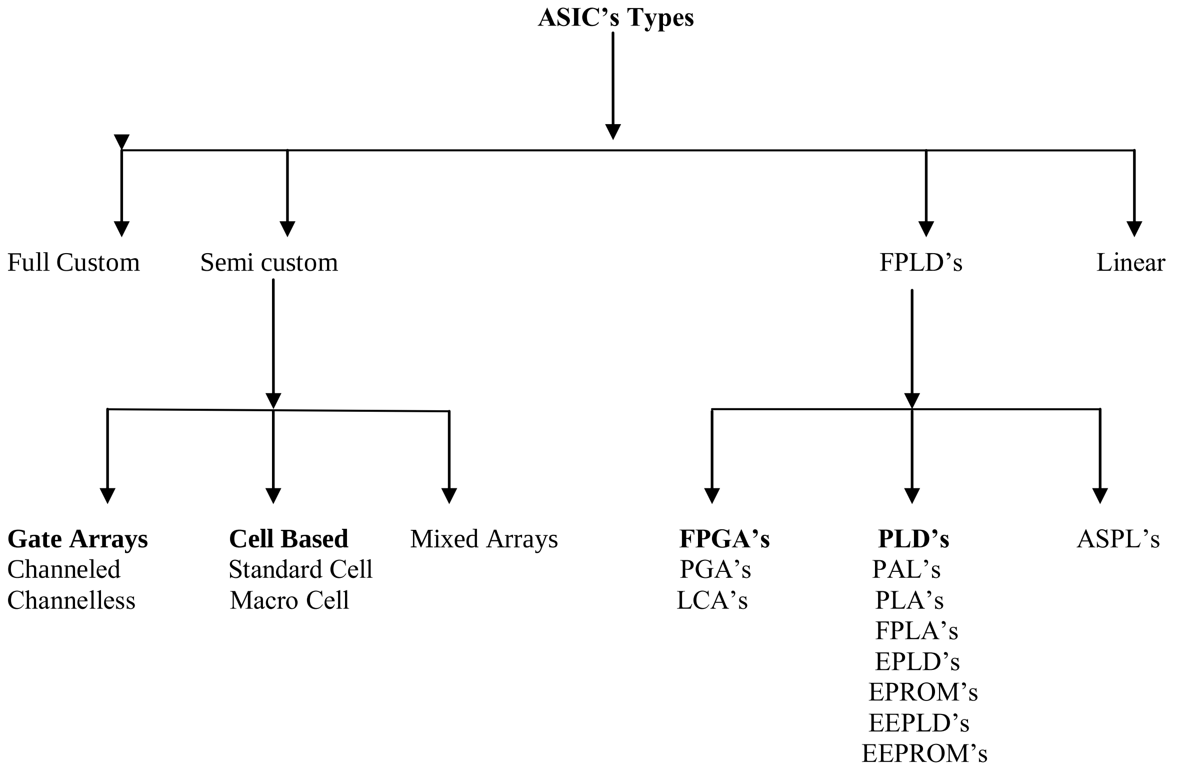

Fig 5. Classification of various types of ASIC's

Advantages of ASIC

- Full Custom Capability.
- Smaller Form Factor.
- Lower Unit Costs.
- For Very High Volume Designs.

Applications of ASIC

- In the field of Medical, Industrial Sectors.
- In the field of Automotive and Sensors.
- In Satellites, Modems, Computer Pc's, RFID Tags.
- Biometric Monitors, Hearing Aids.
- Thermal Controller, Micro-Power 555 Programmable Timer.
- 8-bit Microcontroller.
- Electronic Odometer, Engine Monitor.

II. VLSI DESIGN FLOW

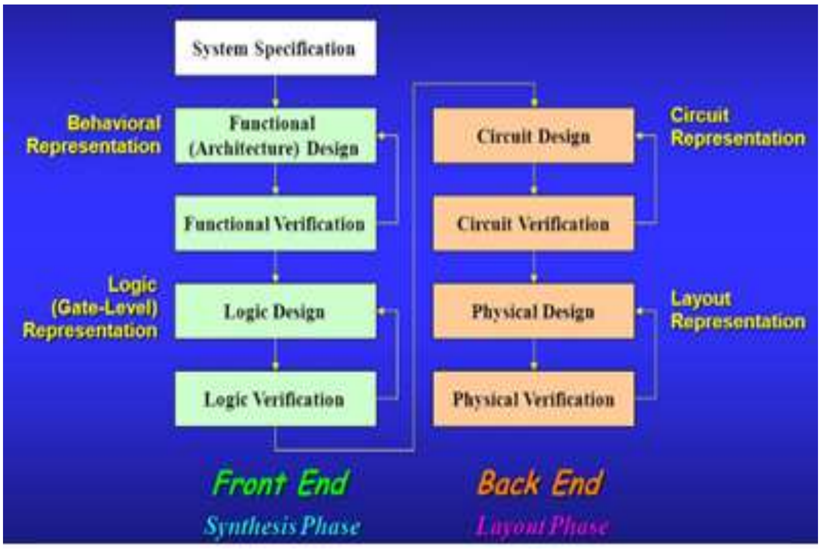

Fig 6. VLSI Design Flow

Generally, VLSI design flow is divided into two parts-

- FrontEnd design flow
- BackEnd design flow

FrontEnd Flow

FrontEnd design flow is responsible to determine a solution for a given problem and transform it into a RTL circuit description. The steps involved in frontend design flow are:

- Specifications
- Behavioral description
- RTL coding
- Functional verification

BackEnd Flow

BackEnd design flow is responsible for the physical implementation of a circuit. It converts the RTL circuit description into a physical design composed by gates and its interconnection. Steps involved in backend design flow are: [2]

- Floor planning
- Place and Route
- Fabrication and Packaging

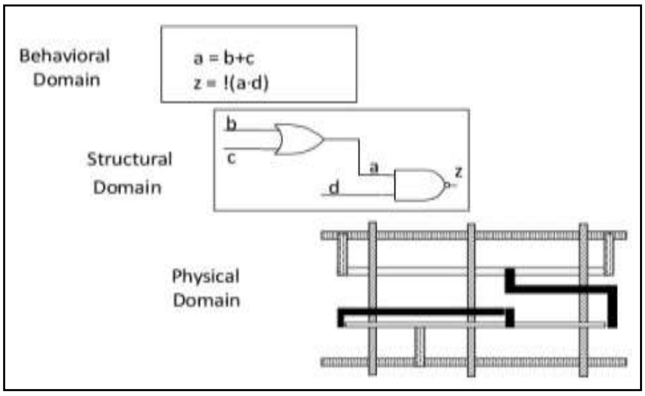

Fig 7. Domain Representations

In VLSI design process there are 3 different domains as shown in figure 7 namely,

- **Behavioral Domain:** It specifies software implementation of system functionality.
- **Structural Domain:** It specifies how modules are connected together to affect the prescribed behavior.
- **Physical Domain:** It specifies the layout used to build the system according to the architects idea from transistor level.

The steps involved in VLSI design cycle are discussed below-

Logic Design

Logic design defines the top-level chip interface and block diagram. Hierarchically all the units are decompose until leaf cells are reached. The logic is specified with HDL, which provides a higher level of abstraction than schematic or layout. This code is often called as RTL description [2].

Circuit Design

Circuit design deals with arranging of transistors to perform a particular logic function. By circuit design, the delay and power of the circuit can be estimated. The circuit can be represented as a schematic, or in textual form as a netlist. Common transistor level net list formats include Verilog and SPICE [2].

Floor Planning

Physical design begins with a floor plan. The floor plan estimates the area of major units in the chip and defines their relative placements. The floor plan is essential to determine whether the proposed design will fit in the chip area budgeted and to estimate wiring lengths and wiring congestion [2].

Routing

The routing is to locate a set of wires in the routing space that connect all the nets in the netlist. The capacities of channels, width of wires and wire crossings are need to be taken into consideration. There are two types of routings. These routings are shown in figure 8.
They are: Global Routing and Detailed Routing.

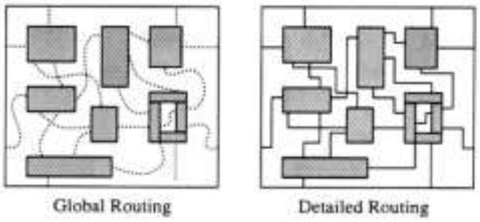

Fig 8. Routing

Placement

This step occurs after logic synthesis and before routing process. Placement is a process in which the correct positions to the blocks are assigned on the chip with no overlapping to achieve optimized circuit design.

Design Verification

Design verification step is useful for finding the errors before manufacturing takes place. Instead, the design is usually tested for functionality at the architectural level with a model in a language such as C and at the logic level by simulating the HDL description [2].

Test bench

Test bench is used to verify that the logic is correct or not. The test bench instantiates the logic under test. It reads a file of inputs and expected outputs called test vectors, applies them to the module under test and logs mismatches [2].

Testing: Testing can occur at the following levels:

- Wafer level
- Packaged chip level
- Board level, system level and field level.

To test a chip after it is fabricated, the user need a tester, a test fixture and a test program.
Tester: A tester is a device that can apply a sequence of stimuli to a chip or system under test and monitor and/or record the results of those operations. Testers come in various shapes and sizes. To test a chip, following types of test fixtures may be required. They are as follows:

- A probe card to test at the wafer level or unpackaged die level with a chip tester.
- A load board to test a packaged part with a chip tester.
- A PCB for bench level testing

Logic Synthesis

Logic synthesis transforms HDL code into a net list describing the hardware i.e., logic gates and the wires connecting them. The logic synthesizer may perform optimizations to reduce the amount of hardware required. The net list may be a text file or it may be displayed as a schematic to help visualize the circuit.

Fabrication Process

The following are some of the steps involved in fabrication process-

- **Wafer preparation**
- **Oxidation:** In this step, silicon reacts with oxygen to form silicon dioxide layer over the substrate.
- **Photolithography**
- **Etching**
- **Diffusion:** It is a process by which atoms move from a high concentration region to low concentration region.
- **Ion implantation**: It is another method used to introduce impurities into the semiconductor crystal.
- **Metallization:** The purpose of this step is to interconnect the various components to form the desired IC. Metallization involves the deposition of a metal over the entire surface of the silicon. Metal layer is normally deposited via sputtering process.

III. FPGA DESIGN FLOW

A. Design Entry

There are different techniques for design entry . Schematic based , HDL and combination of both.Selection of a method based on the design and designer. [3,4]

HDL: It represents a level of Speculation that can isolate the designers from the given details of Hardware description. This method can choose when a design is in Algorithmic way.

Schematic: It gives designer more capability of providing a clear unobstructed view into hardware. This method can choose when a design is complex or a series of state. FPGA design flow is shown in figure 9.
Design entry subdivided into following two steps:

1. New Source Wizard.
2. Language Template.

1. **New Source Wizard**

- Select the Source to create and enter name and location.
- File name. (Enter a file name for source)
- Location. (Path to the current project,which is default)
- Add to Project(Adds source to the project when check box is selected)
- Optionally,use the language templates to assist in coding of the design.
- Edit the design testbench or waveform files to drive stimulus for testing the design files.
- Assign constraints, such as timing constraints, pin assignments and area constraints.
- **MEM:** Memory Definition File(MEM). Defines the contents of the memory.
- **BMM:** Block RAM Memory map(BMM). Uses in Power Pc and MicroBlaze Processor designs to describe the organization of block RAM Memory.

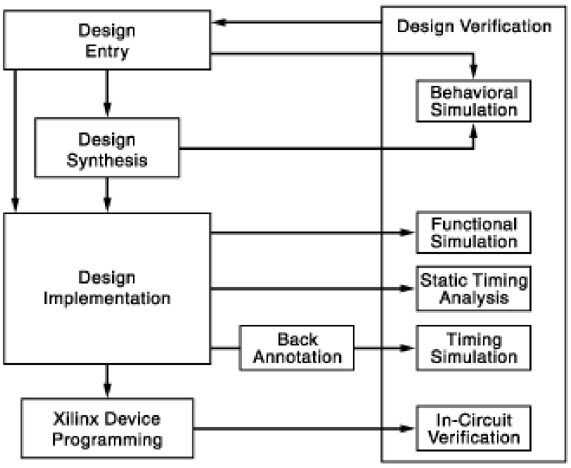

Fig 9: FPGA Design Flow

2. **Language Template**

Language Templates provides code syntax to use in source files. These templates enable easy insertion of pre-built text structures in VHDL, Verilog, ABEL, TCL or UCF souce file. There are several types of pre-built templates available, such as common language structures or instantiation templates for synthesis.[7]

- **VERILOG**

Verilog is a hardware description language (HDL). It is most commonly used language in the design and verification of digital circuits at the register-transfer level of abstraction. It is also used in verification of analog circuits and mixed-signal circuits.

- **UCF**

User constraints file (UCF). Adds the file to project.

- **ABEL**

Advanced Boolean Expression Logic (ABEL) explains input stimulus and expected outputs for logic simulation of ABEL design code.

B.Design Synthesis

This process translates VHDL or verilog code into a device netlist format i.e., logical elements with complete circuit for the given design. Netlist generates when the design contains more than one sub design. Synthesis process will check code syntax and analyze the hierarchy of design which shields that the design is optimized for design architecture or not.The resulting netlist is saved to an NGC (Native Generic Circuit) for Xilinx synthesis technology. Design synthesis is shown in figure 10. [8]

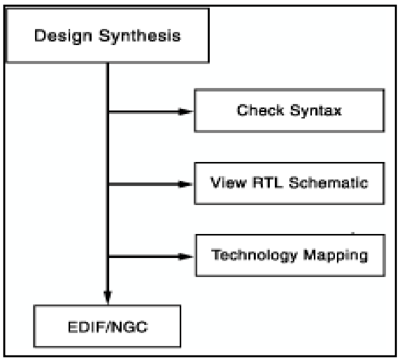

Fig 10: Design Synthesis

C.Design Implementation

This process consists of three steps

- Translate.
- Map.
- Place & route.

Translate: Which combines all the incoming netlist and constraints to a logic design file.

MAP: Process divides the circuit with logic elements into many sub blocks. So that they can fit in Logic Blocks of FPGA. Map process fits logic Blocks by Native Generic Circuit (NGD) file into FPGA element and generates output Native Circuit Description (NCD).

Place & Route: Which places and routes the design to timing constraints. This tool takes the mapped NCD file as input and gives a completely routed NCD file as output. It contains routing information.

D. Device Programming

The design must be converted to a format to load on a FPGA. BITEN Programme Deals with conversion process and Native Circuit Description (NCD) file is given to BITEN to generate a bit programmable cable, cables can be selected depending on design. There are two ways of programming : through a PROM device and directly from device.
Translate is shown in figure 11(a), Map is shown in figure 11(b), Place and Route is shown in figure 11(c). [8]

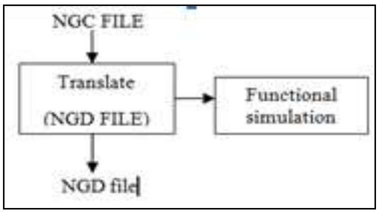

Fig 11(a) Translate

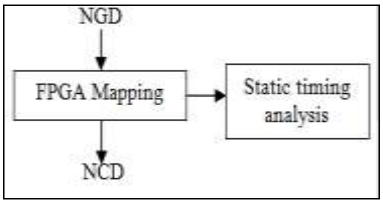

Fig 11(b) Map

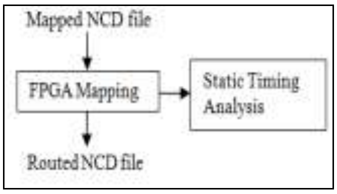

Fig 11(c) Place and Route

E.Design Verification

- **Behavioural Simulation:** This is first simulation process among all. Which are encountered by hierarchy of designflow. This simulation can be performed on VHDL or Verilog designs.
- **Functional Simulation**: It is an iterative process, performs function simulation after creating a testbench and designing a code. It gives an information about logic operation of a circuit.
- **Static Timing Analysis**: Timing analyzer is used to perform a detailed analyzer of FPGA design. This process can be done after map or place and route process. Post PAR timing report gives timing delay information to provide a comprehensivetiming of a design.
- **Timing Simulation:** Timing simulation is to check the implemented design meets all timing requirements or not.Working through timing simulation confirms that the completed design is free of defects.
  Defects that timing simulation helps to find
- Post synthesis and implementation of functionality changes
- Missing components generic for VHDL
- Operation of asynchronous paths. [7]

Manufacturing companies of Field Programmable Gate Array are shown in table 1

Table 1. Manufacturing Companies of FPGA

Companies	Percentage of Share in Market
Xilinx	51
Altera	32
Lattice Semiconducter	7.8
Actel	5.4
Quick Logic	1.4
Atmel	0.5

IV. ASIC DESIGN FLOW

Application Specific Integrated Circuit (ASIC) Design Flow

The design is tested through a simulation process. Simulation is carried out through dedicated tools. With every simulation run, the simulation results are studied to identify errors in the design description. The errors are corrected and another simulation run carried out. Simulation or changes in the design description together form a cyclic iterative process and repeated untill an error free design is evolved. [5]

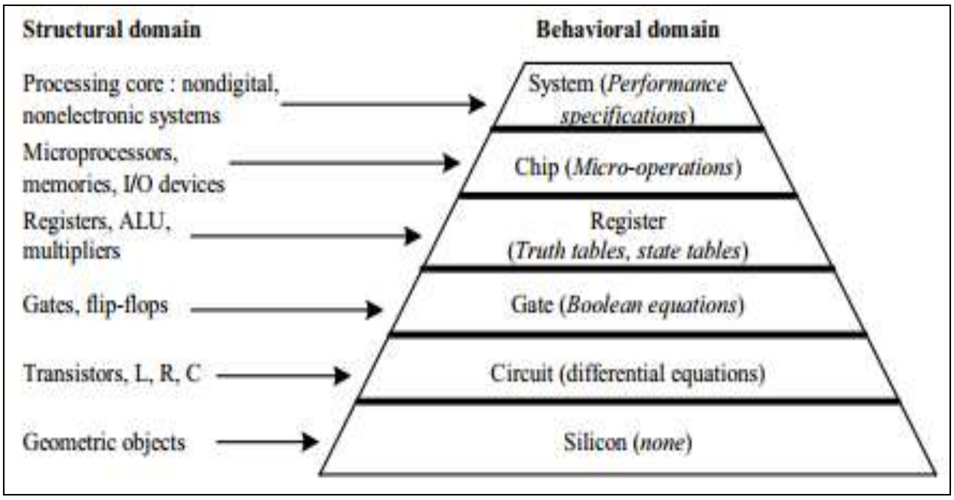
Structural domain
Behavioral domain
Processing core : nondigital, nonelectronic systems
Microprocessors, memories, I/O devices
Registers, ALU, multipliers
Gates, flip-flops
Transistors, L, R, C
Geometric objects
System (Performance specifications)
Chip (Micro-operations)
Register (Truth tables, state tables)
Gate (Boolean equations)
Circuit (differential equations)
Silicon (none)

Fig 12 :Design Domain and Levels of Abstarction.

Design description is an activity independent of the target technology or manufacturer. It results in a description of the digital circuit. To translate it into a tangible circuit, one goes through the physical design process. The same constitues a set of activities closely linked to the manufacturer and the target technology. The design domain and Levels of Abstraction are shown in figure 12. Major activites in ASIC Design are shown in figure 13. [5,9]

ASIC's are broadly classified into three types they are:

- Full –Custom ASIC's.
- Semi-Custom ASIC's.
- Programmable ASIC's.

Full-Custom ASIC's: A full custom ASIC is one which includes some logic cells that are customized and all mask layers that are customized**.** A micro processor is an example of afull custom IC. Full custom IC's are the most expensive to manufacture and to design . The manufacturing lead time (the time required just to make an IC not including design time) is typically eight weeeks for a Full-Custom IC.

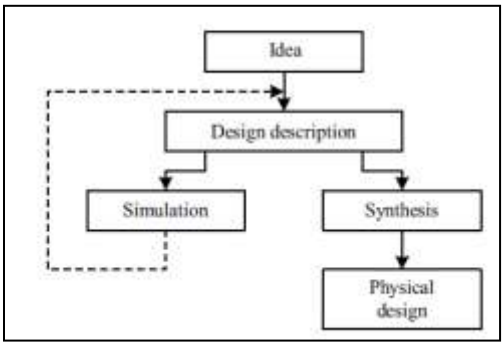

Fig 13: Major activities in ASIC Design

Semi-Custom ASIC's: ASIC's for which all of the logic cells are pre-designed and some of the mask layers are customized are called Semi-Custom ASIC's. Using the pre-designed cells from a cell library makes the design,
much easier. There are two types of Semi- Custom ASIC's (i) Standard cell based ASIC's . (ii) Gate Array based ASIC's.

Standard cell based ASIC's: A cell-Based ASIC uses pre-designed logic cells (AND gates ,OR gates,Multiplexers,and flip-flops).

Gate Array based ASIC's: In a gate array the transistors are pre-defined on the silicon wafer.The logic cells in a gate array library are often called Macros.There are three types of gate array based ASIC's

- Channeled gate arrays.
- Channelless gate arrays.
- Structured gate arrays.

Channeled gate arrays (CGA): A channel gate array is similar to a CBIC. Both use the rows of cells seperated by channels used for interconnect. One difference is that the space for interconnect between rows of cells are fixed in height in a channeled gate array.

Channelless gate arrays (CLGA): The routing on a channelless gate array uses rows of unused transistors. The key difference between a CGA & CLGA is that there are no pre-defined areas set aside for routing between cells on a channelless gate array. [5]

Structured gate array: This design combines some of features of CBIC's and MGA's. It is also known as an embedded gate array or structured gate array.

Programmable ASIC's: Major PLD's are shown in figure 14

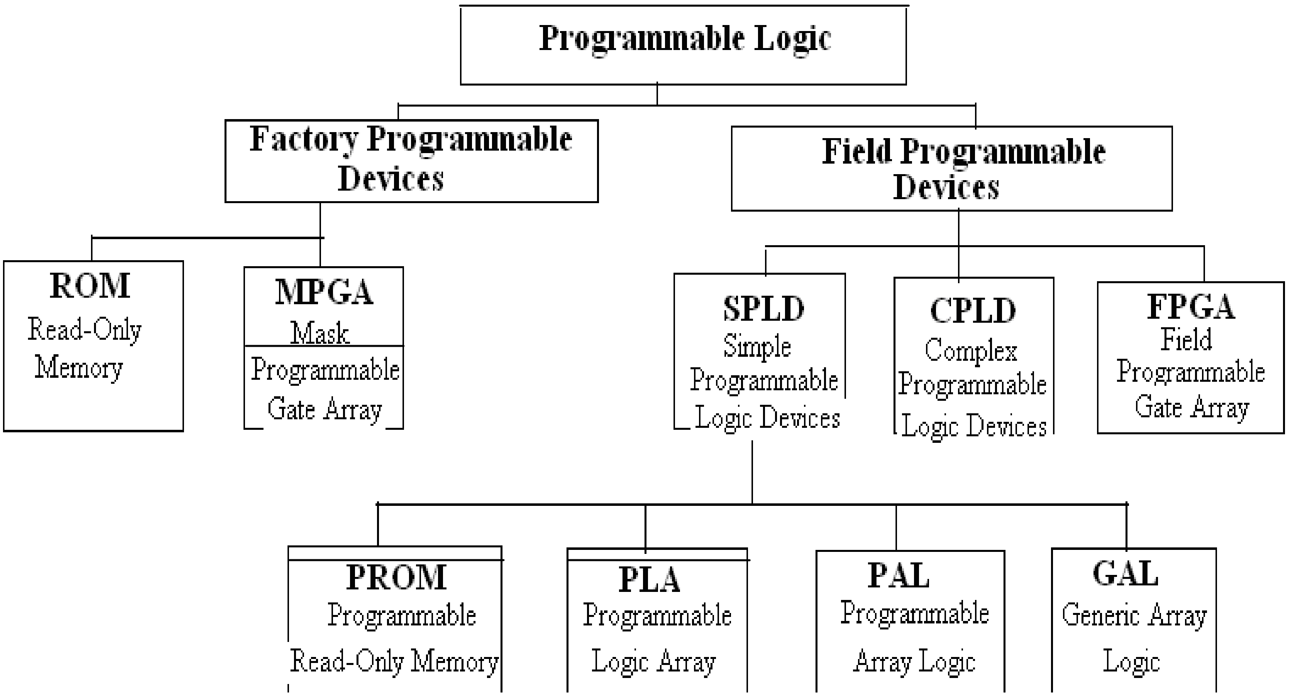
Programmable Logic
Factory Programmable Devices
Field Programmable Devices
ROM Read-Only Memory
MPGA Mask Programmable Gate Array
SPLD Simple Programmable Logic Devices
CPLD Complex Programmable Logic Devices
FPGA Field Programmable Gate Array
PROM Programmable Read-Only Memory
PLA Programmable Logic Array
PAL Programmable Array Logic
GAL Generic Array Logic

Fig 14: Major PLD's.

Manufacturing companies of ASIC

- **Cadence**
- **Synopsis**

V. CONCLUSION

In Today's world VLSI circuits are present every where i.e., electronic gadgets, communications, signal processing etc.,The EDA tools are used to design System on Chip (Soc) applications with the help of Digital ICs, Analog IC's and Mixed signal IC's. In this paper the design procedure of FPGA, VLSI & ASIC are discussed. The major PLD's are also discussed. The FPGA Xilinx and Mentor Graphics tools, ASIC Cadence tools are used for Analog, Digital and Mixed signal designs with the help of HDL entry, schematic entry and other options such as Physical design approach to meet the present day System on Chip (Soc) requirements.

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