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COMPARISON BETWEEN 3 LEVEL AND 5 LEVEL DIODE CLAMPED INVERTER

Kunjal Solanki[1], Krina Talati[2], Amit Panchal[3]

[1]P.G Student, [2] P.G Student, [3]Assistant Professor
Electrical Engineering Department
Parul Institute of Engineering and Technology

Abstract —*Multilevel began with the three level inverter. Use of conventional two – level pulse width modulation (PWM) inverter provide less distorted current and voltage but at cost of higher switching losses due to high switching frequency. Multilevel inverter is emerging as a viable alternative for high power, medium voltage application. This paper compares total harmonics distortion in three level and five level diode clamped multilevel inverter. Diode –clamped three phase topology is considered for study. A sinusoidal PWM technique is used to control the switches of the inverter. Simulation study confirms the reduction in harmonics distortion.*

Keywords- *Harmonics, multilevel inverter, pulse width modulation, Total harmonics distortion.*

I. INTRODUCTION

Multilevel inverter is based on the fact that sine wave can be approximated to a stepped waveform having large number of steps. The steps being supplied from different DC levels supported by series connected batteries or capacitors. The unique structure of multi- level inverter allows them to reach high voltages and therefore lower voltage rating device can be used. As the number of levels increases, the synthesized output waveform has more steps, producing a very fine stair case wave and approaching very closely to the desired sine wave. Total harmonic distortion is defined as the ratio between the RMS value of the harmonics and the RMS value of the fundamental. For example, if a nonlinear current has a fundamental component of I_1 and harmonic components of I_2, I_3,I_4…., then the RMS value of the harmonics is:

$I_H = \sqrt{I_2^2 + I_3^2 + I_4^2 + \cdots}$

THD is expressed as,

$THD = \left(\frac{I_H}{I_1}\right) \times 100$

The harmonic frequency currents generated in power conversion equipment can be stated as :

$n = kq+1$

Where n is the significant harmonics frequency, k is any positive integer (1,2,3 etc.),and q is the pulse number of the power conversion equipment which is the number of power pulses that are in one complete sequence of power conversion. For example , a three phase full bridge inverter has six power pulses and so has a pulse no of six the following significant harmonics may be generated:

For k = 1, n=(1× 6) ± 1 =5^{th} and 7^{th} harmonics.

For k = 2, n=(2× 6) ± 1 =11^{th} and 13^{th} harmonics.

With six pulse power conversion equipment, harmonics below the 5^{th} harmonic are significant. So, typically, for six pulse power conversion equipment, the 5^{th} harmonic current would be the highest ,the 7^{th} would be lower than the 5^{th} ,the 11^{th} would be lower than the 7^{th} ,and so on as below:

$I_{13} < I_{11} < I_7 < I_5$

When using 12 pulse power conversion equipment, harmonics below the 11^{th} harmonic can be made significant. The total harmonic distortion is also reduced [1].

II. MULTILEVEL INVERTER TOPOLOGIES

A. Diode Clamped Multilevel Inverter

The first invention in multilevel converters was the so-called neutral point clamped inverter. It was initially proposed as a three level inverter. It has been shown that the principle of diode clamping can extended to any level [6].

The main advantages and disadvantages of this topology are:

Advantages

1. High efficiency for the fundamental switching frequency.
2. The capacitors can be pre-charged together at the desired voltage level.
3. The capacitance requirement of the inverter is minimized due to all phases sharing a common DC link.

Disadvantages

1. Packaging for inverters with a high number of levels could be a problem due to the quadratically relation between the number of diodes and the numbers of levels.
2. Intermediate DC levels tend to be uneven without the appropriate control making the real power transmission a problem.
3. Uneven rating in the diodes needed for the converter.

Applications

1. An interface between High voltage DC transmission line and AC transmission line.
2. High power medium voltage variable speed drives.
3. Static VAR compensation.

B. Flying-Capacitor Multilevel Inverter

As an alternative for the diode clamped inverter is the capacitor clamped inverter proposed by Meynard and Foch, which shared many of the advantages.
The structure of the capacitor clamped inverter is similar to that of the diode clamped converter. The main difference is that the diodes used for the clamping are replaced by capacitors. For this topology the most common application is static VAR generation.

C. Cascaded Multilevel Inverter

The cascaded multilevel inverter is based on the series connection of single leg or double leg (H bridges) inverters with separate DC sources or capacitors. For each of these two types of configurations several states exist regarding to the switches states. The single leg unit, has 2 states for each of the two possible current(s) directions while the double unit has 4 states.
The series connection between the modules has a capacitor that is charged and discharged by a controlled DC current. The resultant voltage waveform is made by the addition of the voltage generated in each module that is connected [2].

III. PULSE WIDTH MODULATION

Pulse Width Modulation refers to a method of carrying information on a train of pulses, the information being encoded in the width of the pulses. The pulses have constant amplitude but their duration varies in direct proportion to the amplitude of analog signal. PWM is the most popular method for producing a controlled output for inverters. They are quite popular in industrial applications. The modulation techniques used for high switching frequency PWM are Space vector modulation (SVM) and Sinusoidal PWM.

A. Sinusoidal PWM

In this modulation technique there are multiple numbers of output pulses per half cycle and pulses are of different width. The width of each pulse is varying in proportion to the amplitude of a sine wave evaluated at the centre of the same pulse. Carrier Based Pulse width modulation (CBPWM) or SPWM technique has been extensively used, because it improves the harmonic spectrum of the inverter by moving the voltage harmonic components to higher frequencies The gating signals are generated by comparing a sinusoidal reference with a high frequency triangular signal.

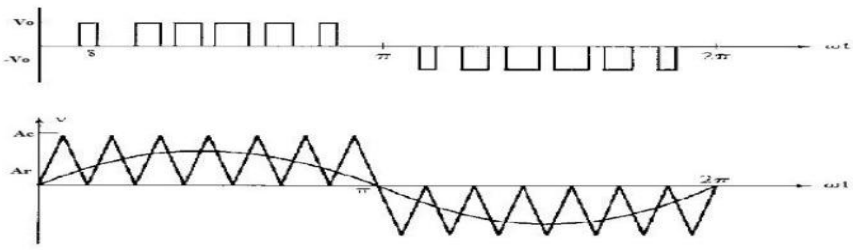

Figure 1. Sinusoidal pulse width modulation

IV. DESIGN AND SIMULATION OF THREE-LEVEL DIODE CLAMPED INVERTER

The three-level inverter topology is being widely used in high voltage, high power applications due to its high voltage handling and good harmonic rejection capabilities with currently available power devices. Figure 2 shows the basic circuit diagram of a three-level inverter excluding detailed snubber circuit. It is known that the three-level inverter roughly improves by a factor of four the harmonics content compared with conventional two-level topology having the same number of devices and ratings. Various PWM techniques for control of three-level inverter have been studied, such as, modified two-level triangular carrier modulation, cost function minimizing PWM and space vector PWM.

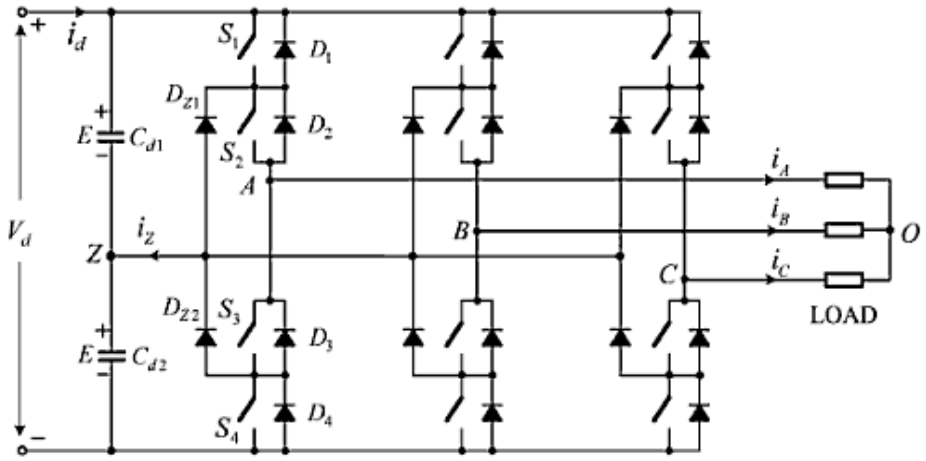

Figure 2. Three Level diode clamped inverter

In the proposed configuration, a three- level diode clamped inverter is used. It is controlled by a sinusoidal pulse width modulation scheme. An m level inverter leg requires 2(m-1) switching devices and (m-1)(m-2) clamping diodes. For a three-level inverter, m=3, so it needs four switching devices and two clamping diodes per leg as shown in Figure 2.

1. For an output voltage of Va = Vdc, all the upper-half switches of a-phase leg are turned ON, i.e., S1 and S2 are ON.
2. For output voltage of Va = Vdc/2, only S2 and S3 are ON.
3. For output voltage of Va = 0, all the lower-half switches of a phase leg are turned ON, i.e., S3 and S4 are ON.

Table 1 shows the voltage levels at their corresponding switch states. State condition "1"states that the switch is ON, and state "0" means the switch is OFF. It should be noticed that there are two complementary switch pairs. These pairs for one leg of the inverter are (S1, S3) and (S2, S4).

Table 1. Switch states for various voltages of a phase leg

Voltage level Va=	**SA1**	**SA2**	**SA3**	**SA4**
Vdc	1	1	0	0
Vdc/2	0	1	1	0
Zero	0	0	1	1

Thus, if one of the complementary switch pairs is turned ON, the other of the same pair must be OFF. Two switches are always turned ON at the same time. For m-level Diode Clamped inverter, each switching device is only required to block a voltage level of Vdc/(m-1). For switching devices unequal conduction duty requires at different current ratings. Therefore, if the inverter design uses the average duty cycle to find the device ratings, the upper switches may be over sized, and the lower switches may be undersized [7-8].

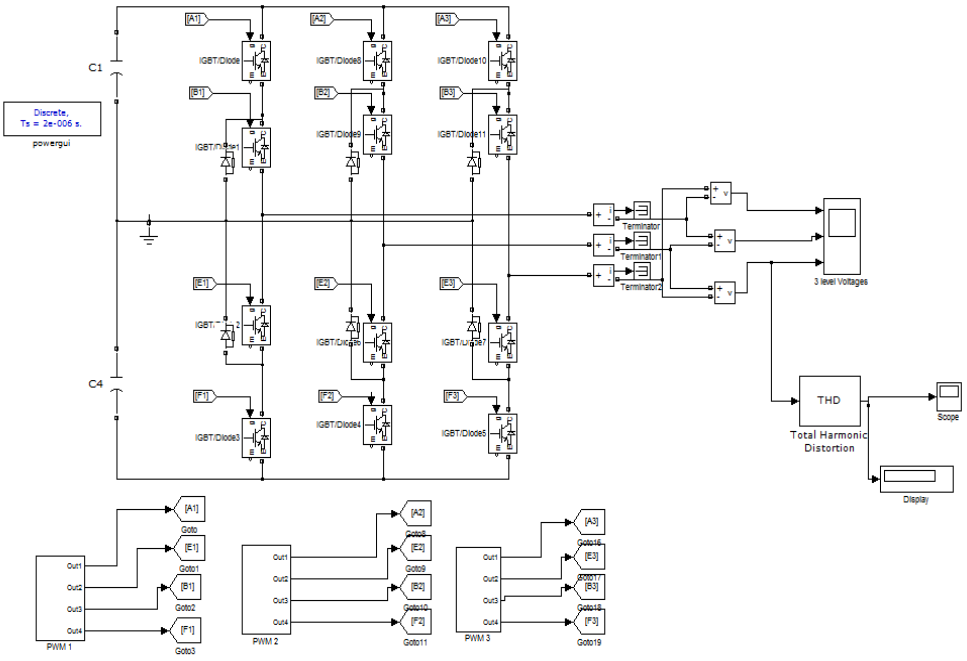

Figure 3. Simulation diagram of a three level inverter

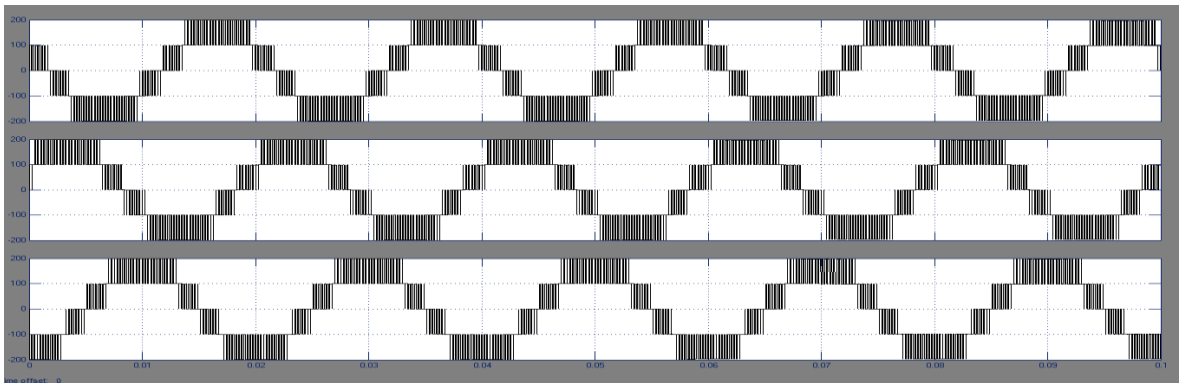

Figure 4. Output voltage waveform of a three level inverter

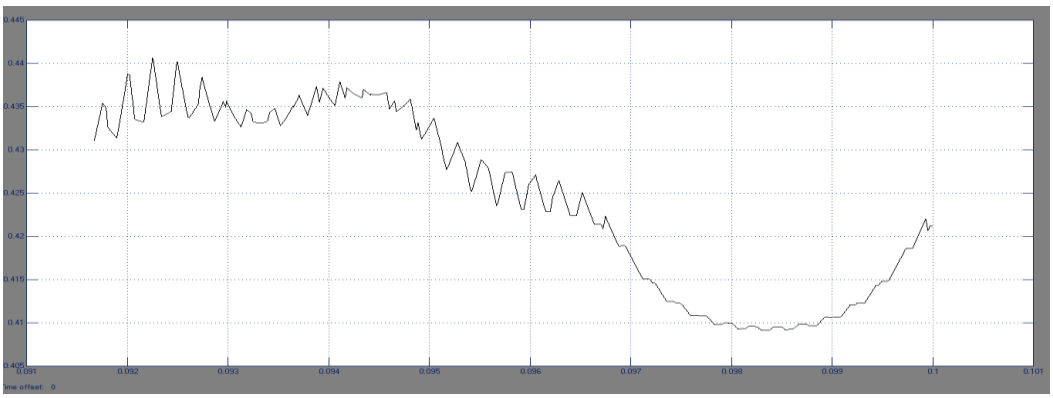

Figure 5. Total harmonic distortion of a three level inverter

V. DESIGN AND SIMULATION OF FIVE-LEVEL DIODE CLAMPED INVERTER

The diode-clamped multilevel inverter uses capacitors in series to divide up the dc bus voltage into a set of voltage levels. M-level diode-clamp inverter needs m-1 capacitors on the dc bus to produce m levels of the phase voltages. A 3-phase 5-level diode-clamped inverter is shown in Fig. 6.

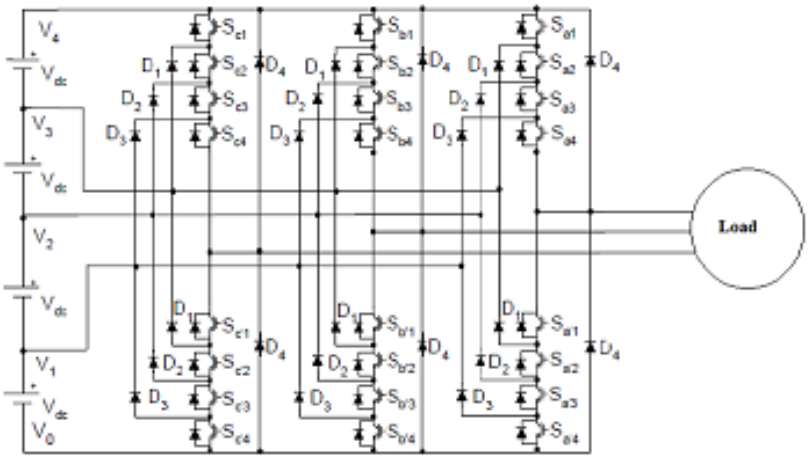

Figure 6. Five level diode clamp inverter

Table 2 . Switch states for various voltages of a phase leg

Output VAO	Sa 1	Sa 2	Sa 3	Sa 4	Sa' 1	Sa' 2	Sa' 3	Sa' 4
V5=Vdc	1	1	1	1	0	0	0	0
V4=3Vdc /4	0	1	1	1	1	0	0	0
V3=Vdc/ 2	0	0	1	1	1	1	0	0
V2=Vdc/ 4	0	0	0	1	1	1	1	0
V1=0	0	0	0	0	1	1	1	1

The dc bus consists of four capacitors, i.e., C1, C2, C3, and C4. For a dc bus voltage Vdc, the voltage across each capacitor is Vdc/4, and each device voltage stress will be limited to one capacitor voltage level, Vdc/4, through clamping diodes. DCMI output voltage synthesis is relatively straight forward. Thus, if one of the complementary switch pairs is turned ON, the other of the same pair must be OFF. Two switches are always turned ON at the same time. For m-level Diode Clamped inverter, each switching device is only required to block a voltage level of Vdc/(m-1). For switching devices unequal conduction duty requires at different current ratings. Therefore, if the inverter design uses the average duty cycle to find the device ratings, the upper switches may be over sized, and the lower switches may be undersized [7].

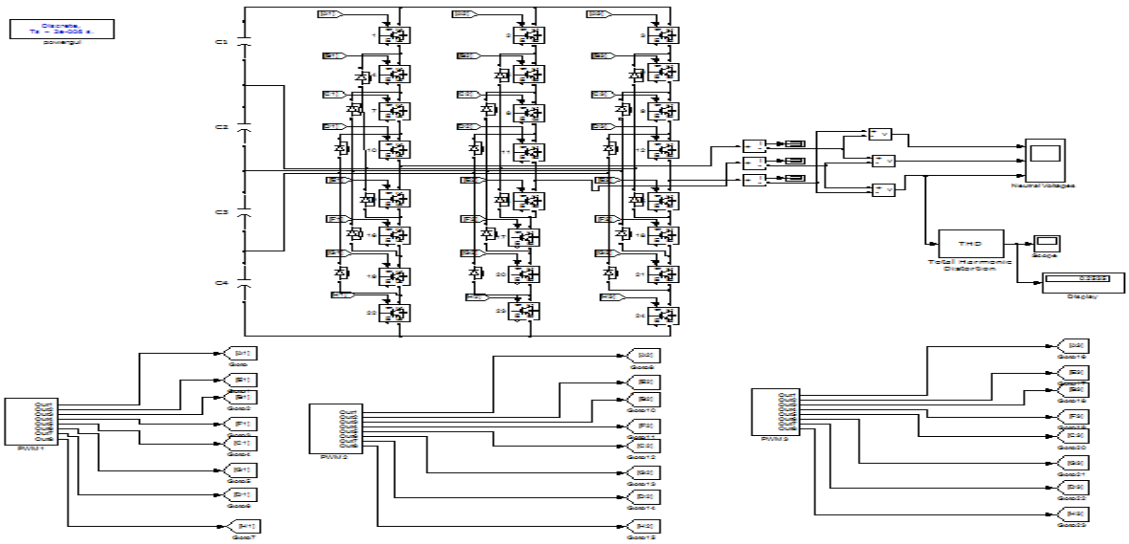

Figure7. Simulation diagram of a five level inverter

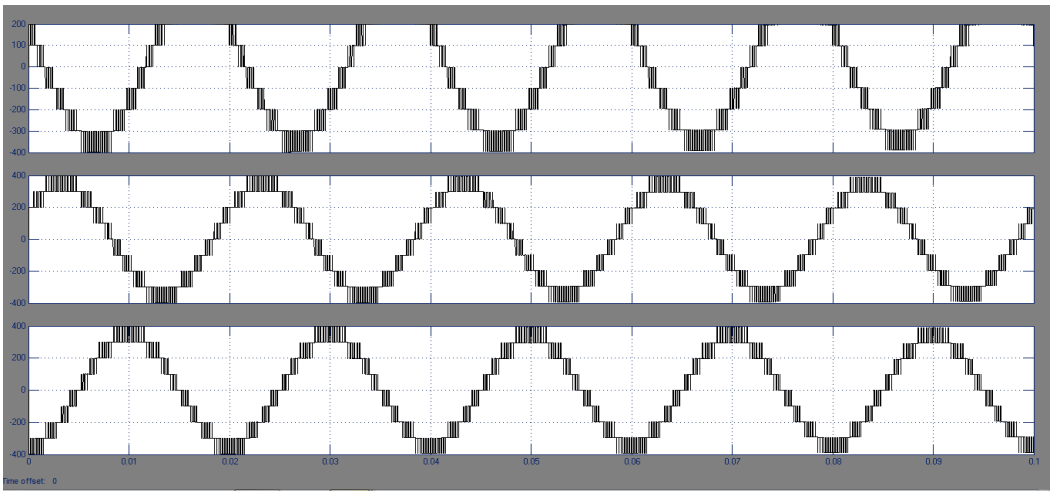

Figure 8. Output voltage waveform of a five level inverter

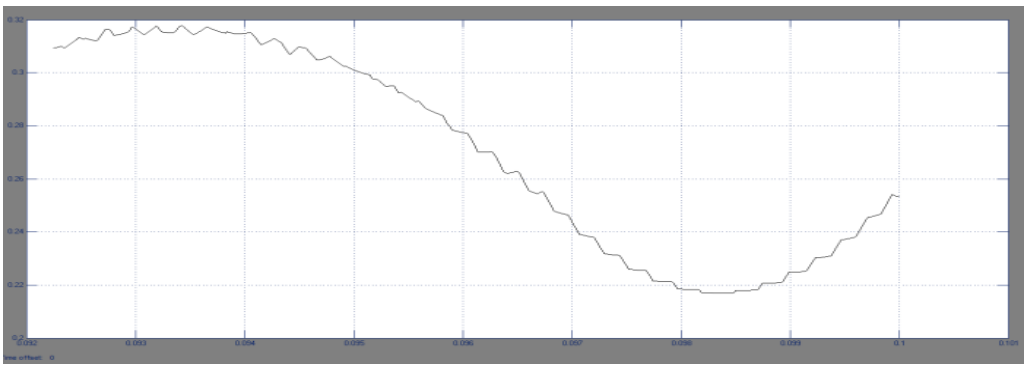

Figure 9. Total harmonic distortion of a three level inverter

Table 3. Comparison of THD values

Configuration	THD value
3-level	0.4211
5-level	0.2535

VI. CONCLUSION

Using 3-level power conversion equipment, harmonics below the 11th harmonic can be made insignificant. The total harmonic distortion is considerably reduced than conventional.3 level power conversion equipment costs more than conventional six pulse power equipment. Where harmonic currents are the primary concern, 5 level power conversion equipment may be considered. From table 3, it can be observed that, the harmonic distortion is less as we increase number of pulses. Harmonic distortion is very less for 5 level converter. Where harmonic currents are the primary concern 5 level converter may be considered.

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