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Design and Implementation of class AB VGA in deep sub micron technology

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Abstract— A variable gain amplifier (VGA) is an indispensible building block in many communication systems. In communication receiver, VGA is typically employed in a feedback loop to realize an automatic gain control (AGC). In this paper class AB VGA consisting of a linear transconductor amplifier and a linear transimpedance amplifier, is designed, analyzed and simulated in GENERIC 0.13um CMOS process(pre-layout and post-layout simulation is done) using Mentor Graphics Tool. The simulation results shows that, the modified VGA has bandwidth of 1660MHz and gain of 66.01 dB and power dissipation is less than 100uW at 1.2v supply voltage. The results show that the circuit is capable of working with high linearity and wide bandwidth by varying Rf and Rs. The modified class AB VGA is appropriate for low power, UWB applications.

Keywords- variable gain amplifier (VGA), CMOS, Automatic gain control(AGC), DVGA, AVGA, Wide Bandwidth UWB

I. INTRODUCTION

VGA is essential building block in automatic gain control system (AGC). Variable gain amplifier is signal conditioning amplifier with electronically settable voltage gain. VGA is used to maximize the dynamic range of overall system by maintaining a fixed voltage output for various input signals at the receiver in many communication systems, medical equipments, hearing aids, disk drives, and others.[1]-[6] . VGA play the important role of stabilizing the amplitude of the output signal under various conditions [5]. To design CMOS VGA, there are two approaches used to realize VGAs depending on whether the control signal is digital or analog. The digitally controlled VGAs use a series of switchable resistors or switched-capacitor techniques to control gain whereas analog controlled VGAs (AVGAs) adopt a variable transconductance or a variable resistance to control the gain [8].

In digitally controlled VGAs (DVGAs), gain varies as a discrete function of the control signal, which can lead to discontinuous signal phases that can cause problems in many systems. In order to reduce the amount of jumps, a large number of control bits are required with digitally controlled VGAs. Therefore, for applications that require smooth gain transitions, the VGAs controlled by analog signal are preferred. VGAs are available in dc to gigahertz frequencies and variety of I/O configurations. Indeed, class AB has become very significant alternative for any application requiring VGA over the last few years [6-7].

VGA, as well as other circuits, are required to operate with low power supply voltage and low power consumption. As the process technologies develop, the maximum allowable supply voltage will scale down. It is inevitable that most low power integrated circuits will have to operate with power supply voltages between 1 V to 1.5 V. It is very challenging to design a VGA with high linearity and wide bandwidth with low supply voltage and low power consumption. In addition, VGA is generally required to maintain high linearity and low noise over the entire bandwidth and gain range. It is also important that the bandwidth of the amplifier remains constant when the voltage gain is varied and this can be obtained by employing current-mode techniques [9].

At present, current mode-technique has been extensively implemented in designing a VGA. A circuit using the current-mode technique has many advantages, such as, larger dynamic range, higher bandwidth, greater linearity, simpler circuitry and lower power consumption. In class-AB operation, each device operates the same way as in class B over half the waveform, but also conducts a small amount on the other half. As a result, the region where both devices simultaneously are nearly off is reduced. The result is that when the waveforms from the two devices are combined, the crossover is greatly minimized or eliminated altogether. The exact choice of quiescent current, the standing current through both devices when there is no signal, makes a large difference to the level of distortion and to the risk of thermal runaway that may damage the devices. Often the bias voltage applied to set this quiescent current has to be adjusted with the temperature of the output transistors [9].

Since its operation is limited at class-A amplifier, signal swing is small compared to class -AB amplifier [10]. This paper presents an improved VGA to the circuit designed by P. Khumsat et. al [10]. It will be shown that the proposed circuit operates in class-AB manner outperforms its predecessor (class -A), especially, in terms of signal swing and linearity while maintaining the same static power dissipation and silicon area [11]. So in VGA, class AB amplifier is widely used.

A number of class AB VGA have been designed so far to achieve high linearity and wide bandwidth with acceptable power dissipation. However, researchers experienced gain limitation issues in wide bandwidth and the transistor's size as well. P. Khumsat et. al implemented a low cost, low power and highly reliable class AB VGA in CEDEC 0.18µm CMOS process [10]. The research showed that in designing a 100MHz VGA under 1V power supply, the highest frequency response (gain) is 33dB. However, it suffers from instability at high frequencies as mentioned before.

In this research, a low voltage class AB VGA is designed to attain the VGA with high dynamic range, high linearity and wide bandwidth with low power supply and low power consumption. This design overcomes the limitations of the conventional class AB VGA. Current mode technique has been used in this design to achieve better circuit performance. Small size of transistor is used in this design to reduce the size of circuit and cost as well. The proposed class AB VGA amplifier is designed in GENERIC 0.13µm process. Simulations results show that the modified low voltage class AB VGA performs better than the sense amplifier designed by P. Khumsat et. al.The amplifier output stage is an important part of an operational amplifier, as it is the stage that delivers the input signal to the load. In a well-designed two or three- stage operational amplifier it is also the stage which consumes most of the amplifier biasing current and ultimately sets limits on linearity of the amplifier and its maximum tolerated capacitive load. When the operating environment of an amplifier requires it to drive low ohmic resistive loads, high current source loads or large capacitive loads, the output stage must be able to source and sink currents that greatly exceed its biasing current. In practice this requires some kind of common drain-based class AB output stage, as shown conceptually in Fig. 1, at least in a low voltage environment, in order not to degrade the available dynamic range any further.

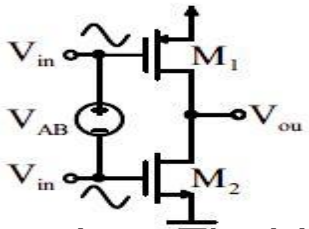

Figure 1: A conceptual common drain stage-based class AB output stage.

III. TWO STAGE CURRENT MODE VARIABLE GAIN AMPLIFIER

The previously proposed VGA in [10] has shown its versatility and potential to operate at low supply voltage, low power consumption with high bandwidth while maintaining good degree of dynamic range and occupying small silicon area. This VGA's architecture is presented in Fig . 2, which is a cascade of a linear transconductance cascaded and a linear transimpedance amplifier with shunt-feedback resistors

(R_f).

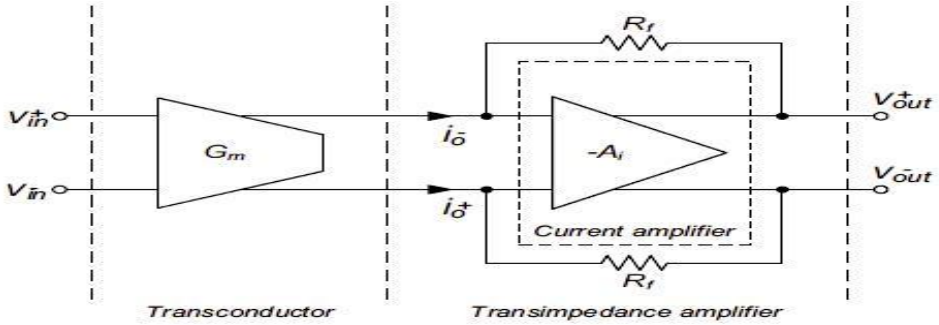

Figure 2: Architecture of the proposed VGA stage in [10].

This allows constant bandwidth when varying the voltage gain. The voltage gain of the VGA circuit is the product of the transconductance gain (G_m) and the transimpedance gain (R_m). The transimpedance gain is given by

$$R_m = \frac{(R_f A_i - R_{in})}{1+A_i} \qquad (1)$$

where R_{in} and A_i, respectively, are the input resistance and the current gain of the current amplifier. Note that, when Ai >> 1, we have $R_m \approx -R_f$. There, a linear Gm and a high- gain current amplifier are required to realize a high-linearity VGA. The proposed VGA circuit realization in CMOS is also depicted in Fig. 3. The circuit is very compact; however it has a bandwidth limitation at which the bandwidth is restricted to 1660MHz and using the big size of transistor. Table 1 shows parameter or size of transistor that have been used in previous circuit.

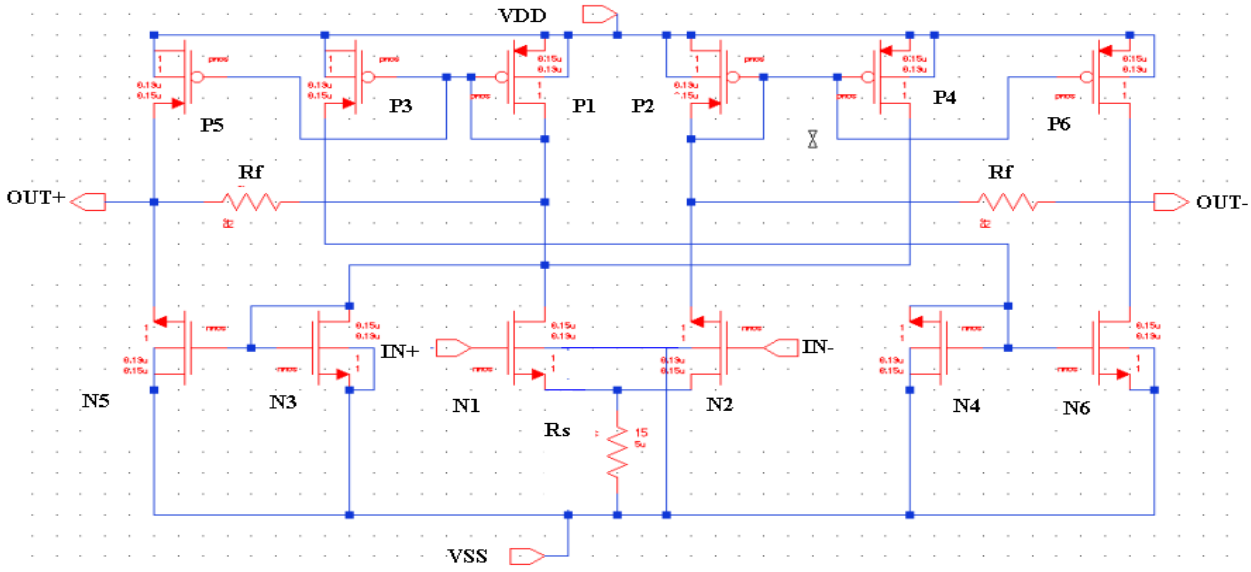

Figure 3: Circuit realization of the proposed circuit [10] with CMOS

Fig. 4 shows the circuit implementation of the proposed VGA cell, which combines a source degeneration differential input transconductance amplifier (N1 – N2, R_s) and a current-mode transimpedance amplifier (P1 – P6, N3 – N6) in order to maximum transconductance/bias current efficiency and minimize supply voltage and noise [13-14] . Cascaded current mirrors are used to implement the DC current sources. Despite these advantages, such structure possesses a serious drawback in being unable to reject common-mode signal. The second stage mirror -based current amplifier (P1 –

P6, N3 – N6) resolves this problem by employing feed forward technique that allows differential signals to be constructively combined while on the other hand cancel a common-mode signal [15-16]. This current amplifier combined with feedback resistors Rs form a transimpedance amplifier necessary for current-to voltage conversion. Moreover, such output stage also provides a class-AB operation allowing larger signal swing compared to its predecessor presented in [17-18]. Thus the major advantage of such VGA circuit is its ability to offer excellent signal linearity without sacrificing the original advantages on both aspects of the power consumption and circuit complexity.

It is important to note that the size of each transistor is reduced according to the ratio (W/L) to get a smaller size of IC. Besides that, the number of resistor Rs that have been used in previous circuit is also reduce from 2 to 1.Table 2 shows the comparison size of transistor between this work and previous circuit.

Table 2
Comparison of VGA transistors

Transistor	W/L(um/um)of this work	W/L(um/um)of circuit in [10]
N1-N2	1.5/0.18	0.5/0.13
P1-P2	3.6/0.18	2.4/0.13
P3-P6	9/0.18	7.6/0.13
N3-N6	1.8/0.18	1.2/0.13

A small-signal transconductance of the first stage is simply expressed as

$$G_m = \frac{gin}{(1+g_m R_s+sR_sC_{gs})} \quad (2)$$

where g_m and C_{gs} are respectively transconductance and gate source capacitance of N1 and N2. The amplifier differential current gain A_i and input resistance R_{in} have been analyzed to be

$$A_i = \frac{g_{mx}}{g_{mi}+sC_x}\left(1+\frac{g_{my}}{g_{my}+sC_y}\right) \quad (3)$$

$$R_{in} = \frac{1}{g_{mi}+sC_x} \quad (4)$$

where g_{mi}, g_{mx} and g_{my} are transconductance of P1 – P2, P3 – P6 and N3 – N6 respectively. The parameters C_x and C_y are equivalent total capacitance (referred to ground) at gates of P1 (P2) and N3 (N4) whose values are mainly contributed from gate-source capacitance. At low frequency, since $g_{mx} = g_{mi}(\alpha/2)$, thus A_i of Fig. 4 equals to α, which is the same as what obtained from the original circuit in Fig. 3. Thus, by substituting (3) and (4) into (1), a small-signal transimpedance gain could be obtained to be

$$R_m = \frac{-\alpha\left[2R_f - \frac{1}{g_{mx}} + s\frac{C_y}{g_{my}}\left(R_f - \frac{1}{g_{mx}}\right)\right]}{2\left[1+\alpha+s\left(\frac{C_y}{g_{my}}\left(1+\frac{\alpha}{2}\right)+\frac{C_x}{g_{mi}}\right)+s^2\frac{C_xC_y}{g_{mi}\,g_{my}}\right]} \quad (5)$$

The feedback resistor R_f is selected to set a voltage gain range whereas a source degeneration resistor R_s is tuned to vary the amplifier gain. The minimum value of Rs sets the maximum gain for a specific gain range (as previously set by R_f) and it also defines the maximum static current consumed by the VGA. The similar technique proposed in [19] can be used to tune the grounded resistor R_s.

V. RESULT AND DISCUSSION

The improved class AB VGA circuit with a single 1.2V power supply voltage have been designed and

simulated in GENERIC 0.13-µm CMOS process. Simulations were executed to evaluate the circuit performance of the modified class AB VGA with the previously reported class AB VGA [10].With $\alpha = 5$, transistor sizing of the VGA circuit is listed in Table 3. The minimum value of R_s is chosen to be 500 Ohms to ensure a maximum power consumption not exceeding 97.6uW for a bandwidth over 1660MHz.

Table- 3 Transistor sizing within the VGA operating under a 1.2V supply voltage.

Transistor	W/L(um/um)
N1-N2	0.5/0.13
P1-P2	2.4/0.13
P3-P6	7.6/0.13
N3-N6	1.2/0.13

By using a Mentor Graphics design architect IC (DA-IC), Fig. 5 shows the layout of class AB VGA. Fig. 6 shows the frequency response at lower gain setting of curves of measured gain response, which was obtained by setting the feedback resistors(R_f) from 15k to 500k. This renders coarse gain tuning of the amplifier, where high gain settings (upper family of curves) and low gain settings (lower family of curves) can be achieved with R_f = 500k, and R_f = 15k, respectively. Within each family of curve, the value of R_s was changed to obtain fine gain tuning. It can be seen that voltage gain control with constant bandwidth can be achieved by varying R_s, while changing R_f affects the bandwidth of the VGA because R_f determines the dominant output pole frequency of the circuit. Therefore to design the VGA, R_f should be chosen first according to the bandwidth requirement and Rs is then tuned to adjust the voltage gain.
A comparisons study of class AB VGA between this work and P. Khumsat et. al is shown in Table 4. From the study, it is shown that the circuit is able to vary the voltage gain in linear dB manner from -26.49 to 39.52 dB. The total power consumption is less than 97.6uW from a single 1.2 V power supply voltage and has a wide and constant bandwidth, which is better than the P. Khumsat et. al. Table 4 also summarizes the experimental performance of the overall class AB VGA. It can see that the proposed class AB VGA can achieved the similar gain range to other reported VGA, while operating under lower supply voltage and smaller size transistor indicating that the proposed VGA is more superior.

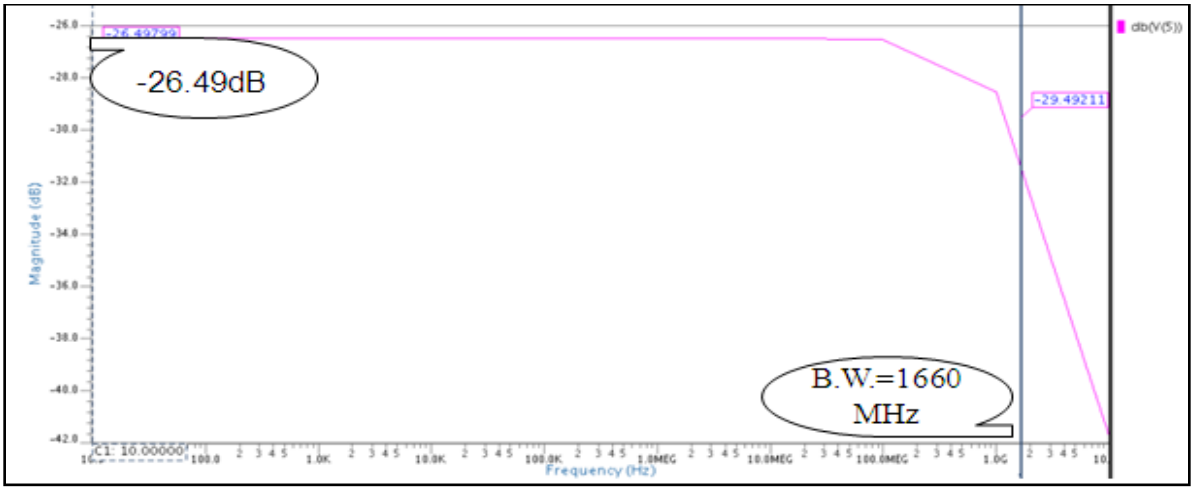

Figure 4:- frequency response at lower gain setting in pre-layout simulation

Table 4: VGA performance comparison

Parameters	**This work**	**Circuit[10]**
technology	GENERIC 0.13um	CEDEC 0.18um

Supply voltage(v)	1.2	1
Gain Range(dB)	-26.49-39.52	-7-26
Gain(dB)	66.01	33
Bandwidth(MHz)	1660	100
Power dissipation(uW)	97.6	125

The modified class AB variable gain amplifier (VGA) circuit layout is designed in GENERIC 0.13-µm CMOS process. In Fig. 5, the completed chip layout of the modified class AB VGA is presented. In this layout the resistor size is larger because it require large area.

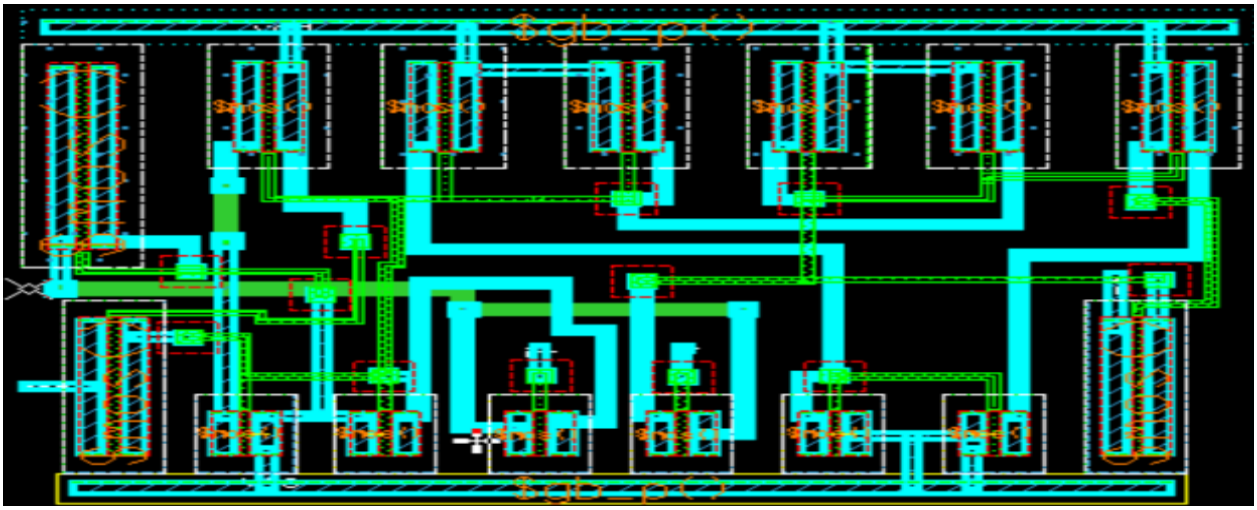

Figure 5: A layout design of class AB variable gain amplifier

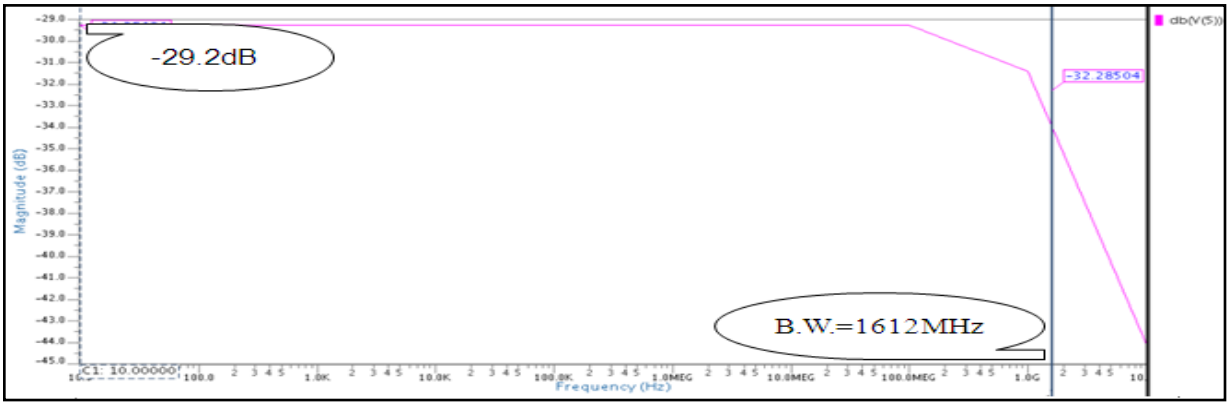

Figure 6:- frequency response at lower gain setting in post-layout simulation

Table 4: pre-layout and post-layout comparison in GENERIC 0.13um

Parameters	**Pre-layout**	**Post-layout**
Supply voltage(v)	1.2	1.2
Gain Range(dB)	-26.49-39.52	-29.2-35.06
Gain(dB)	66.01	64.26
Bandwidth(MHz)	1660	1612

Power dissipation(uW)	97.6	86.5

CONCLUSION

An improved design and a comparative study of class-AB variable gain amplifier using two stage architecture comprising a linear transconductor cascaded by a current amplifier-based feedback transimpedence amplifier is presented in this research. The modified circuit has been designed and analyzed by using the GENERIC 0.13-µm CMOS process. Here, analysis shows that there is small difference in gain and bandwidth in pre-layout and post-layout simulation. In this research, small design parameters were used to reduce the cost and die size of whole chip. According to the research results, it has been proven that, the circuit is capable to achieve high linearity and wide bandwidth. The results also verify that by using current mode technique, the voltage gain of the VGA can be tuned while the bandwidth is higher. Additionally, the circuit size reduced significantly by using small transistors and less number of resistor.

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