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Sophisticated design of low power high speed full adder by using SR-CPL and Transmission Gate logic

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Abstract: *Adder are the basic building blocks of any computing system.. These Arithmetic operations are widely used in most digital computer systems. Addition will be the basic component in arithmetic operation and is the base for arithmetic operations such as multiplication and the basic adder cell can be modified to function as subtractor by adding another xor gate and can be used for division. Therefore, 1-bit Full Adder cell is the most important and basic block of an arithmetic unit of a system. In this paper we analysis the 1-bit full adder using SR-CPL style of full adder design and Transmission gate style of design.*

Keywords: *SR-Cpl, Transmission Gate Full Adder, Leakage, T-Spice*

I. INTRODUCTION

Due to rapid advances in electronic technology, electronics market is becoming more competitive, which results in consumer electronic products requiring even more stringently high quality. The design of consumer electronic products requires not only light weight and slim size, but also low power and fast time-to-market. Therefore, the integrated circuit (IC) designers have to consider more important issues such as chip area, power consumption, operation speed, circuit regularity, and so on. Due to these design issues relevant to the key competitive factors of electronic systems, IC designers and electronic design automation (EDA) vendor are very concerned about the development of effective methodologies to fetch smaller chip area design, lower power consumption, faster operation speed and more regular circuit structure.

The arithmetic circuit is the important core in electronic systems. If the arithmetic circuit has good characteristics, the overall performance of electronic systems will be improved dramatically. Obviously, the performance of the arithmetic circuit directly determines whether the electronic system in market is competitive.

It is well known that full adder is the crucial building block used to design multiplier, microprocessor, digital signal processor (DSP), and other arithmetic related circuits. In addition, the full adder is also dominant in fast adder design. Therefore, to effectively design a full adder with smaller chip area, low power consumption, fast operation speed and regular circuit structure, are the common required for IC designers. Since full adder plays an extremely important role in arithmetic related designs, many IC designers puts a lot of efforts on full adder circuit research. Consequently, there are many different types of full adders have been developed for a variety of different applications. These different types of full adders have different circuit structures and performance. Full adder designs have to make tradeoff among many features including lower power consumption, faster operating speed, reduced transistor count, full-swing output voltage and the output driving capability, depending on their applications to meet the needs of electronic systems. One important kind of full adder designs focus on adopting minimum transistor count to save chip area.

. These full adder designs with fewer transistors to save chip area does have excellent performance, however, due to MOS transistors reduced, these full adders have threshold voltage loss problem and poor output driving capability. Some full adders are designed to emphasize making up for threshold voltage loss to improve circuit performance [6, 7, 8].

These full-swing full adder designs insist on using fewer MOS transistors to reduce circuit complexity to go along with reduced power consumption and delay time. However, the full-swing full adders have no output driver in design leading to signal attenuation problems when they are connected in series to construct multi-bit adders. Therefore, many studies focus on gathering many features such as full-swing voltage, powerful output driving capability and good power delay product [9, 10, 11, 12, 13] in the meantime to boost the performance of full adder circuit design as a whole. However, the penalties have to pay for taking too many design issues into consideration are increased circuit complexity, larger chip area, difficult layout design, and increased transistor count.

Therefore, how to design a full adder circuit with better performance and simpler structure is the main goal of full adder design field. In order to design a full adder with low circuit complexity, good circuit performance and the modularized

structures, a multiplexer-based full adder is proposed in this study. The multiplexer-based full adder has not only regularly modularized structure, but also superior circuit performance.

The rest of this paper is organized as follows: In section 2, some previous works on full adder design are discussed. A novel multiplexer-based full adder design is presented in section 3. In section 4, we show the experimental results and make a discussion. Finally, a brief conclusion is given in section 5.

1.1 Previous Works on Full Adder Design

The full adder function is to sum two binary operands A, B and a carry input C_i, and then generate a sum output (S) and a carry output (C_o). There are two factors affecting the performance of a full adder design: one is the full adder logic architecture, and the other is the circuit design techniques to perform the logic architecture function. Therefore, the full adder design approach requires using different types of logic architecture and circuit design technique to improve the total performance.

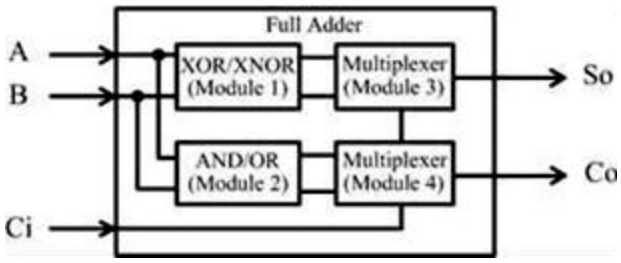

Fig. 1: Full adder logic architecture with four modules.

The traditional full adder logic architecture can be divided into three modules [6, 7, 8], and the logic architecture block diagram is shown in Fig. 1. New-HPSC full adder [9] and Hybrid-CMOS full adder [10] also belong to this category. These two full adders achieve logic functions of three modules by using pass transistor logic (PTL) and static complementary metal-oxide-semiconductor (CMOS) circuit design techniques. Fig. 1 schematically show another logic architecture block diagram of a full adder in which logic architecture is divided into four modules. DPLFA full adder and SR-CPL full adder also belong to this category. DPLFA full adder and SR-CPL full adder achieve logic functions of full adder modules by using double pass transistor logic (DPL) and swing restored complementary pass-transistor logic (SR-CPL) circuit design techniques, respectively.

II. DESIGN CONSIDERATIONS

A. Impact of Logic Style

The logic style used in logic gates basically influences the speed, size, power dissipation, and the wiring complexity of a circuit. The circuit delay is determined by the number of inversion levels, the number of transistors in series, transistor sizes[3] (i.e., channel widths), and intra- and inter-cell wiring capacitances. Circuit size depends on the number of transistors and their sizes and on the wiring complexity. Power dissipation is determined by the switching activity and the node capacitances (made up of gate, diffusion, and wire capacitances), the latter of which in turn is a function of the same parameters that also control circuit size.

Finally, the wiring complexity is determined by the number of connections and their lengths and by whether single-rail or dual-rail logic is used. All these characteristics may vary considerably from one logic style to another and thus make the proper choice of logic style crucial for circuit performance. As far as cell-based design techniques (e.g., standard-cells) and logic synthesis are concerned, ease-of-use and generality of logic gates is of importance as well. Robustness1 with respect to voltage and transistor scaling as well as varying process and working conditions, and compatibility with surrounding circuitries are important aspects influenced by the implemented logic style.

B. Logic Style Requirements for Low Power

According to the formula_

$$P_{dyn} = V_{dd}^2 \cdot f_{clk} \cdot \sum_n \alpha_n \cdot c_n + V_{dd} \cdot \sum_n i_{sc_n}$$

the dynamic power dissipation of a digital CMOS circuit depends on the supply voltage, the clock frequency , the node switching activities the node capacitances the node short circuit currents and the number of nodes _ . A reduction of each of

these parameters results in a reduction of dissipated power [4]. However, clock frequency reduction is only feasible at the architecture level, whereas at the circuit level frequency is usually regarded as constant in order to fulfill some given throughput requirement. All the other parameters are influenced to some degree by the logic style applied. Thus, some general logic style requirements for low-power circuit implementation can be stated at this point.

Switched capacitance reduction: Capacitive load, originating from transistor capacitances (gate and diffusion) and interconnect wiring, is to be minimized. This is achieved by having as few transistors and circuit nodes as possible, and by reducing transistor sizes to a minimum. In particular, the number of (high capacitive) inter-cell connections and their length (influenced by the circuit size) should be kept minimal. Another source for capacitance reduction is found at the layout level [4], which, however, is not discussed in this paper. Transistor downsizing is an effective way to reduce switched capacitance of logic gates on noncritical signal paths [5]. For that purpose, a logic style should be robust against transistor downsizing, i.e., correct functioning of logic gates with minimal or near-minimal transistor sizes must be guaranteed (ratio less logic).

Supply voltage reduction: The supply voltage and the choice of logic style are indirectly related through delay-driven voltage scaling. That is, a logic style providing fast logic gates to speed up critical signal paths allows a reduction of the supply voltage in order to achieve a given throughput. For that purpose, a logic style must be robust against supply voltage reduction, i.e., performance and correct functioning of gates must be guaranteed at low voltages as well. This becomes a severe problem at very low voltage of around 1 V and lower, where noise margins become critical.

Switching activity reduction: Switching activity of a circuit is predominantly controlled at the architectural and register transfer level (RTL). At the circuit level, large differences are primarily observed between static and dynamic logic styles. On the other hand, only minor transition activity variations are observed among different static logic styles and among logic gates of different complexity, also if glitching is concerned.

Short-circuit current reduction: Short-circuit currents (also called dynamic leakage currents or overlap currents)may vary by a considerable amount between different logic styles. They also strongly depend on input signal slopes (i.e., steep and balanced signal slopes are better)[7] and thus on transistor sizing. Their contribution to the overall power consumption is rather limited but still not negligible (10–30%), except for very low voltages where the short-circuit currents disappear. A low-power logic style should have minimal short-circuit currents and, of course, no static currents besides the inherent CMOS leakage currents.

C. Logic Style Requirements for Ease-of-Use

For ease-of-use and generality of gates, a logic style should be highly robust and have friendly electrical characteristics, that is, decoupling of gate inputs and outputs (i.e., at least one inverter stage per gate) as well as good driving capabilities and full signal swings at the gate outputs, so that logic gates can be cascaded arbitrarily and work reliably in any circuit configuration. These properties are prerequisites for cell-based design and logic synthesis, and they also allow for efficient gate modeling and gate-level simulation. Furthermore, a logic style should allow the efficient implementation of arbitrary logic functions and provide some regularity with respect to circuit and layout realization. Both low-power and high-speed versions of logic cells (e.g., by way of transistor sizing) should be supported in order to allow flexible power-delay tuning by the designer or the synthesis tool.

D. Static Versus Dynamic Logic Styles

A major distinction, also with respect to power dissipation, must be made between static and dynamic logic styles. As opposed to static gates, dynamic gates are clocked and work in two phases, a pre charge and an evaluation phase. The logic function is realized in a single NMOS pull-down or PMOS pull-up network, resulting in small input capacitances and fast evaluation times. This makes dynamic logic attractive for high-speed applications. However, the large clock loads and the high signal transition activities due to the pre charging mechanism result in excessive high power dissipation. Also, the usage of dynamic gates is not as straightforward and universal as it is for static gates, and robustness is considerably degraded. With the exception of some very special circuit applications, dynamic logic is no viable candidate for low-power circuit design

III. DESIGN TECHNOLOGIES

There are many sorts of techniques that intend to solve the problems mentioned above

Full Adder Design:

So = H′Ci + HC′o (1)

Co = HCi + H′A (2)

where H = A Xor B and H′ = A Xnor B. An Full Adder is made up of an XOR–XNOR module, a sum module and a carry module.

The XOR–XNOR module performs XOR and XNOR logic operations on inputs A and B, and then generates the outputs H and
H′. Subsequently, H and H′ both are applied to the sum and the carry modules for generation of sum output So and carry output Co

1) SR-CPL Full Adder Design:

A SR-CPL is designed using a combination
of pass transistor logic (PTL) and static CMOS design techniques to provide high energy efficiency and improve driving capability. An energy efficient CMOS FA is implemented using swing restored complementary pass-transistor logic (SR-CPL) and PTL techniques to optimize its PDP

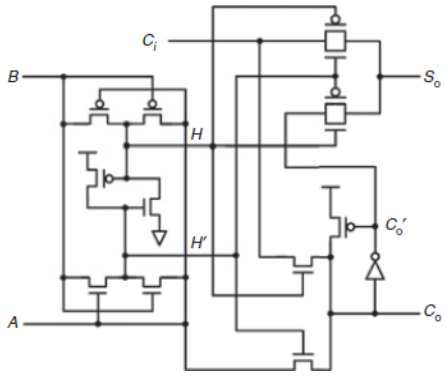

Fig 4 :SR-CPL Full Adder Design

2) Transmission gate CMOS (TG) uses transmission gate logic to realize complex logic functions using a small number of complementary transistors. It solves the problem of low logic level swing by using pMOS as well as nMOS

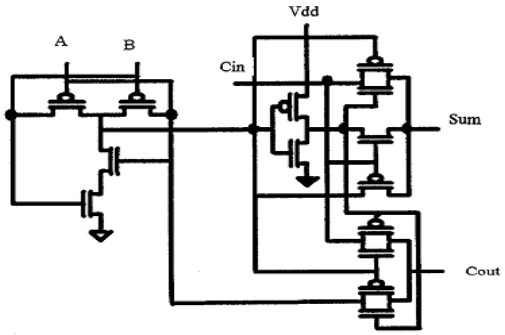

Fig1: Transmission Gate Full Adder

IV. SIMULATION ANALYSIS

Full Adder was designed with different logic using Tanner Tools and simulated

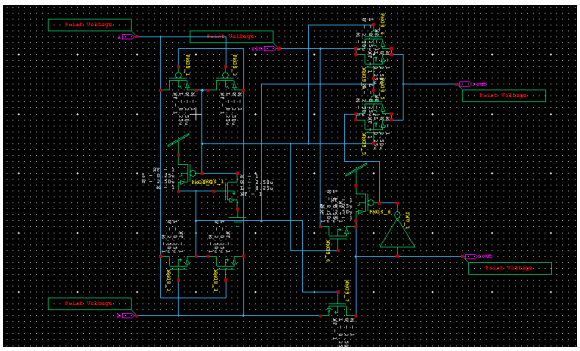

Fig11: SR-CPL full Adder Design

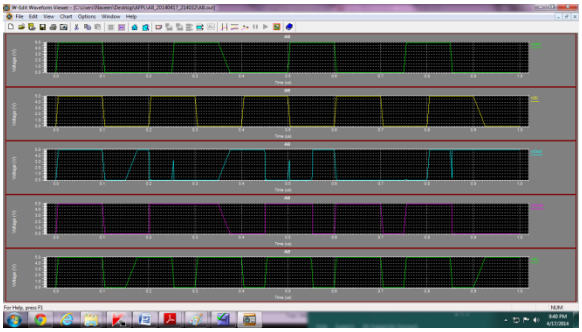

Fig12: SR-CPL full Adder simulation

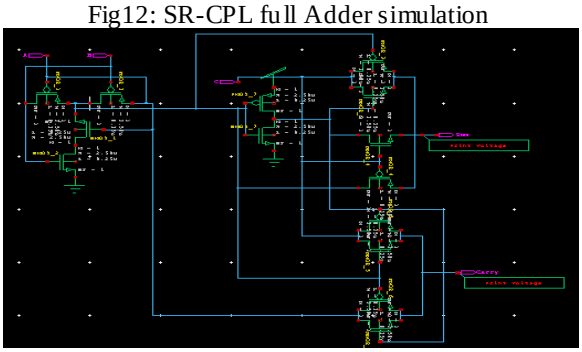

Fig5: Transmission Gate Full Adder Design

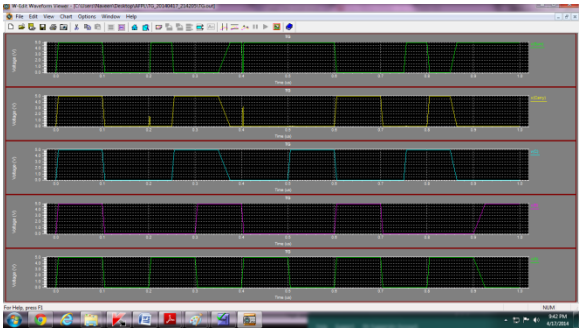

Fig6: Transmission Gate Full Adder simulation

Tabulation:

Circuit	Power Dissipation
SR-CPL	7.045079e-005 watts
Transmission Gate	3.099718e-005 watts

The above circuits of full adder are simulated using Tanner Tools using TSMC018 and its delay and power of individual circuits are tabulated

V. CONCLUSION

In this paper we show the low power adder design full adder with less number transistors. CMOS design styles make the full adder to design in less no of transistors as wells as with lower power dissipation. For performance validation, Tanner simulations were conducted on FAs implemented with TSMC 018 CMOS process technology in aspects of power consumption, delay time In contrast to other types of FAs with drivability, an SR-CPL-FA is superior to the other ones and can be applied to design related adder-based portable electronic products in practical applications in today's competitive markets.

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