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A Review on Efficient FFT/IFFT algorithm for OFDM systems using FPGA

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Abstract — *Orthogonal Frequency Division Multiplexing (OFDM) is a multi-carrier modulation technique which divides the available spectrum into many carriers. However, recently the attention toward OFDM has grown dramatically in the field of wireless and wired communication systems. FFT and IFFT are the important modules for OFDM design. This paper concentrates on finding methods for Fast Fourier Transform (FFT) and Inverse Fast Fourier Transform (IFFT), in an efficient way. Field Programmable Gate Array (FPGA) is also emerging as a fundamental paradigm in the implementation of these standards. This is due to their increased capabilities (speed and resources).*

Keywords- *OFDM, FFT, IFFT, FPGA*

I. INTRODUCTION

Orthogonal Frequency Division Multiplexing (OFDM) could be tracked to 1950's, but it had become very popular at these days, allowing high speeds at wireless communications. OFDM could be considered either a modulation or multiplexing technique, and its hierarchy corresponds to the physical and medium access layer. [5]The fast Fourier transform (FFT) is one of the most popular algorithms in digital signal processing and it is used in communications, radar and reconnaissance applications. Field programmable gate arrays (FPGAs) have long been attractive for accelerating FFT processing speed.[1]A basic OFDM system consists of a QAM or PSK modulator/demodulator, a serial to parallel / parallel to serial converter, and an IFFT/FFT module. The iterative nature of the FFT and its computational order makes OFDM ideal for a dedicated architecture outside or parallel to the main processor. [5]

II. REVIEW OF EXISTING FFT/IFFT ALGORITHMS FOR OFDM SYSTEMS

Discussion: Research paper titled Special-purpose computer for 64-point FFT based on FPGA, IEEE Wireless Communications & Signal International Conference on Nanjing China,Nov-2010, describes a high speed 64-point FFT processor based on FPGA using a hybrid-parallel and pipeline architecture. The study has been particular used to decimation-in- frequency (DIF) FFTs of length 64 points and a 8-bit word size has been considered. The whole processor has been implemented using two parallel 8- point FFT and 8 complex multipliers between them. 'Twiddle factor' addresses can be easily generated with counters. The address generation logic is very simple and does not limit the throughput of the system. To improve the system operation speed, a hybrid parallel FFT algorithm is used in this processor. Internal structure of hybrid parallel FFT Firstly, a DEMUX operation is used to de-series the input data into 8 parallel channels. Secondly, a global pipeline 8-point FFT is employed to these parallel data. Thirdly, the outputs of global pipeline FFT are multiplied with 8 complex coefficients from FPGA internal ROM. Lastly, another global pipeline 8- point FFT processor is employed to the outputs of the 8 complex multiplies. Afterwards, a MUX operation issued to make a serial output from FPGA.[1]

Research Paper tilted An Efficient 64-point Pipelined FFT Engine by Prof. J. M. Rudagi, Richard Lobo, Pradeep Patil, Nikit Biraj, Naimahmed Nesaragi IEEE 2012 International Conference on Advances in Recent Technologies in Communication and Computing explains In This Paper Describes the Fast Fourier Transform (FFT) is a very important algorithm in signal processing, software defined radio and the most promising modulation technique i.e. Orthogonal Frequency Division Multiplexing (OFDM). This paper describes the design and implementation of a fully pipelined 64-point FFT engine in programmable logic. The FFT takes 16-bit fixed point complex numbers as input and after a known pipelined latency of 20 clock cycles produces the desired output. The input data samples are fed in parallel to the FFT engine to generate outputs in parallel. The architecture requires 25% multiplication operations compared to conventional Cooley-Tukey approach. Hence it leads to low power and area saving. [2]

Research paper titled Design and Implementation of Inverse Fast Fourier Transform for OFDM by R.Durga Bhavani, D.Sudhakar. International Journal of Science and Engineering Applications Volume 2 Issue 7, 2013 explains, OFDM is the most promising modulation technique for most of the wireless and wired communication standards. The basic idea of OFDM is to divide the available spectrum into several sub channels, making all sub channels narrowband which experiences flat fading. OFDM uses the spectrum efficiently due to its orthogonally and prevents interference between the closely spaced carriers. OFDM provides high bandwidth efficiency because the carriers are orthogonal to each other's

and multiple carriers share the data among themselves. The main advantage of this transmission technique is their robustness to channel fading in wireless communication environment. The main focus of this paper is to design IFFT and FFT blocks which are used in transmitter and receiver blocks of OFDM system. The methodology used is the 8-point IFFT/FFT (DIF) with radix-2. The design unit also consists of spreader and despreader for mapping technique. The implementation is done in FPGA by using Verilog HDL. The timing simulation and synthesized results are performed and the design is analyzed by using Xilinx ISE tools. [3]

By doing design and observing the performance analysis of the 32 FFT and 64 point FFT, using Radix-2, Radix-8 and Split Radix algorithm. The algorithm is developed by Decimation-In-Time (DIT) of the Fast Fourier Transform (FFT), using VHDL as a design entity and synthesis are performed in Xilinx ISE Design Suite 13.2 version [4] Using synthesis results performance analysis is done between 32 and 64 point Fast Fourier Transform (FFT) in terms of speed and computational complexity. Compare the Devices utilization summary report 32-point and 64-point as shown Table 2.1.3 [4]

Logic Utilization	Used 32-Point FFT	Used -64 Point FFT
No. of Slice LUTs	18253	22120
No. of Fully Used LUTFFT Pairs	0	0
No. of Bonded IOBs	2560	2560
No. of DSP48EIs	148	160

The Fast Fourier Transform (FFT) is one of the rudimentary operations in field of digital signal and image processing. Some of the very vital applications of the Fast Fourier transform include Signal analysis, Sound filtering, Data compression, Partial differential equations, Multiplication of large integers, Image filtering etc. Fast Fourier transform (FFT) is an efficient implementation of the discrete Fourier transform (DFT). This paper concentrates on the development of the Fast Fourier Transform (FFT), based on Decimation-In- Time
(DIT) domain, Radix-2 algorithm, this paper uses VHDL as a design entity, and their Synthesis by Xilinx Synthesis Tool on Vertex kit has been done. The input of Fast Fourier transform has been given by a PS2 KEYBOARD using a test bench and output has been displayed using the waveforms on the Xilinx Design Suite 12.1.Thesynthesis result As shown Table III that the computation for calculating the 32-point Fast Fourier transform is efficient in terms of Area. [6]

III. CONCLUSION

By doing literature survey we can conclude that FFT/IFFT algorithm is required large number of multiplication and addition. The order of arithmetic operations for FFT is (NlogN) that is NlogN additions and (N/2)logN multiplications. In arithmetic operation large number of resource are required. But one limitation in FPGA is the limited number of resources. So reduce the number of arithmetic operation and more efficient way to implement FFT/IFFT algorithm for OFDM system on FPGA..

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