High Speed CMOS Charge Pump Circuit for PLL Applications Using 180nm CMOS Technology

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Abstract- The performance of charge pumps depends heavily on the ability to efficiently generate high voltages on-chip while meeting stringent power and area requirements. The paper presents a High Speed CMOS charge pump circuit for PLL applications using 180nm CMOS technology. The proposed circuit has simple symmetric structure and provides more stable operation while reducing spurious jump phenomenon. The output voltage of presented design can be increased up to 1000mV. The functionality of charge pump has been tested at operating based frequency of 1000 MHz.

Keywords- Low Power, Low Voltage, Phase Locked Loop (PLL), Charge pump, High Speed Network.

INTRODUCTION

Wireless telecommunication has typical element known as Phase locked loop (PLL) are mostly used in computers, radio, telecommunications and other electronic applications. PLL has elements such as WLANs, mobile communications and satellite. In the 1930s, phase concept was invented and swiftly found wide usage in electronics & communication. While the basic phase-locked loop has remained nearly the same since then, its implementation in different technologies and for different applications continue to challenge designers.

PLL is simple feedback system that compares the output phase with the input phase and produces the output frequency which is proportional to the input phase difference.

Now days low-cost and small size circuits are increasing in demand; So RF designers face this problem. They are doing more effort in low-cost CMOS technologies for achieving higher levels of integration of RF transceivers. To enable single-chip fully integrated solutions, PLL synthesizers are important building blocks, alongside the digital signal processors. Worlds of advanced IC technology, PLLs are available cheaper monolithic ICs.

THEORY OF PLL

After the invention of PLL in1932, the basic phase locked loop has remained nearly the same but its implementation in different technologies is still a challenge for technicians.

PLL consist five main blocks

1) Phase Frequency Detector (PFD)
2) Charge Pump (CP)
3) Low Pass Filter
4) Voltage Controlled Oscillator (VCO)
5) Divided by N Counter.

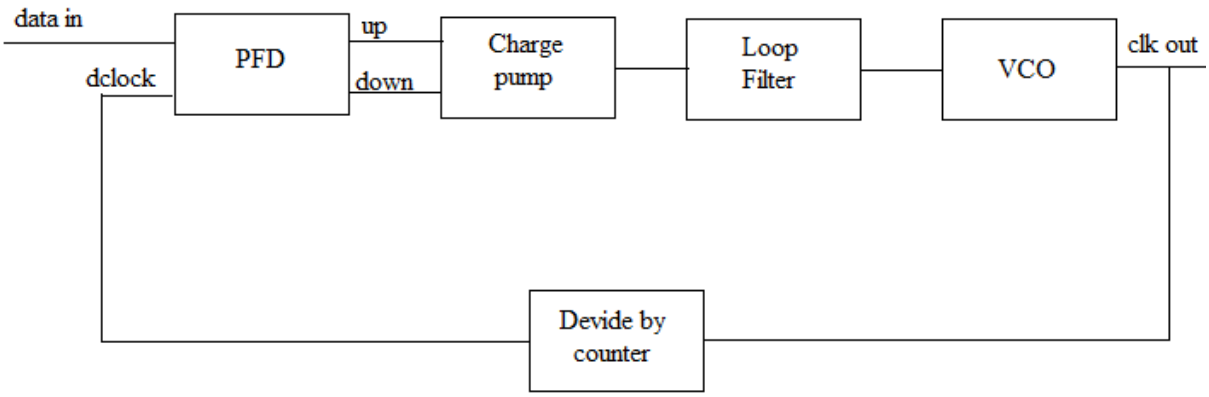

Fig. 1 A Basic Block Diagram of Phase Locked Loop

CHARGE PUMP

Charge pump is the next block to the phase frequency detector. The output signals - UP signal and DWN signal generated by the PFD is directly connected to the charge pump.

The main purpose of a charge pump is to convert the logic states of the phase frequency detector into analog signals suitable to control the voltage-controlled oscillator (VCO). Basically, the charge pump consists of current sources and switches. The output of the charge pump is connected to a low pass filter that integrates the charge pump output current to an equivalent VCO control voltage (Vcntl).

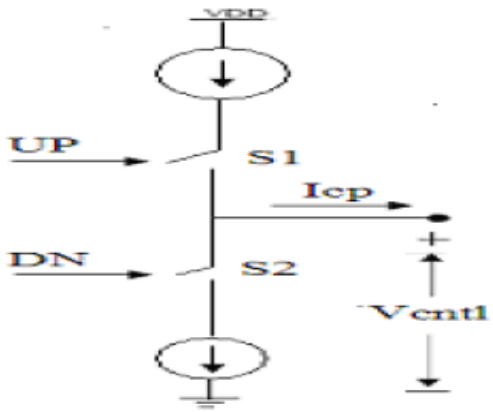

Fig. 2: Basic Block Diagram of Charge Pump

Three states in the charge pump correspond to its output to the loop filter:

State 1: Charging current: +ICP
State 2: Discharging current: -ICP
State 3: Zero current

As mentioned earlier, the PFD needs to produce a certain amount of pulse width of the UP and DN signal in the beginning of the period. In this condition, ideal charge pump will give zero current which is state 3 since the charging current is equal to the discharging current.

When the VCO output frequency is leading the reference frequency, the PFD will activate the DOWN signal and deactivate the UP signal. Hence, switch S1 will be opened and switch S2 will be closed. This time, current ICP will flow out from the filter and reduce the Vcntl. Consequently, the VCO output frequency is decreases.

The lock condition of the PLL is established when the VCO output frequency is the same as the reference frequency.

During this period, the PFD will deactivate both up and down signals. Hence switches S1 and S2 will be opened until the VCO output frequency changes. Since switches are open, there is no current path formation, hence no current will flow into or out from the filter.

UP Signal	DOWN Signal	Condition	Note
1	0	Charging	Current flows into filter
0	1	Discharging	Current flows out from filter
0	0	Vout constant	Current zero
1	1	Vout constant	Current zero

Table 1: Operation of Ideal Charge Pump

PROPOSED CHARGE PUMP STRUCTURE

There are number of charge pump circuits were designed to reduce jump phenomenon from time to time. The proposed circuit, as shown in Fig.3, is a new way to achieve this purpose and increases the output voltage range.

The Proposed charge pump circuit consists of pull-up & pull-down network. The charge pump circuit works as follows,

When the signal UP =1 (high logical level), P1 is 'OFF' and the current source I1 drives P3. Since the power supply is 1V, when P3 is 'ON', the voltage headroom between gate and source of P2 is not enough to open it. Obviously, P5 is 'ON' and so P3 and P5 compose a current mirror. Capacitor Cp will be charged by the current source I1, raising the voltage Vc. In other hand DN =0 (Low logical level), pull-down network is OFF.

When the signal UP =0 (low logical level), P1 and P2 are both 'ON'. Since IP1=IP2+I1, The current in P3 and P5 are so small that they are negligible. Then, the voltage Vc at the capacitor should, ideally, remain stable. P4 and N1 are used to predischarge to the gate of P5 (pre-discharge at the gate of N6). If they are cancelled in this charge pump circuit, when the UP signal is switched from 0 to 1, the charging time of P3 is relatively long, which results in delaying open speed of P5. So to overcome this problem, P4 and N1 are taken advantage at the gate of P5. Then, the voltage at the gate of P5 is rapidly pulled down once the UP signal switches from 0 to 1 opening P5 in a much shorter time. In other hand DN =1 (High logical level), pull-down network is 'ON' and capacitor Cp will be discharged.

When they are both ON, they operate in the saturation region. So, to carry the same currents, P4 and N1 have to be perfectly matched (IP4=I N1). M meanwhile, in order to minimize the introduction of the parasitic capacitance, the width and length values of P4, N1 must be as small as possible.

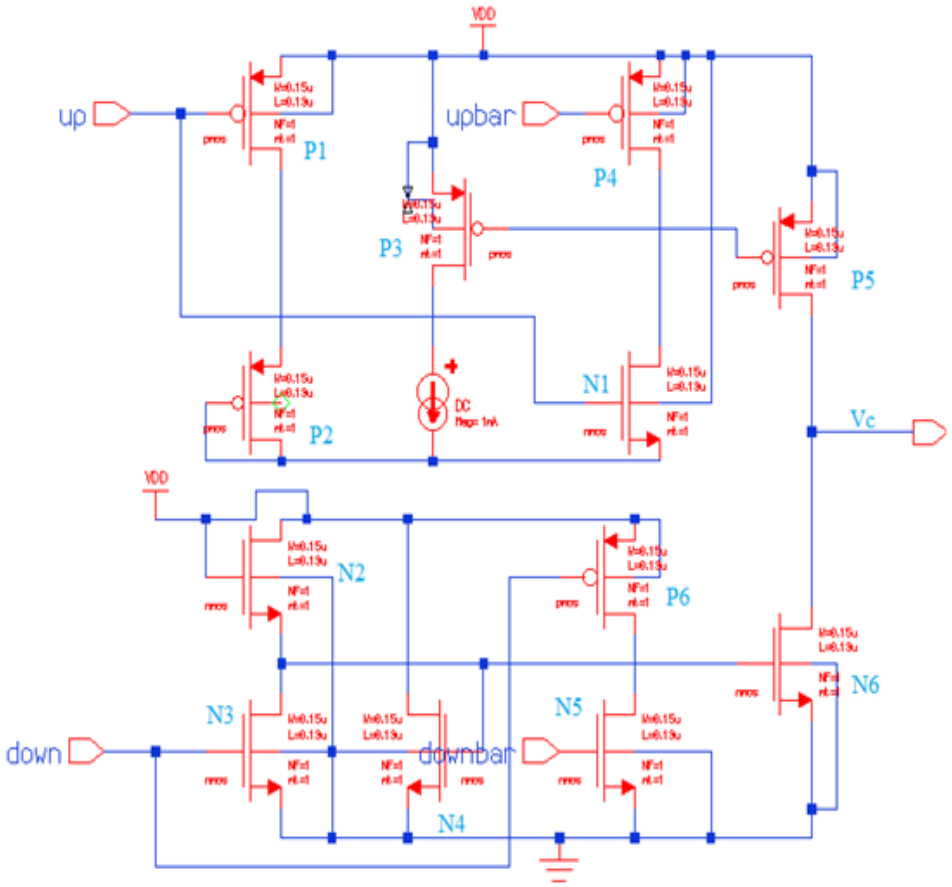

Fig. 3: Improved Charge Pump

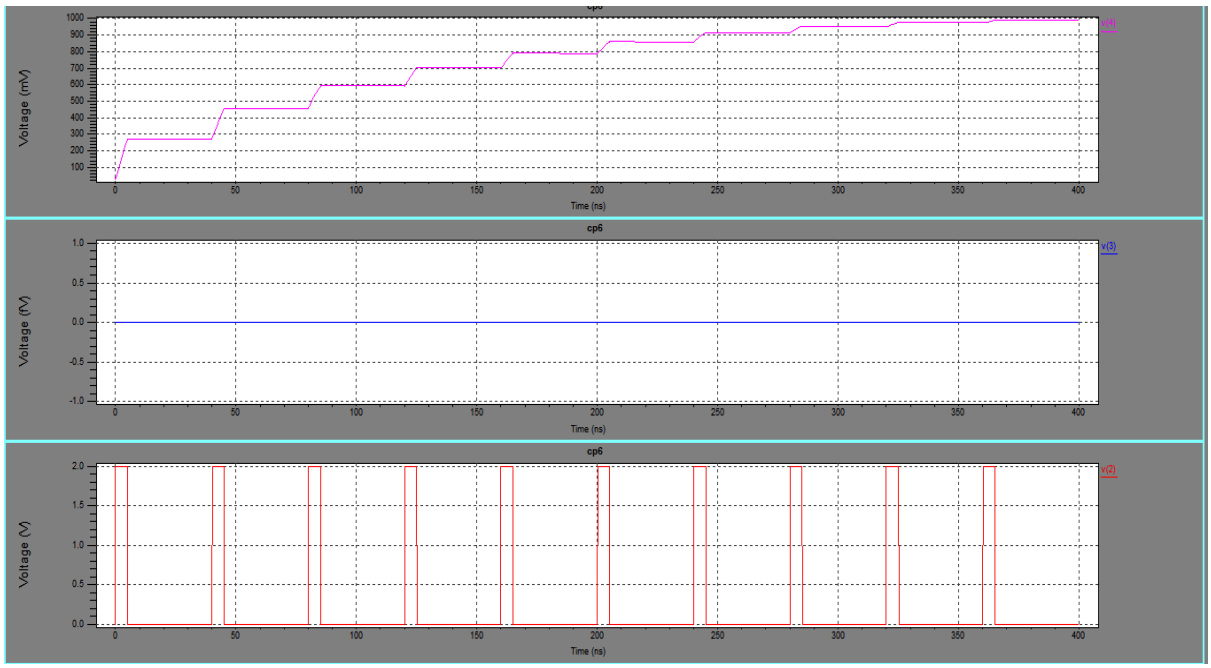

Fig. 4: Charging Waveform of the Charge Pump

Parameters	Improved Results
Power supply	1 V
Operating Frequency	1000 MHz
Output voltage range	840mv to 880mv
Technology	180nm

Table 2: Performance Summary

SIMULATIONS RESULTS

The new charge pump circuit is designed in 90nm CMOS process, simulated using T-Spice under a 1V power supply. The pull up current I1 and the pull down current I2 are both set to 100µA. The operating frequency is 1000MHz and Fig. 4 shows the charging result of the new charge pump circuit. The output voltage range is from 840mV up to 880mV.

A summary of the circuit characteristics is presented in Table 2.

CONCLUSION

In this paper, a high speed CMOS charge pump for PLL application has been designed and simulated using the 90nm CMOS technology. The simple and symmetric structure of the circuit reduces jitter phenomenon and provide more stable operation under a 1 V power supply without use of op-amp circuit. It has output voltage range from 840mV up to 880mV and more stable step voltage. Simulations were done using T-Spice. The operating frequency is 1000MHz.

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