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Area and Power Efficient Layout Design of Inverter

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Abstract- *In recent years, the demand for low power devices has grown significantly. This growth is mainly due to the fast growth of battery-operated semiconductor devices such as cell phone, tablets, laptop etc. Reducing power consumption and surface area in integrated circuit is an important factor for both portable and desktop applications. In this paper an inverter and its layout have been designed using PMOS and NMOS transistors. The result has been compared in terms of power consumption and surface area. The simulated results show that semi-custom layout of an inverter consumes 52.5% more power and 35.9% more surface area than the full custom layout of inverter.*

Key Words- *CMOS inverter; Dynamic Power; NMOS; PMOS; Static Power; VLSI*

I. INTRODUCTION

CMOS is the most popular technology for the fabrication and implementation of digital systems. CMOS is the most dominant among all the IC technologies available for the designing of digital circuits. In the earlier period, VLSI designers were more bent toward the performance and areas of digital circuits [1]. Cost and Reliability also gained core importance whereas power consumption was secondary consideration for them. In recent years the power is an important parameter in comparison to surface area and speed [2]. Power consumption is one of the basic constraints in any integrated circuit. There is always a trade-off between power and performance of any circuit [3]. Power consumption of CMOS consists of dynamic and static components [4]. Static power dissipation happens due to the leakage current. The leakage current occur due to the off transistor because some minutely current flow in off transistor whether it is PMOS or NMOS [5]. Dynamic and leakage power contributes the total power consumption. Traditionally static power consumption was overshadowed by dynamic power consumption, but the transistor size was continued to shrink. Dynamic power dissipation is proportional to square of the supply voltage. In deep submicron process supply voltages and threshold voltages for CMOS transistors have greatly reduced. This reduces the dynamic power dissipation [6]. The dynamic power cannot be completely eliminated; however, they can be reduced by circuit design technique.

II. INVERTER

VLSI circuit is used for increasing number of portable application with limited amount of power available [7]. Inverter is a basic circuit to design any kind of digital circuits. It is a circuit which performs the complement or invert operation of the given input. Inverting operation can be described by table 1.

TABLE 1. INVERTER OPERATION

Input	*Output*	*LED*
0 (Switch OFF)	*1*	*Glow*
1 (Switch ONN)	*0*	*Not Glow*

The most conventional CMOS inverter design is a combination of PMOS and a NMOS. CMOS inverter is the combination of pull-up network and pull- down-network. In pull-up network, PMOS and in pull down network NMOS is used. A low power design is essential to achieve long battery life in battery operated devices. The size of the transistor is reduced with technology scaling, thereby increasing the integration density and the operating speed of the circuits [8]. In this paper low area and efficient power inverter has been designed using 90 nanometer technology. Figure 1 shows CMOS inverter.

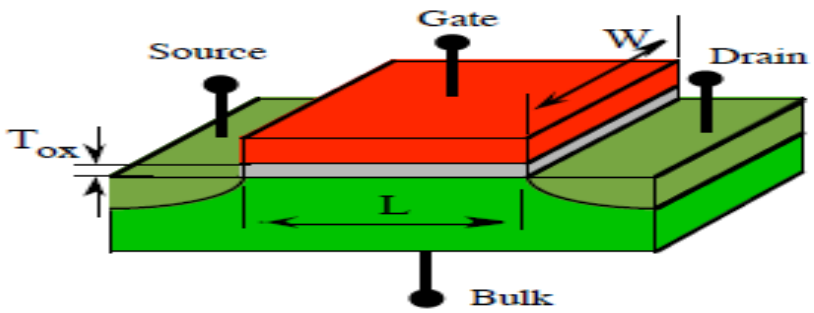

Figure1: CMOS inverter [9]

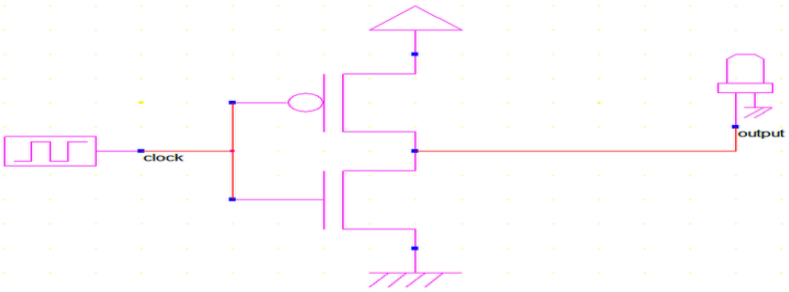

Figure2: Schematic diagram of CMOS inverter using DSCH

III. LAYOUT DESIGN

The scaling of CMOS technology in 90 nanometer technology reduces supply voltage and threshold voltage. Figure 3 shows the semi-custom layout of an inverter using PMOS and NMOS transistors. Generally all parameters of CMOS depend on W/L ratio. This technique uses aspect ratio W/L=5 for PMOS and NMOS transistor. The layout design rule describes how the small feature can be and how closely they can be packed in a particular manufacturing process. Different logical layers are used by the designer to generate the layout of the circuit. There are specific layers for metal, contacts and diffusion areas and polysilicon. DSCH and Microwind 3.1 tools are used for the designing of an inverter and λ based design rules have been implemented. In λ based rule the metal and diffusion have a minimum width of 4 λ.

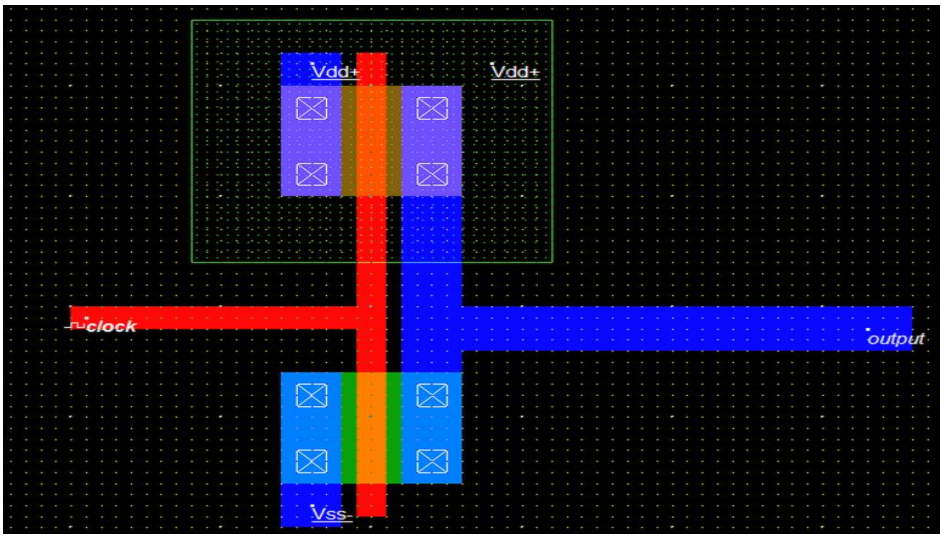

Figure 3: Semi-custom layout of inverter

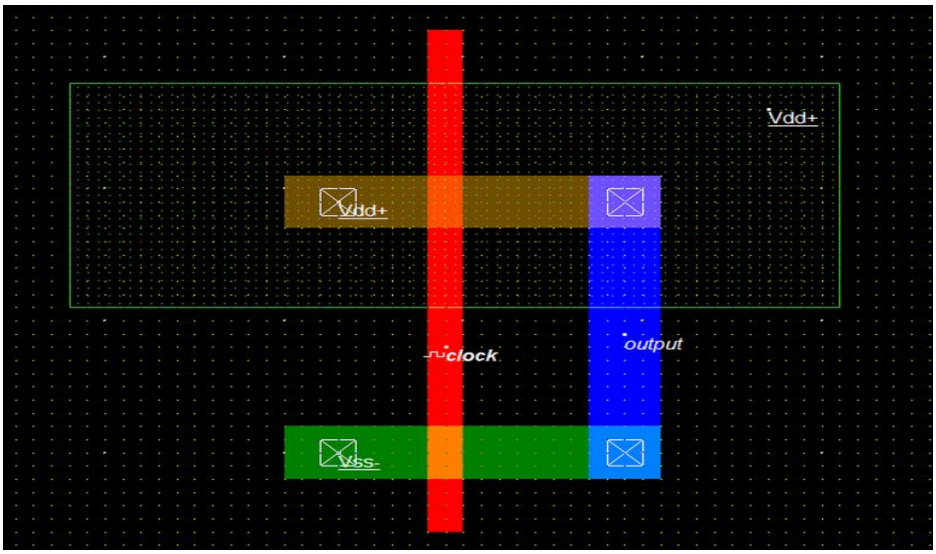

Figure 4: Full-custom layout of inverter

Polysilicon uses a width of 2 λ. Contacts are 2 λ each in length and height. Polysilicon overlaps diffusion by 2 λ where transistor is required and has a spaced of 1 λ. Polysilicon and contacts have spacing of 3 λ from other polysilicon and contacts. N-well surrounded PMOS transistor by 6 λ and avoids NMOS transistor by 6 λ.

Figure 4 shows the full custom layout of an inverter using PMOS and NMOS transistor. W/L ratio being the same as semi- custom layout. In semi-custom layout 8 metal contacts are used while in full custom only 4 metal contacts are used. Hence area is reduced and less power is consume. In full custom layout less polysilicon and metals are used.

IV. SIMULATED RESULT

TABLE 2. PARAMETERS OF CLOCK USED IN SIMULATION

Parameters	*Value*
Level 1 (V)	*1.20 V*
Level 0 (V)	*0.00 V*
Time low (tl)	*0.390 ns*
Rise time (tr)	*0.010 ns*
Time high (th)	*0.390 ns*
Fall time (tf)	*0.010 ns*

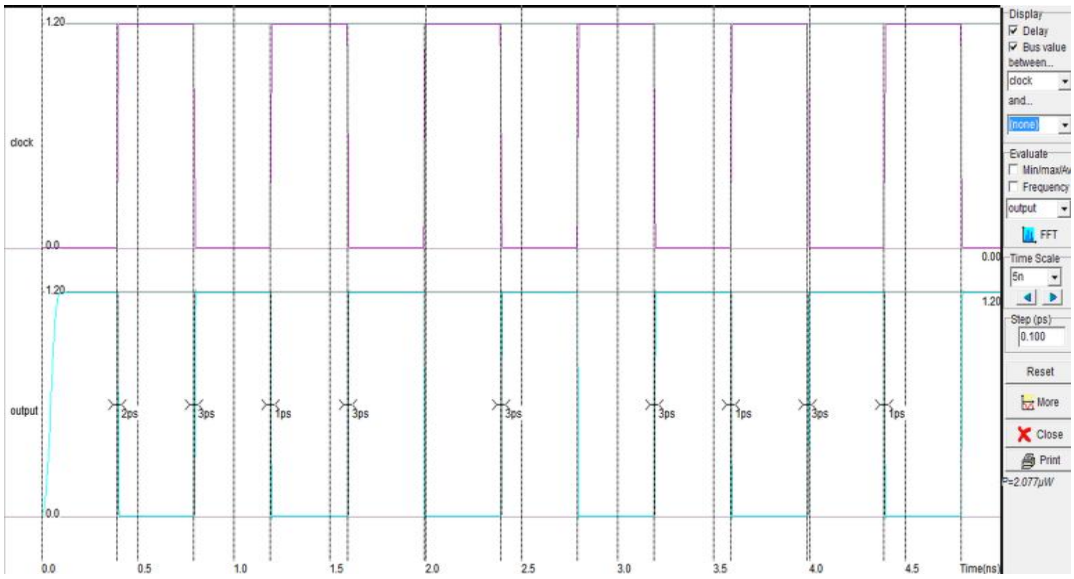

Figure 5: Voltage versus time (semi custom)

Figure 5 and figure 6 show the voltage versus time (Timing diagram) of semi-custom layout and full custom layout. The time scale is 5n and step (PS) is 0.100. Upper half part of figure 5 and figure 6 is clock and lower part is the output of inverter. Figure 7 is the voltage versus voltage (Hysteresis) output of an inverter.

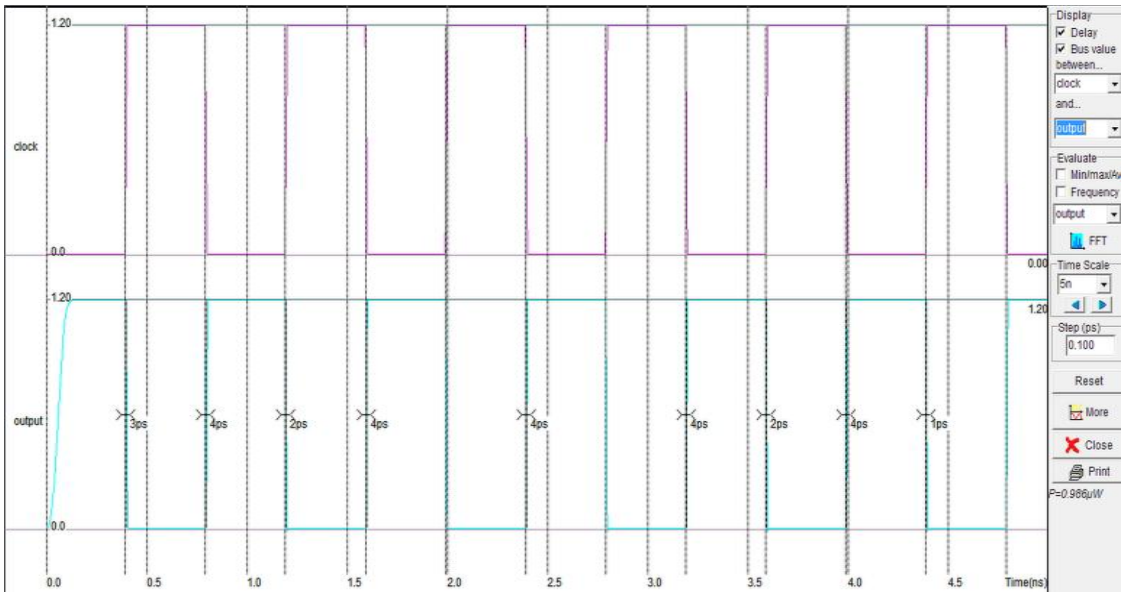

Figure 6: Voltage versus time (full custom)

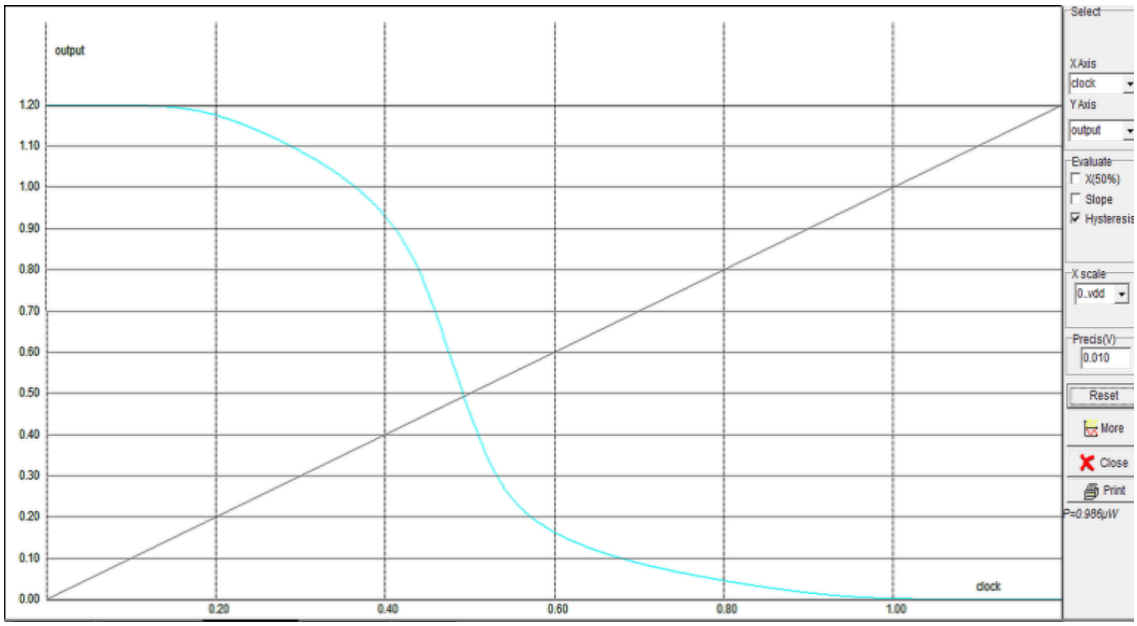

Figure 7: Voltage versus voltage (Full Custom)

TABLE 3. COMPARISON OF DIFFERENT LAYOUT

Parameter	*Semi-custom layout*	*Full custom layout*
Power	*2.077 µw*	*0.986 µw*
Surface Area	*6.4 µm^2*	*4.1 µm^2*

Table 3; indicate the comparison of power and surface area of different layout of an inverter.

V. CONCLUSION

In this paper an inverter and its layout have been designed using PMOS and NMOS transistors and 90nm technology with DC level 1.2 V have been used. Simulated results have compared in terms of power consumption and surface area of semi- custom layout and full custom layout using DSCH and Microwind tool. The simulated results show that semi-custom layout covers 6.4 µm^2 and full custom layout covers 4.1 µm^2 surface areas. The simulated results also show that semi-custom layout consumes 2.077 µw and full custom layout consumes 0.986 µw power. The full custom structure has added advantages of reduced surface area and power.

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