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Design and Implementation of high-speed adders for various digital applications

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Abstract - *In this rampant age of technology, every new invention and discovery bring some revolutionary changes along with them. From the era when 3rd generation computers stepped in, then Illiac IV supercomputers and now the 7th generation have already hit the market. The basis of all these technologies and the faster processors is the key ingredient – Adders. Adders are one of the most universally accepted components in any digital integrated circuit design. In digital adders, the speed of addition is defined by the time required to propagate carry through the adders.With the advances in technology, researchers are busy designing adders which offer either high speed, low power consumption or the combination of both. In this paper, our holistic aim is to optimise the speed of the adders with the minimum time complexity and the minimum power utilisation. The design of various adders such as Carry Look Ahead Adder(CLA), Ripple Carry Adder (RCA), Carry Save Adder (CSA), Carry Select Adder(CSL), Carry Skip Adder(CSK), Koggy Stone Adder are discussed and have been compared according to the delay generation and power consumption. Mentioned adders have been designed using Verilog HDL and then simulated and synthesised using Xilinx Vivado v.16 for power consumption and delay. In this paper 6 different adders as mentioned above has been implemented and compared in terms of speed and power. It has been found that 64 bit Koggy Stone Adder is having minimum delay and minimum power. (Abstract)*

Keywords- *Carry Look Ahead Adder(CLA), Ripple Carry Adder (RCA), Carry Save Adder (CSA), Carry Select Adder(CSL), Carry Skip Adder(CSK), Koggy Stone Adder, Verilog HDL, Xilinx Vivado*

I. INTRODUCTION

The Datapath is the hardware that performs all the required operations, for example, ALU, registers, and internal buses. The central unit of every microprocessor and a digital signal processor is its data path. The core of data-path and addressing units are basically the arithmetic units which include adders as one of the most common blocks. People are working to find the efficient solution to the binary addition problem which is well suited for VLSI implementations. As adders are the basic components for many such electronic complex systems. They are the building blocks of multipliers, comparators, dividers, arithmetic functions, shifters etc. In short, adders have become a critical hardware for the efficient implementation of arithmetic unit. Reduction of computational time increases the speed of electronic devices. So, in high-speed circuits, it is essential to carry out these operations in minimum possible time. Addition is simply the summing of two number and generating their sum and carry[1]. All complex adder architecture are designed from major building blocks like half adder (HA) or full adder (FA) . In this paper, an attempt is been made to implement high-speed adders like Carry Save Adder (CSA), Carry Skip Adder (CSK), Carry look Ahead Adder (CLA), Carry Select Adder (CSL), Ripple Carry Adder (RCA) and Koggy Stone Adder and comparing the best one which can be further used for digital applications like multipliers. Our holistic aim will be to optimize the speed of the adders with minimum time complexity. Then the performance of various adders will be calculates and compared.

II. ADDERS

The design of various adders such as Ripple Carry Adder, Carry Look Ahead Adder, Carry Save Adder, Carry Select Adder, Carry Skip Adder, Koggy Stone Adder have been briefly discussed below.

2.1 Ripple Carry Adder

The basic operation of ripple carry adder as shown in the scheme below, is the addition of two numbers having bits that can be extended indefinitely. The basic component of ripple carry adder is the full adders. The full adder adds two bits along with the carry bit and generates a sum and a carry[1]. Carry generated propagates to the next full adder in series and so on. Therefore, we can say that delay in a ripple carry adder increases as a number of bits increases.

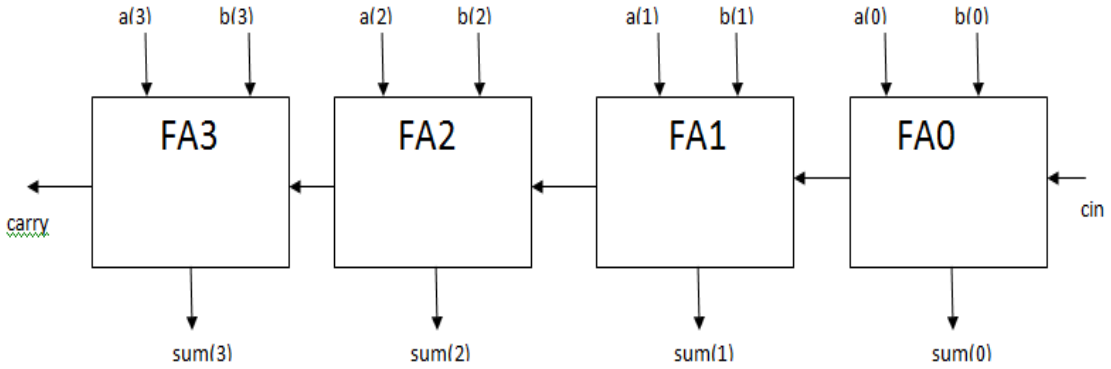

Fig.-1 Ripple Carry Adder

2.2 Carry Look Ahead Adder

Carry look Ahead Adder design is based on the principle of looking at lower adder bits of argument and added if higher order carry generated as shown in the fig.2. Carry Look Ahead Adder minimises the propagation delay by generating the carries of each stage in parallel. The delay time of CLA architecture exhibits logarithmic on the size of the adder, which allows the propagation delay of the carry signal to be minimised.[3] The expressions for Gi and Pi with two input inary operands Ai and Bi as follows:

$$Gi = Ai.Bi \quad \text{(i)}$$

$$Pi = Ai \oplus Bi \quad \text{(ii)}$$

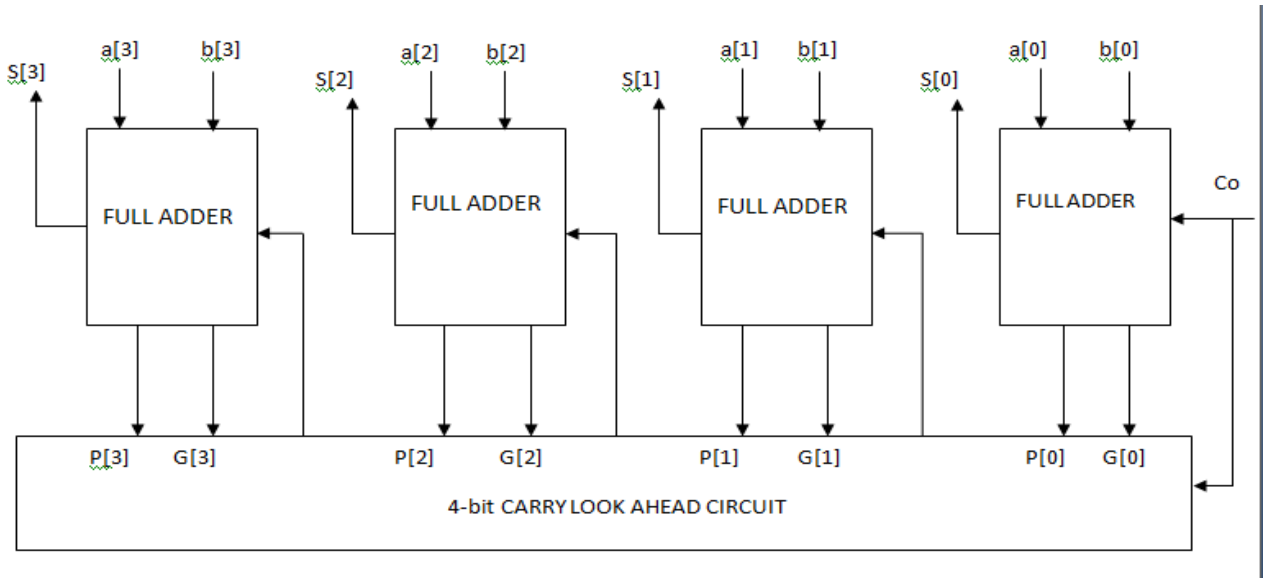

Fig.-2 Carry Look Ahead Adder

2.3 Carry Select Adder

Carry Select Adder is one of the fastest adders by partitioning the adder into two groups, each of which performs two addition in parallel. In the CSL, both the operands Ai and Bi are divided into k blocks of possibly different sizes as shown in the scheme below. One block takes cin as its initial carry and is implemented typically by RCA. The other block implements RCA assuming cin=1 and 0 simultaneously[5]. Once, the carry signals are finally computed, the correct sum and the carryout signal is simply selected by a set of multiplexers.

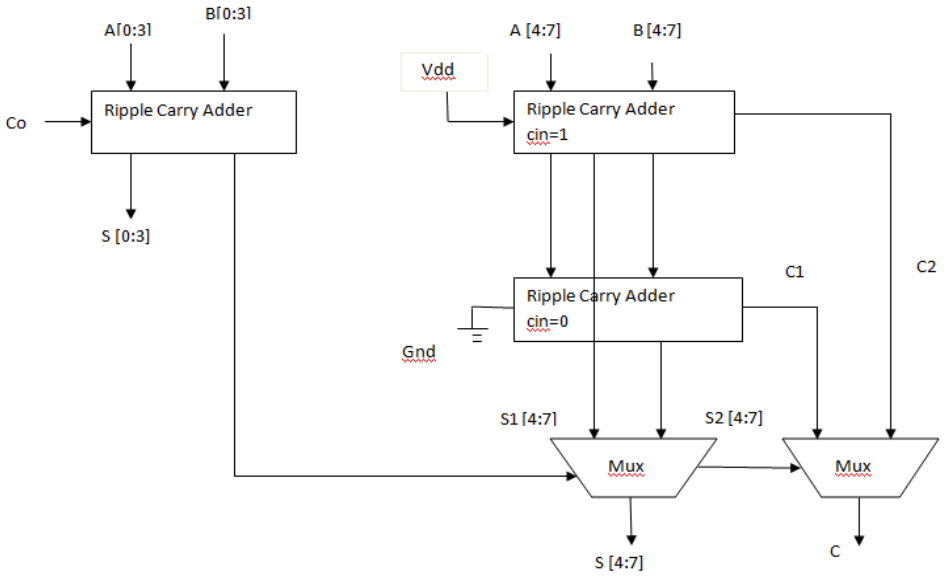

Fig.-3 Carry Select Adder

2.4 Carry Save Adder

In Carry Save Adder, three bits are added parallelly at a time as shown in the fig.4 below. In CSA, instead of propagating the carry, it saves its carry and updates it as addend value in the next stage. Hence, the delay due to carry is reduced in this scheme.

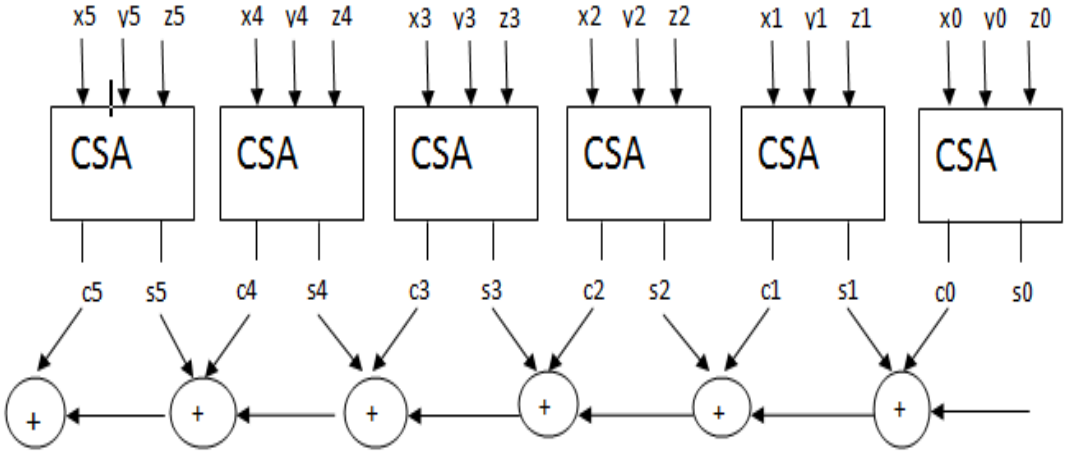

Fig.4 Carry Save Adder

2.5 Carry Skip Adder

Carry Skip Adder uses a concept of skipping over groups of successive adder stages to reduce the carry propagation time. In CSK, N-bit RCA is divided into 4-bit blocks and each block has four stages ranging from 4k to 4k+3 where k is the number of the block[1] as shown in the scheme below. It is designed to speed up the addition operation by adding a propagation of carry bit around a portion of the entire adder. We denote the block carry propagation signal as:

$$P_{[4k,4k+3]} = P_{[4k]} . P_{[4k+1]} . P_{[4k+2]} . P_{[4k+3]} \quad \text{(iii)}$$

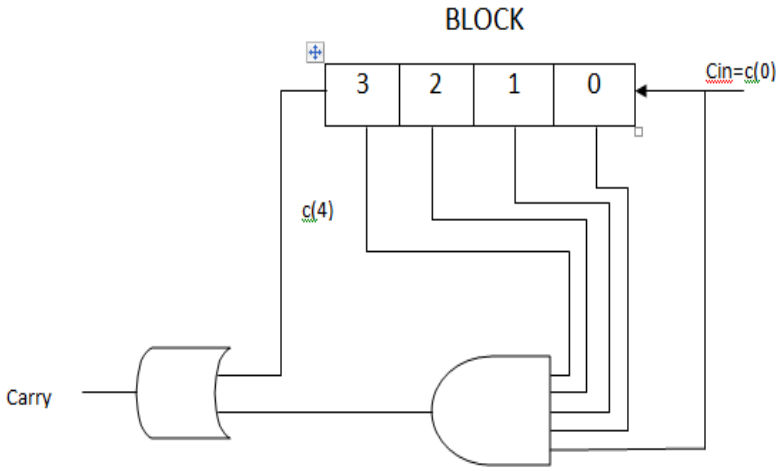

Fig.-5 Carry Skip Adder

2.6 Koggy Stone Adder

Koggy Stone Adder as shown in Fig.6 is one of the fastest parallel prefix adders.

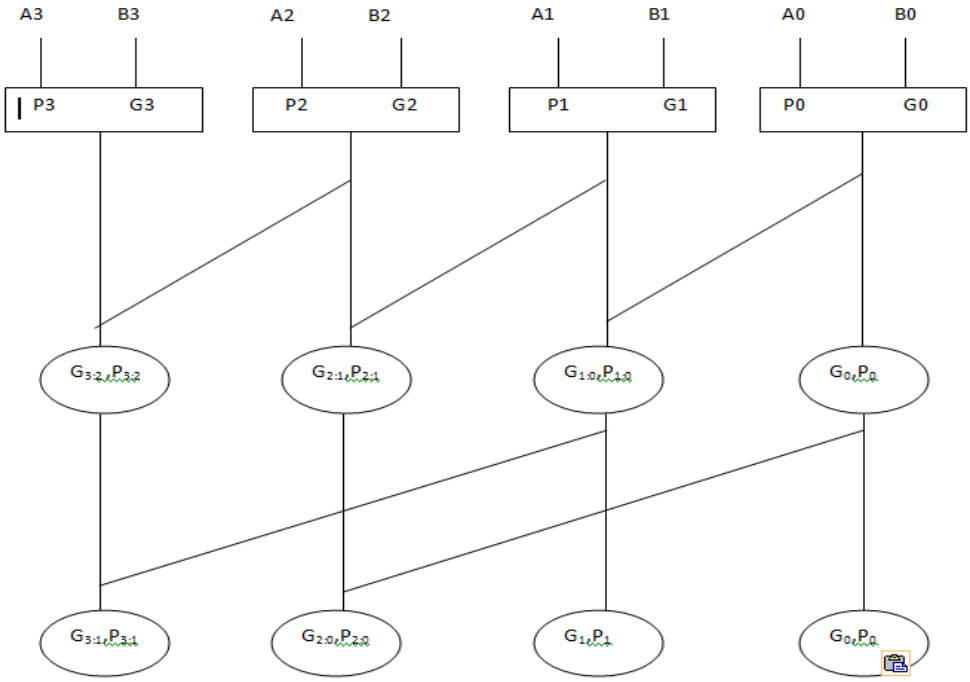

Fig.-6 Koggy Stone Adder

It generates carry in O(logn) time and is widely considered as the fastest adder and is widely used in industries in high-performance arithmetic circuits. In KSA, carries are computed fast by computing them in parallel at the cost of increased area [4].

III. DESIGN AND IMPLEMENTATION

As discussed in the literature review, we have compared the 6 different types of 8-bit high-speed adders. The implementation is done on Xilinx Vivado v.16 Virtex7, and delay and power has been compared as shown the Fig7 and 8 respectively below:

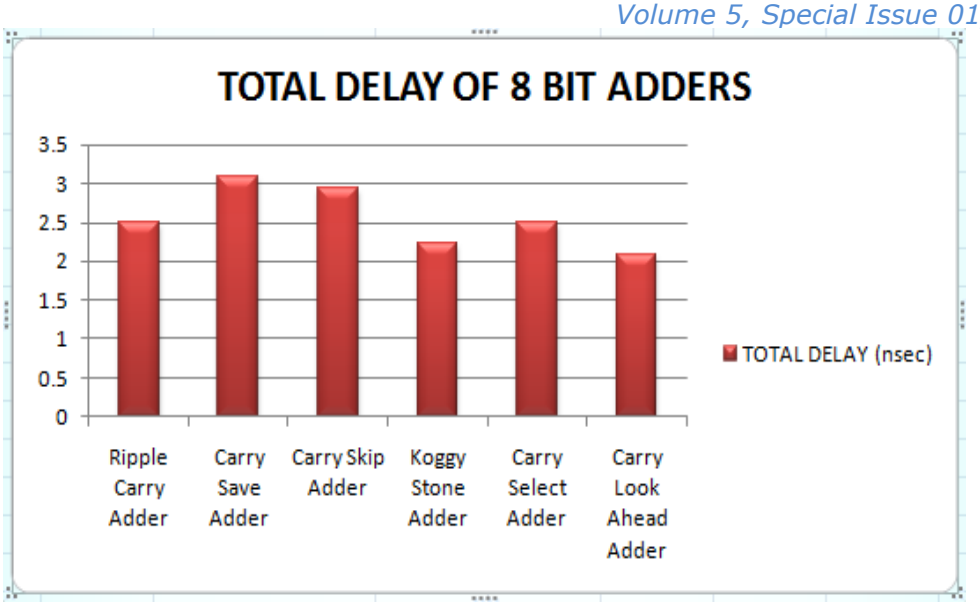

Fig.7- Comparison of 6 8-bit adders on the basis of delay

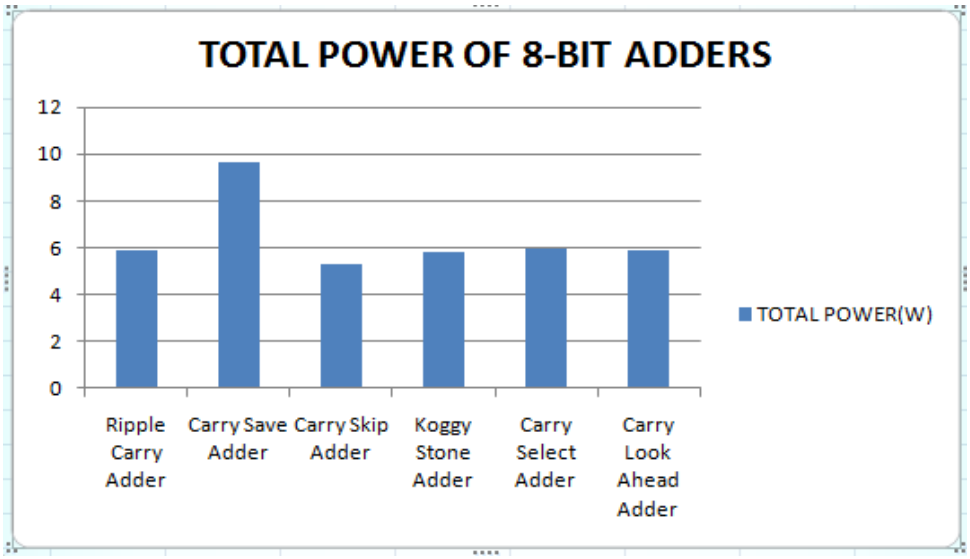

Fig.8- Comparison of 6 8-bit adders on the basis of power

From, the above performed analysis graphs, it is observed that Carry Select Adder(CSL), Carry Look Ahead Adder(CLA), Koggy Stone Adder have achieved better results in terms of delay and power. The power and delay comparison of above mentioned adders have been done in 32-bits and is illustrated in Table 1 below:

Table 1: Comparison of 32-bit adders on the basis of delay and power

ADDERS	LOGIC DELAY (nsec)	NET DELAY (nsec)	TOTAL ON-CHIP DELAY (nsec)	DYNAMIC POWER (W)	STATIC POWER(W)	TOTAL POWER(W)
KOGGY STONE	0.360	3.289	3.649	22.463	0.649	23.112
CARRY SELECT	0.450	4.147	4.597	23.906	0.699	24.605
CARRY LOOK AHEAD	0.765	6.543	7.308	22.507	0.650	23.157

From the above table, we have the Carry Select Adder (CSL) and Koggy Stone Adder as the best among the following in terms of delay and power. Table 2 illustrates the comparison between these two adders in 64-bits.

Table 2: Comparison of 64-bits adders on the basis of delay and power

ADDERS	LOGIC DELAY(nsec)	NET DELAY(nsec)	TOTALON-CHIP DELAY(nsec)	DYNAMIC POWER(W)	STATIC POWER(W)	TOTAL POWER(W)
KOGGY STONE ADDER	0.360	3.289	3.649	45.582	2.233	47.815
CARRY SELECT ADDER	0.900	7.805	8.705	47.939	2.531	50.470

Various adders have been implemented using Xilinx Vivado v.16 using Virtex7 family. It is concluded that Koggy Stone Adder achieves better performance in terms of delay and power among all the above implemented adders as shown in table 2. The synthesised Koggy Stone Adder is shown in fig-9.

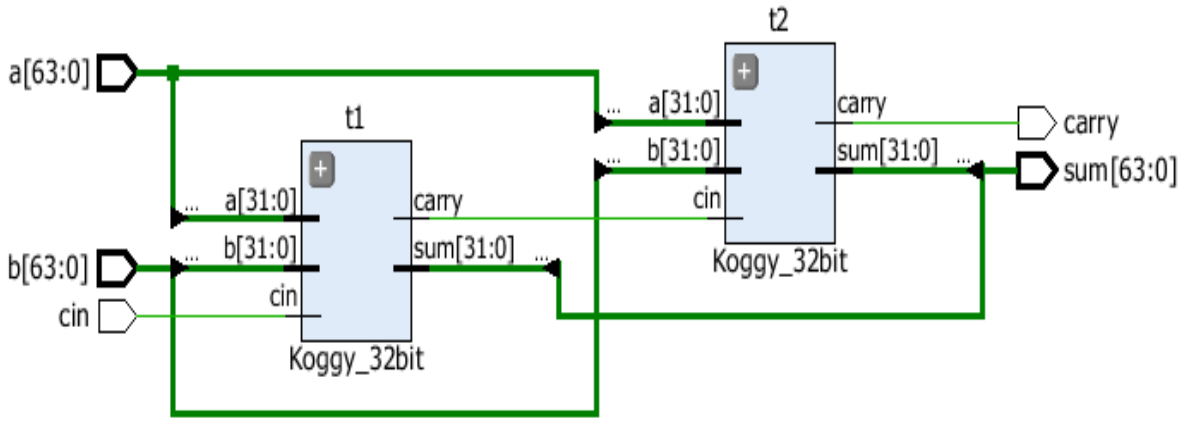

Fig.-9

IV. CONCLUSION

Koggy Stone Adder is having the minimum delay and power among all the 6 adders implemented in this paper. Though there are adders which have high speed but not very power efficient so as per application of the circuit we can use the other circuits. The high speed adders are used for implementing high speed multipliers.

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