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FPGA Implementation of Zero-Forcing Pre-coding for MIMO WiMAX Transceivers

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Abstract- *Next generation wireless communication networks are expected to achieve increasing data rates. To obtain the expected performance Multi-User Multiple–Input–Multiple–Output (MU–MIMO) is a key technique. In MU–MIMO systems, the base stations transmit signals to two or more users over the same channel, because of which every user can experience inter-user interference. In Multiuser MIMO (MU-MIMO) systems, pre-coding is essential to eliminate or minimize the multiuser interference (MUI). The design of a suitable pre-coding algorithm with good overall performance and low computational complexity at the same time is quite challenging, especially with the increase of system dimensions. In this paper, FPGA implementation of a novel low-complexity high-performance pre–coding algorithm that is able to mitigate the multi–user interference of the MU-MIMO systems in the context of a realistic WiMAX application scenario is proposed.*

Keywords- *Zero-forcing Algorithm, Pre-coding, multiuser multiple-input multiple-output (MU-MIMO), Singular Value Decomposition (SVD), Signal to Noise ratio (SNR), Coordinate Rotation Digital Computer (CORDIC)*

I. INTRODUCTION

There has been considerable recent interest in wireless multiple-input, multiple-output (MIMO) communications systems, because they allow for drastic enhancement of system throughput and energy efficiency. It was realized that designing wireless digital communication systems that efficiently exploit the spatial domain of the transmission medium allows a significant increase of spectral efficiency. This can be achieved using Multiple Input Multiple Output (MIMO) technique [1], [2], [3] based on multiple antennas at both the transmitter and receiver sides.Multi-user (MU) MIMO systems have the potential to combine the high capacity achievable with MIMO processing with space division multiple access [4]. This allows the transmission of multiple spatially multiplexed data streams to multiple users and thus results in very high data rates.In MU-MIMO operations, two or more users share the same time-frequency resources, and several parallel data streams can be simultaneously transmitted, one for each user. In the downlink (DL) channel, when the base station transmits over the same channel to two or more simultaneous users, every user is exposed to inter–user interference, generated by the signals transmitted to other users [2].To overcome the problem of the multiple access interference (MAI), it is possible to employ multiple–user detection (MUD) [2] at the receiver side, but such techniques are often economically too costly to use at the receivers.It would be better to mitigate the MAI at the transmitter side by properly designing the transmitted signals. So, the inter–user interference can be mitigated by pre–coding the signals that have to be transmitted.Design for the multiple-input single output (MISO) multiuser broadcast channel is an important problem in modern wireless communication systems. The main difficulty in this channel is that coordinated receive processing is not possible and that all the signal processing must be employed at the transmitter side.
From signal processing point of view, there are still many open queries and search is on, aimed at finding efficient yet simple transmitter design algorithms. In particular, linear pre-coding schemes which seem to provide a promising trade-off between performance and complexity were proposed in [5]–[6].The most common linear pre-coding approach is zero-forcing (ZF) beam forming which is a suboptimal approach and has attracted considerable attention since there are computational difficulties even within the class of linear pre-coding strategies.This paper proposes FPGA implementation of a pre–coding algorithm able to mitigate the multi–user interference of the MU-MIMO systems in the context of a realistic WiMAX application scenario. Some part of simulation results have been shown and future results will clearly evidence the benefits achieved by the proposed pre–coding technique in terms of increased capacity, SNR and BER

II. ZERO-FORCING PRE–CODING ALGORITHM

In this section, an overview of the considered Zero-Forcing pre–coding algorithm is presented.ZF decouples the multiuser channel into multiple independent sub channels and reduces the design to a power allocation problem. Consider a multiuser DL MIMO channel with “K” users and a base station (BS). The received data for standard MISO multiuser broadcast channel is given by

$$y_k = h_k^H + w_k, \qquad k = 1,2 \ldots\ldots k \qquad (1)$$

where y_k is the received data of the kth user, h_k is the channel parameter to this user, x is the transmitted vector and w_k is complex Gaussian noise samples. For simplicity, we use the following matrix notation

$$y = HX + w \qquad (2)$$

where $y = [y_1, \ldots, y_k]^T$, $H = [h_1, \ldots, h_k]^H$ and $w = [w, \ldots, w_k]^T$

Consider BS has n_T transmit antennas and the j^{th} receiver has n_{Rj} antennas. Thus the total number of antennas at all receivers will be $n_R = \sum n_{Rj}$. The channel is modelled by an $n_R \times n_T$ matrix **H** so that each of its elements is viewed as the transmission coefficient linking one of the transmit antennas with one of the receive antennas.
Now considering a MU-MIMO transmission system that includes linear pre–coding performed at the transmitter. The received signal $\hat{d}$ can be defined as

$$\hat{d} = \mathbf{HMd} + \mathbf{n} \qquad (3)$$

where **d** is a data vector of arbitrary dimension $n_T \times m$, **M** is the $n_T \times m$ pre–coding matrix.
To eliminate the multi user interference the condition is $H_i M_j = 0$ for $i \neq j$. The computation of the pre–coding matrix **M** becomes then extremely important [7].It is possible to find the optimal pre–coding matrix **M** such that all MUI is eliminated by choosing a pre–coding matrix M_j that lies in the null space of the other users' channel matrices. In order to achieve that goal, the channel matrix of each user is required. Zero-Forcing(ZF) algorithm tries nulling of the MUI completely. A MU–MIMO DL channel is then decomposed into multiple parallel independent SU MIMO channels [8]. The main idea behind the method relies on the computation of the BD matrix via a Singular Value Decomposition (SVD) [9].Figure 1 shows the flowchart of the ZF Algorithm.First step is the computation of SVD of the matrix $\widetilde{H}_j$. $\widetilde{H}_j$ is definedas:

$$\widetilde{H}_j = \left[H_1^T \ldots\ldots\ldots H_{j-1}^T H_{j+1}^T \ldots\ldots.. H_K^T\right]^T \qquad (4)$$

The zero MUI constraint forces M_j to lie in the null space of $\widetilde{H}_j$
The SVD of $\widetilde{H}_j$, whose rank is $\tilde{L}_j$, provides:

$$\widetilde{H}_j = \widetilde{U}_j \widetilde{\Sigma}_j \left[\widetilde{V}_j^{(1)} \widetilde{V}_j^{(0)}\right]^* \qquad (5)$$

Where * indicates the Hermitan transpose. We choose the last right $n_T - \tilde{L}_j$ singular vectors $\widetilde{V}_j^{(0)}$ which form an orthogonal basis for the null space of $\widetilde{H}_j$. The equivalent channel of user *j* after eliminating the MUI is identified as $H_j \widetilde{V}_j^{(0)}$, whose dimension is $n_{R_j} \times (n_T - \tilde{L}_j)$ and is equivalent to a system with $n_T - \tilde{L}_j$ transmit antennas and n_{R_j} receive antennas. Each of these equivalent SU MIMO channels has the same properties as a conventional SU MIMO channel.
In the second step the SVD is re–computed on the product $H_j \widetilde{V}_j^{(0)}$ that yields:

$$H_j \widetilde{V}_j^{(0)} = \cup_j \Sigma_j \left[V_j^{(1)} V_j^{(0)}\right]^* \qquad (6)$$

and let the rank of the *j*-th user's equivalent channel matrix be L_j. The product of the first L_j singular vectors $V_j^{(1)}$ and $\widetilde{V}_j^{(1)}$ produces an orthogonal basis of dimension L_j and represents the transmission vectors that maximize the information rate for user *j* subject to the zero MUI constraint.

The operations for each user are repeated until the condition $j < K$ is valid, where K is the number of users.
Finally, the modulation matrix is defined as:

$$M = \left[\widetilde{V}_1^{(0)} V_1^{(1)}, \widetilde{V}_2^{(0)} V_2^{(1)}, \ldots\ldots., \widetilde{V}_K^{(0)} V_K^{(1)}\right] \Lambda^{1/2} \qquad (7)$$

where Λ is a diagonal matrix whose elements λ_i scale the power transmitted into each of the columns of **M**. Theoptimal power loading coefficients in Λ are found usingwaterfilling [10] on the diagonal elements of the singularvalues contained in the matrix Σ given a pre–defined total power constraint.

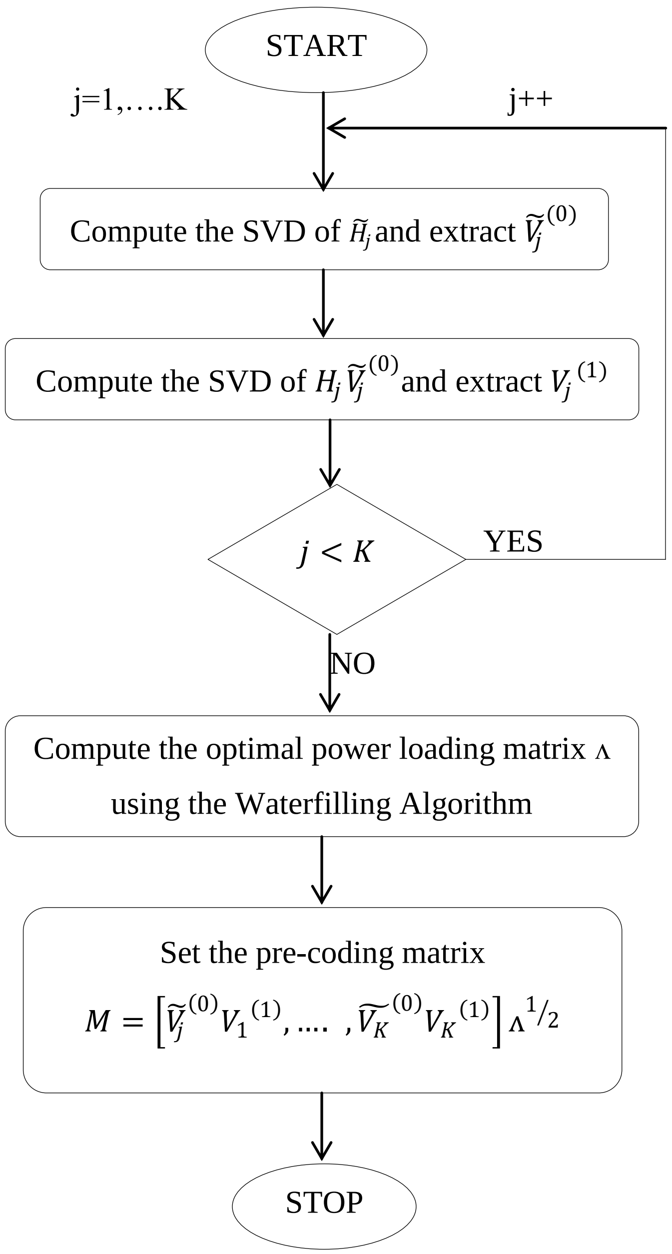

Figure 1. Flow Chart of Zero forcing Algorithm

III. SINGULAR VALUE DECOMPOSITION

Let X denotes an m × n matrix of real-valued data and *rank*r, where without loss of generality $m \geq n$, and therefore $r \leq n$.
The equation for singular value decomposition of X is the following:

$$X = USV^T \qquad (8)$$

Where U is an m × n matrix, S is an n × n diagonal matrix, and V^T is also an n × n matrix.
If the matrices *U, S and V* are partitioned by columns as:

$$U = [u_1, u_2, \_\_\_, u_m]$$

$$S = diag\,[\sigma_1, \sigma_2 \_\_\_, \sigma_n]$$

$$V = [v_1, v_2 \_\_\_, v_n]$$

Then σ_i is the i^{th}singular value of X, andu_i and v_i are the left and right singular vectors corresponding to σ_i. If X is real, then the unitary matrices U and V arereal and hence orthogonal.

The singular value decomposition (SVD) has been computed using the Coordinate Rotation Digital Computer (CORDIC) algorithm.

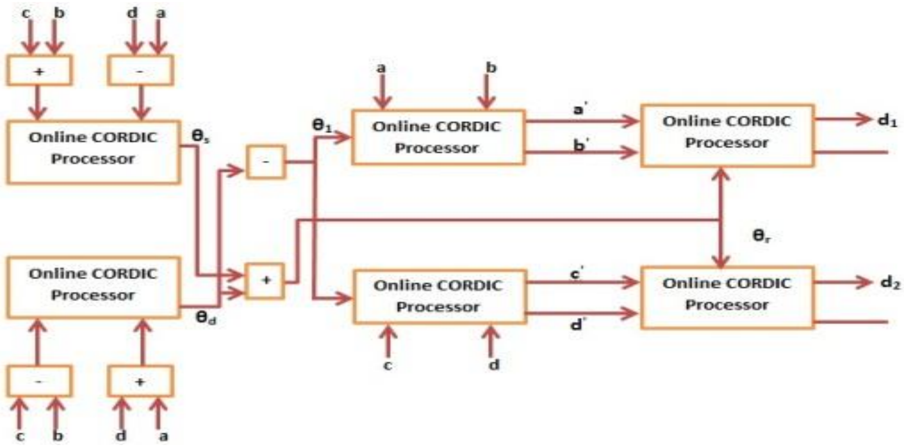

Figure 2 SVD computation using CORDIC processor

CORDIC allow fast iterative hardware calculation of sine, cosine, arctan, sinh, cosh, arctanh, products, quotients, square roots, and conversion between binary and mixed radix number systems. Real-time signal processing combined with the performance and hardware advantages makes CORDIC an attractive alternative to traditional arithmetic units for special-purpose hardware design.

IV. SIMULATIONS AND RESULTS

The first step in the design of Zero-Forcing algorithm is the design of SVD algorithm. As earlier mentioned we have implemented the SVD function using the CORDIC processor. Figure 3 shows the register-transfer level (RTL) diagram of an online configuration for SVD computation using CORDIC processor.

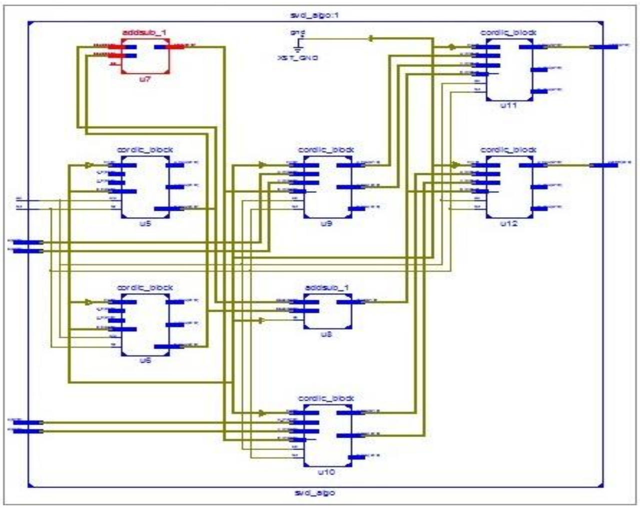

Figure 3 An RTL configuration for SVD computation using CORDIC processor

Table below gives the device utilization summary of SVD computation algorithm.

Table 1 Device Utilization Summary

Logic Utilization	Used	Available	Utilization
Number of Slice LUTs	192	19200	1%
Number of fully used LUT-FF pairs	0	192	0%
Number of bonded IOBs	192	220	87%

The ZF algorithm will be evaluated with the help of Simulink–based model shown in Figure 4.

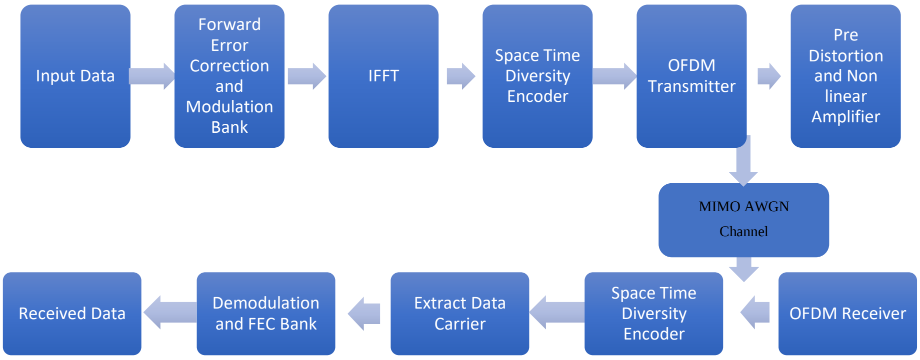

Figure 4 Proposed model used for simulations

The model has the following basic features.

- Forward Error Correction (FEC) consisting of Reed-Solomon (RS) code concatenated with convolutional codes (CC).
- Data interleaving.
- Modulation using BPSK, QPSK, 16–QAM or 64–QAM.
- OFDM transmission using 192 sub-carriers, 8 pilots, 256-point FFTs, and a variable cyclic prefix length.
- Distortion and nonlinearity removal using Digital Pre distortion and nonlinear Amplifier.
- A single OFDM symbol length preamble that is used as the burst preamble.
- WiMAX standard framing
- OFDM receiver that includes channel estimation using the inserted preambles.

The considered MIMOmodel is based on the assumptions of uncorrelated paths. Each path has been modelled as a SISO Rayleigh Fading Channel.

V. CONCLUSIONS

So far the work presented here is the overview of ZF algorithm and implementation of CORDIC based processing element for the implementation of singular value decomposition (SVD) function.It is an efficient algorithm suitable to be implemented in DSP algorithms. It's calculations for complex arithmetic is simple and elegant. It uses CORDIC module to perform the necessary arithmetic operations. Besides, since it avoids using multiplication, adopting the CORDIC algorithm can reduce the complexity and the net result is a flexible computational processing element for digital signal processing algorithms.

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