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DESIGN OF 2 - DIMENSIONAL PHOTONIC CRYSTAL BASED ALL-OPTICAL HALF SUBTRACTOR

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Abstract— *Forthcoming Optical computers and Optical signal Processors need all-optical devices in order to get rid of from Optical-Electrical-Optical conversions; Optical gates play a vital role in Optical networks. Photonic crystals (PhC) are periodic dielectric structures that have a band gap that forbids the propagation of a certain frequency range of light. This property enables one to control light with amazing facility and produce effects that are impossible with conventional optics and its dielectric constant can be varied occasionally. In this paper, Photonic crystal based Optical Half Subtractor on hexagonal lattice pattern with circle shaped rods is proposed. The Half Subtractor enactment can be upgraded by providing proper distinct space in output power between '0' and '1' logical states and operate well even in the reduced input power level. Errors during the identification of logical states (Logic '0' and Logic '1') can be condensed by establishing a threshold for output power. If the output power level is more than 0.7μW or less than 0.35μW, then it is regarded as logic '1' and logic '0' respectively. Another advantage is found with its contrast ratio which is about 7.78 dB and 11.76 dB for Difference and Borrow respectively. Compactness and ease of design are the characteristics which makes suitable for Photonic Integrated Circuit (PIC) applications.*

Keywords— *All-Optical Half Subtractor, Photonic Crystal (PhC), Electric Field, Polarization.*

I. INTRODUCTION

In order to overcome the speed limitation enacted by the electronic devices, All-Optical communication is the best solution. Since digital gates are complicated for optical signal processing and also inconvenient for electro-optic conversion. It demands for the necessity that entire components which are used in optical networks should be all-optical elements. Photonic crystals (PhCs) are periodic structures in one or more spatial directions and offer a way to control light. One of the properties of PhC is the existence of a photonic band gap (PBG) i.e., a frequency range for which light propagation is forbidden inside the structure [1]. Gates plays an important role in realization of all-optical functions since it is the key element. More advantages behind all-optical logic gates over electronic logic gates are its compactness, free from short circuits and electronic interference, transmission only with minimum loss etc.[2]. Another requirement is the transmission bandwidth which is the great need for all tele communication as well as data communication. All optical communication overcomes the problems faced by electronics system by its elegant features. In present days, researchers focusing on optical computing domain in order to increasing the processing speed to terabits per second. These can be achieved only when the signals are processed in terms of optical form where there is no requirement for O-E and E-O conversions [3]. Photonic Integrated Circuits (PIC) has begun superior among all other known technology because of its low cross talk, high bandwidth, less transmission delay etc. For PIC applications, lot of Gates are designed [3-14] by various authors using various techniques, since there is no optimized designed is made. The exponentially growing demands are fulfilled by Photonic crystal designing of all-optical components[15]. For PIC applications, the components like splitter, Couplers, Multiplexer / demultiplexer, modulators / demodulators, circulators / isolators, logic devices and switches / routers [16-18] are designed using photonic crystals. Among these, design and development of logic devices such as gates leads to half adder, encoders [19] switches [20] etc., has been increasing gradually because of their high speed signal processing, compactness and low power consumption. For the design of optical logic gates and optical integrated circuits, PhCs has the applicable structure. In recent times, a lot of attempts have been endeavored based on Photonic crystals for the design of all optical logic devices [21]. The smallest unit for subtraction process is Subtractor and it is used for arithmetic calculation as well as in other parts of the processors for calculating address [22]. The device which is to be designed should satisfy some required parameters such as speed, area, power consumption [23].

In future world, the fabrication of photonic integrated circuits finds a lot of applications in which the optical logic circuits and logic gates acts as the base. Among these logic circuits, not only the gates and adders play a key role in PIC but also other devices play a vital role. In this paper, an all-Optical Half Subtractor is proposed with a good split-up capability to classify logic "0" and logic "1" in output port. The minimum tolerable electric field that can be used as logic "1" is increased in our proposed PhCs based all-optical Half Subtractor which also increases the contrast ratio. In the design of the PhCs based optical logic gates, logic '1' is considered as ON and logic '0' as OFF. The important operation of logic gates is to control the interval variation between the maximum electric field in "0" state, and minimum

in "1" state which is defined as the undefined region, thereby the probability of error in sensing logic "1" and logic "0" will be diminished. This gate forms the basis for all upcoming optical components. The wavelength for the simulation should be in PBG range in order to limit and conduct the light in defect lines. Thus, the 1550 nm wavelength is chosen for simulating the proposed structure.

II. CONVENTIONAL HALF SUBTRACTOR DESIGN

Half Subtractor is simply unique in structure that can be used for both combinational and arithmetic logic circuits. It has two inputs which can be subtracted to produce two output bits as Difference and Borrow. The two inputs are Minuend (A) and Subtrahend (B) such that the minuend is nothing but the first input in subtraction and subtrahend is the number from which another input (B) to be subtracted. The truth table for the half Subtractor is shown in Table 1.

Table 1: Truth table of Half Subtractor

Truth Table			
Input		Output	
Minuend (A)	Subtrahend (B)	Difference (D)	Borrow (BW)
0	0	0	0
0	1	1	1
1	0	1	0
1	1	0	0

The output at Difference Port will be Logic '1' for the case of dissimilar inputs (i.e., A=0, B=1 or A=1, B=0) and it will be Logic '0' for the case of equal inputs (i.e., A=B=0 or A=B=1). Subsequently, the Borrow output will be Logic '1' for only one case (i.e., A=0 & B=1). This is because, in order to subtract HIGH input from LOW input which is impossible, there is a need to borrow an input to perform such subtraction operation, so that the borrow port appears high output for certain case. For all other case (i.e., A=B=0, A=1,B=0 & A=B=1) there is no need to borrow an input since there subtraction is happened from HIGH input. The Difference output bit is considered as the least significant bit (LSB) of the two bit binary addition and the Borrow output bit represents the most significant bit (MSB) of the two bit binary addition. According to the truth table, the functions are derived as follows:

$$\text{Difference 'D'} = A \oplus B \quad (1)$$

$$\text{Borrow 'BW'} = \overline{A} \cdot B \quad (2)$$

From the above equations, it is clearly agreed that the functionality of the half Subtractor depends on those two logic gates such as XOR and AND (with inverted 'A' input). The schematic diagram of conventional half Subtractor is shown in Figure 1.

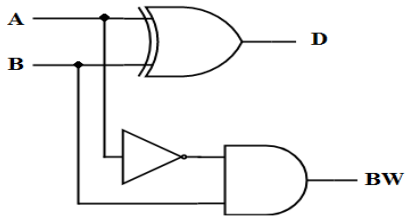

Figure 1: Schematic of binary Half Subtractor

DESIGN AND OPERATION

LAYOUT NARRATION

The proposed design has 19 x 19 arrays of 2-D PhC silica dielectric rods embedded in air substrate of refractive index (n=1) in hexagonal lattice which analogous to fused coupler with waveguides. In this structure, the defects are created by removing the corresponding PhC dielectric rods in the structure that forms the waveguide. The refractive index of chosen Silica rods is about 3.46 and the dielectric constant 'ε_r' is about 11.56 [21]. The radius 'r' of the rods in this work is considered to be 0.18a; where 'a' is known as the lattice constant which is the distance between two dielectric rods. In this design, several junction rods and reflection rods are used. The radius for each junction/reflection rods are chosen as 0.09a so that the Half Subtractor can produce the anticipated output and it is noticed that the maximum power is transmitted at the output ports (Difference and Borrow output Port). Figure 2 shows the layout of all-optical half Subtractor design and it is simulated using finite difference time domain (FDTD) method.

BANDGAP CONFIGURATION

The Plane Wave Expansion (PWE) method is used for obtaining the band structure. Figure 2 shows the normalized band structure for proposed structure. The band structure is obtained for the TE mode. The calculated band structure depicts that the main Photonic Band Gap (PBG) is situated in the range of a/λ = 0.29 to 0.479, such that the wavelength equivalent of this range is 1.29 to 2.13 µm. Then the selected wavelength sources should be in this PBG range and therefore λ = 1550 nm is used for this simulation.

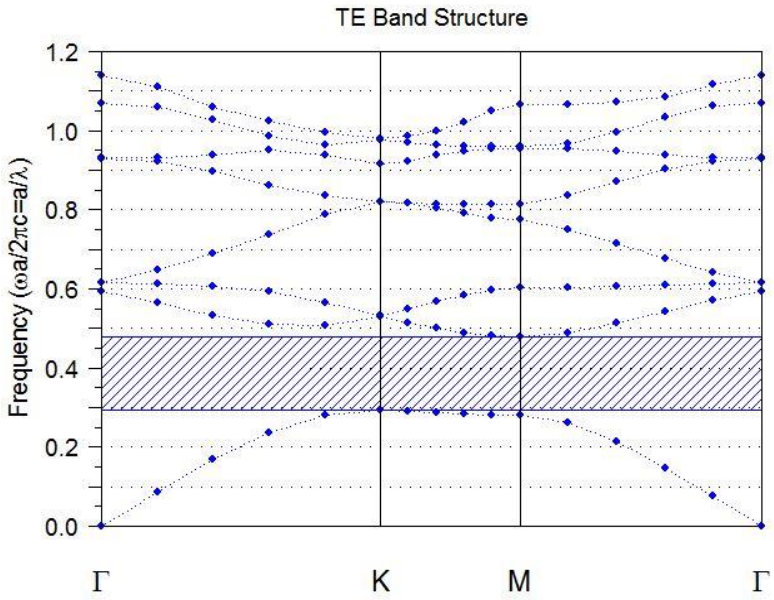

Figure 2: Calculated bandgap for proposed Structure

IV EFFECTS AND EVALUATION

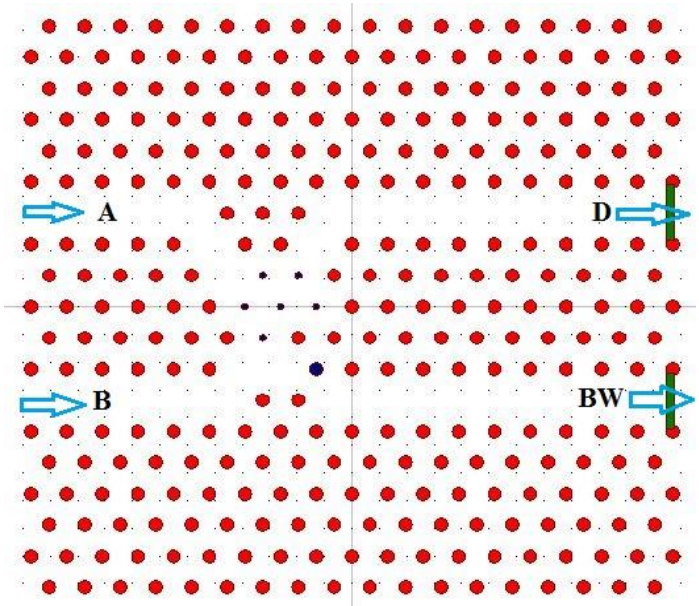

Figure 3: Design for half-Subtractor

The proposed Optical Half-Subtractor has two inputs (A and B) and two outputs (D and BW), where D is the Difference of two inputs and BW is the Borrow output bit. Two optical sources with 1550 nm wavelength are used as inputs. The defect lines of the inputs and outputs of the proposed half-Subtractor are shown in the layout (Figure 3).

The defect lines are selected to intercross each other. The radius of five (blue colored) rods is reduced to 0.5r in their crossing, where r is the radius of base (red colored) rods. These rods act as scatterers which will control and conduct electric field in their output ports.

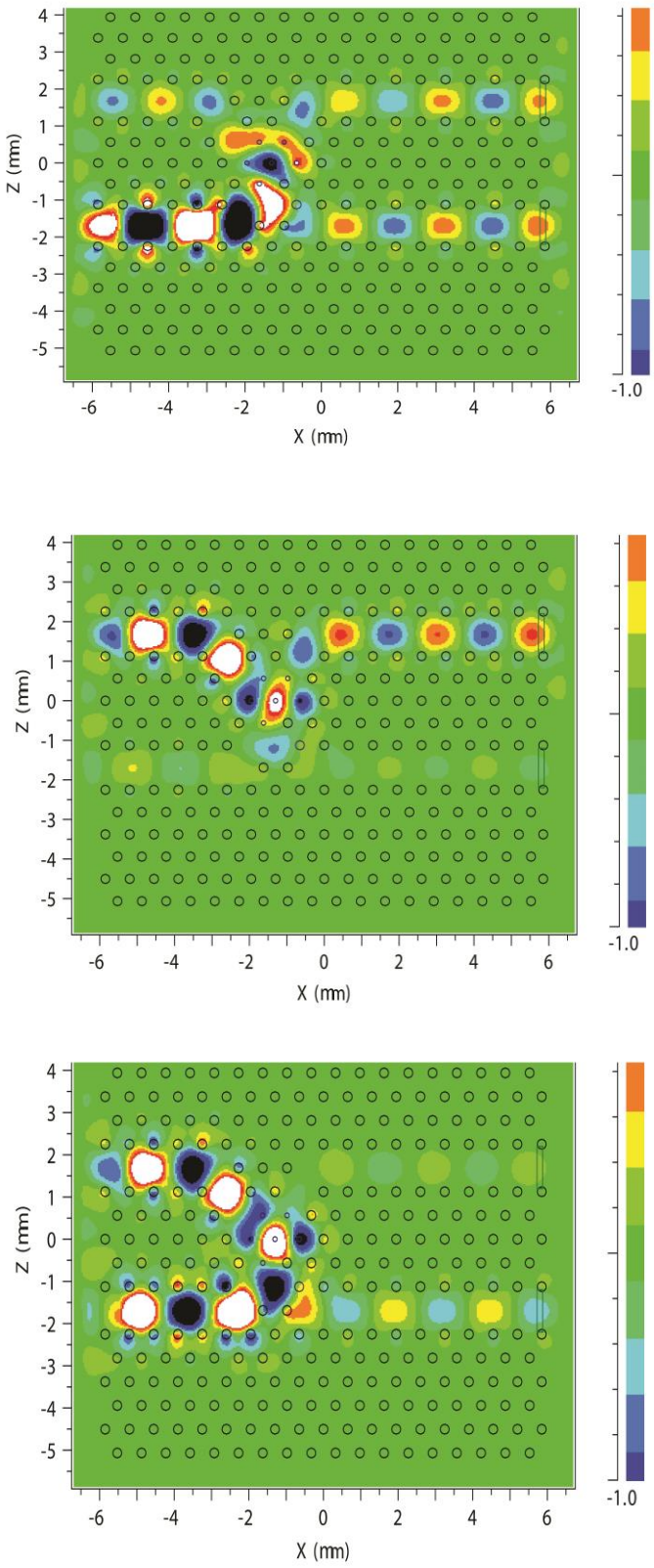

Figure 4: Electric field distribution of inputs a) A = 0, B = 1 b) A = 1, B = 0 c) A = B = 1

When the two input sources are in off state (A = B = 0) there is no possible for electric field distributions in the outputs, then D and BW will be in logic'0' state. For a special case of A = 0 and B = 1, the output is HIGH at both the outputs. When the inputs A = 1, B = 0, the output at D is significant than the BW output. If both of the inputs are HIGH then both of the outputs are LOW. All those cases are clearly shown in Figures 4 (a) (b) and (c).
Table 2 shows the results of the proposed structure that confirms the operation of half Subtractor.

Table 2: Input and output values for half Subtractor at 1550 nm

Input power = 1.0 μW							
INPUT				OUTPUT			
A		B		D		BW	
VALUE	LOGIC	VALUE	LOGIC	VALUE	LOGIC	VALUE	LOGIC
0	0	0	0	0	0	0	0
0	0	1.0	1	0.85	1	0.75	1
1.0	1	0	0	0.9	1	0.05	0
1.0	1	1.0	1	0.15	0	0.25	0

In this simulation, the variation of the electric field is calculated and illustrated in Figures 5, 6 and 7 for the C-band wavelength range (1530 nm to 1610 nm). There is a existence of path loss which is caused by reflection and propagation of light to the undesired output path which should be in logic '0' state. The desired output value which should be set in logic '1' state is also decreased because of these losses. Some amount of these losses emerged from the output port with logic state '0' as shown in these figures. This difference arises because of imperfect symmetry of two defect lines in this structure.
In the case of A = B = 0, both outputs are exactly zero and there is no error. In such special case of A = 0, B = 1, the output obtained at both ports of D and BW is HIGH as shown in Figure 6.

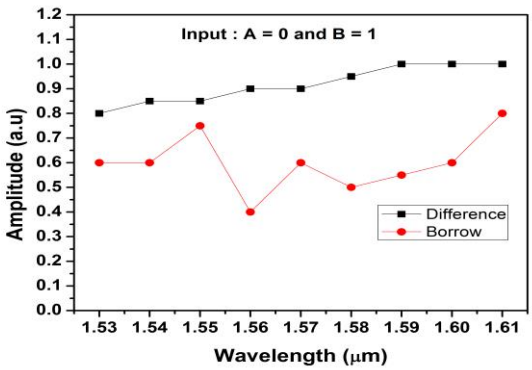

Figure 5: Output graph for various wavelengths with inputs A = 0 and B = 1

When A = 1, B = 0, the output at D is HIGH whereas in BW port the output is LOW. For example, in order to reduce the error detection, we introduce two terms such as Upper threshold (UT) (above which is regarded as logic '1') and Lower threshold (LT) (below which is regarded as logic '1'). In this simulation, the variation of the electric field is calculated and illustrated in Figures 5, 6 and 7 for the C-band wavelength range (1530 nm to 1610 nm).

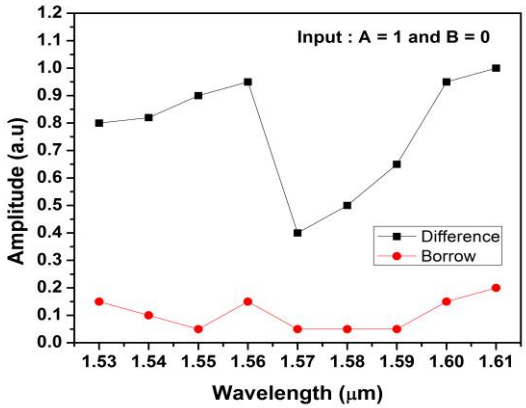

Figure 6: Output graph for various wavelengths with inputs A = 1 and B = 0

When both of the inputs are high such that A = B = 1, the output value of D and BW is obtained as 0.15and 0.25 respectively which indicates that it has the logic state '0' is shown in Figure 7.

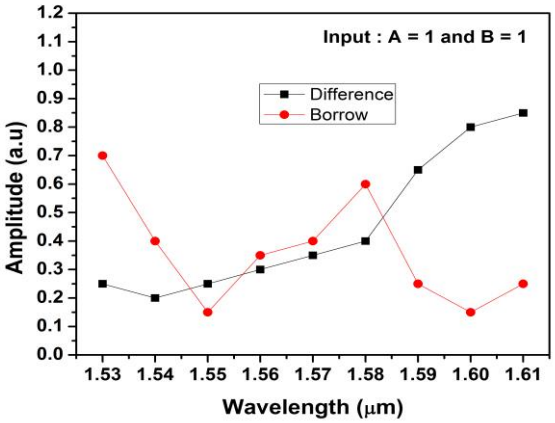

Figure 7: Output graph for various wavelengths with the inputs A=B=1

It is obvious from the figure 5 that the half Subtractor works well in the wavelengths of 1550 nm in which its Difference Borrow output lies above the upper threshold level. Further it is founded from the output graph obtained for the input A = 1, B = 0 as shown in Figure 6 such that it functions well in the wavelengths of 1550 nm in which it has both the maximum output for Difference and minimum output for Borrow. Also from the figure 7, it is found that for the input A = B = 1, it functions well in the wavelengths of 1550 nm in which it has minimum output for both Difference and Borrow.

The contrast ratio is defined as the ratio of ON power to the OFF power at individual ports. It is obtained by using the formula given as follow

$$CR = 10 \log PON/POFF \qquad (1)$$

where P_{ON} and P_{OFF} are the power levels of logic '1' and logic '0' respectively. The contrast ratio obtained at outputs *Difference* and *Borrow* is 7.75 dB and 11.76 dB respectively. This improved contrast ratio provides the significant role in Photonic Integrated Circuits.

From this work it is evident that the proposed design has better contrast ratio compared to the previous work and also our proposed Subtractor provides proper distinct space in output power between '0' and '1' logical states.

V CONCLUSION

All-Optical Half Subtractor based on PhC for the photonic Integrated Circuits are designed and its output is analyzed in terms of Difference and Borrow. The results for all four combinations of inputs of Half-Subtractor are analyzed. For a) A = 0, B = 1, b) A = 1,B = 0 c) A = B = 1 cases, the obtained output power level for Difference is 0.85 µW, 0.9 µW, 0.15 µW respectively and the corresponding Borrow output power is about 0.75 µW, 0.05 µW and 0.25 µW. Better distinct output power levels for logic '0' and logic '1' are obtained with less input power of 1 µW. Improved contrast ratio (7.78 dB for *Difference* and 11.76 dB for *Borrow*) and ultra-compatibility has also proved that this proposed compact design can be certainly used for photonic integrated circuits.

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