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Charge Injection & Clock Feed through Reduction Technique in Switched Capacitor Circuit

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Abstract —*Switched capacitor circuits fill a critical role in analog/digital interfaces particularly highly integrated applications. The switched capacitor circuits are introduced for better performance and reduced area in CMOS technology for both analog and digital functions. Basically switched capacitor circuits are combination of switches and capacitor. And this combination of switches and capacitor replaces the resistor by passes charge into and out of capacitors by controlling the switches. This chapter describes the basic building blocks and non-ideal effects of switched capacitor circuits. Channel charge injection and clock feed-through are two major non-ideal effects existing in switched capacitor circuit. This paper analysis the charge injection and clock feed through error in CMOS switched capacitor circuits. For this reason, the basic S/H topology is used.*

Keywords-*Resistor, MOSFET, sample and hold, channel charge injection, clock feed through,*

I. INTRODUCTION

Until the early 1970s, analog signal-processing circuits used continuous time circuits consisting of resistors, capacitors, and op amps. Unfortunate, the absolute tolerances of resistors and capacitors available in standard CMOS technologies are not good enough to perform most analog signal-processing functions. In the early 1970s, analog sampled-data techniques were used to replace the resistors, resulting in circuits consisting of only MOSFET switches, capacitors, and op amps. These circuits are called switched capacitor circuits and have become a popular method of implementing analog signal-processing circuits in standard CMOS technologies. One of the important reasons for the success of switched capacitor circuits is that the accuracy of the signal-processing function is proportional to the accuracy of capacitor ratios. The primary advantages of switched capacitor circuits include (a) compatibility with CMOS technology, (b) good accuracy of time constants, (c) good voltage linearity, and (d) good temperature characteristics. The primary disadvantages are (a) channel charge injection, and (b) clock feed through.

The important components of signal processing circuits are the signals. Signals can be characterized by their time and amplitude properties. From a time viewpoint, signals are categorized as continuous and discrete. Amplifiers has dealt with only cases where the input signal is continuously available and applied to the circuit and the output signal is continuously observed. Called continuous-time circuits, such amplifiers find wide application in audio-video, and high-speed analog systems. In many situations, we may sense the input only at periodic instants of time, ignoring its value at other times. The circuit then processes each “sample”, producing a valid output at the end of each period. Such circuits are called “discrete-time” or “sampled-data” systems. In this chapter, we study a common class of discrete-time systems called “switched-capacitor circuits.” Our objective is to provide the foundation for more advanced topics such as filters, comparators, ADCs, and DACs. Most of our study deals with switched-capacitor but the concepts can be applied to other discrete-time circuits as well.

II. RESISTOR EMULATION

The most basic and simplest switched capacitor circuit is the switched capacitor resistor, which is made up of one capacitor C and two switches S_1 and S_2 as shown in fig.1. Switches S_1 and S_2 are control by two non-overlapping clocks which connect to the capacitor with a given clock frequency alternately to the input and output of the SC.

A charge *q* transfers from the input to the output, in each switching cycle at the switching frequency f. Charge q on a capacitor can be given by:-

$$Cq = V \tag{2.1}$$

When switch S1 is closed, the charge transferred from the source to CS is:

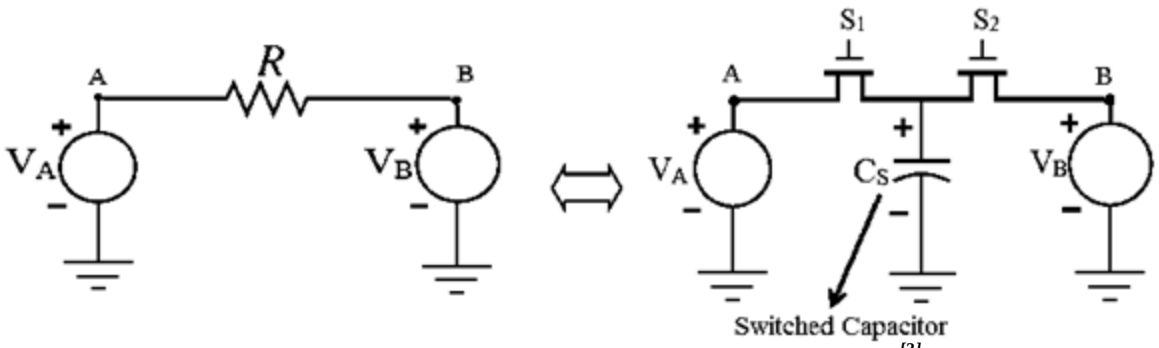
$$q_{IN} = C_S\ V_{IN} \tag{2.2}$$

When switch S2 is closed, the charge transferred from CS to the load is:

$$q_{OUT} = C_S\ V_{OUT} \tag{2.3}$$

The charge transferred in every clock cycle is:-

$$q = q_{IN} - q_{OUT} = C_S\ (V_{IN} - V_{OUT}) \tag{2.4}$$



"***Figure 1. Resistor Replace with Switched Capacitor Circuit*** [3]"

The current flow in the switched capacitor circuit can be given as:-

$$I = qf \tag{2.5}$$

Substituting for q in the above equation:-

$$I = C\,(V_{IN} - V_{OUT})\,f \tag{2.6}$$

The voltage across the circuit from input to output can be given as:-

$$V = V_{IN} - V_{OUT} \tag{2.7}$$

Using Ohm's law and putting values of I and V from above equations, value of R can be derived as:

$$R = \frac{V}{I} = \frac{V_{IN} - V_{OUT}}{C_S(V_{IN} - V_{OUT})f} \tag{2.8}$$

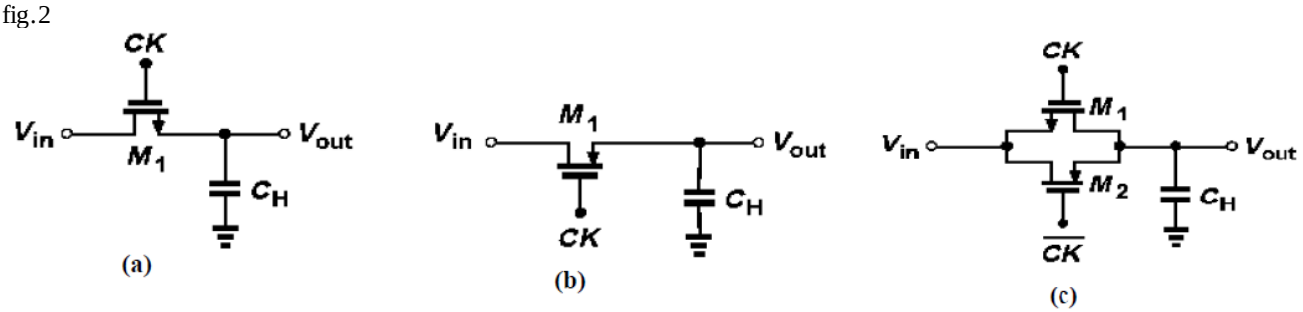
So,

$$R = \frac{1}{C_S f} \tag{2.9}$$

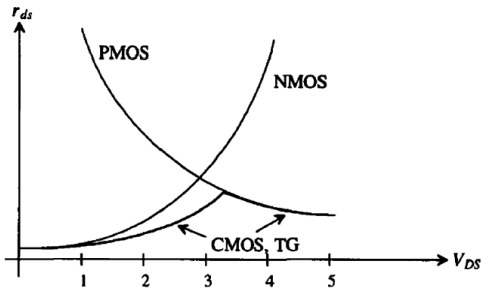
Thus, the SC can be replaced with a resistor whose value depends on capacitance value and switching frequency. The SC resistor is used as a replacement for simple resistors in integrated circuits because it is easier to fabricate reliably with a wide range of values. It has the benefit that its value can be adjusted by changing the switching frequency.

III. MOSFET AS A SWITCH

As shown in fig.1 MOSFET is used as a switch in switched capacitor circuit. A MOS transistor can be used as a switch because; it has the properties which are necessary for sampling. These properties are it can be on while carrying zero current and the drain to source voltage don't need to follow the variation of the gate voltage. So, if we neglect capacitances from the gate to the drain-source, we find that the gate control signal does not interfere with information being passed through the switch. The switch can be a PMOS, an NMOS or a Complementary MOS transmission gate as shown in fig.2



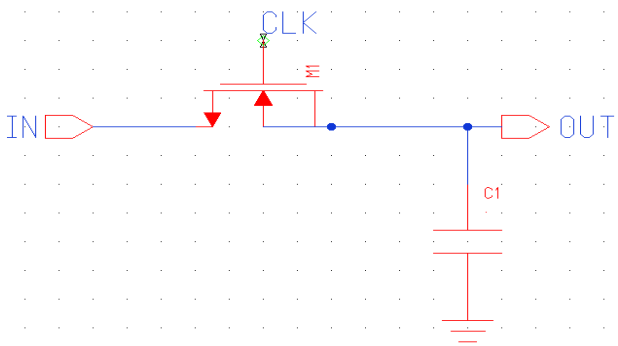
"Figure 2 (a)NMOS as a Switch (b)PMOS as a Switch (c)CMOS transmission gate as a Switch [3]"



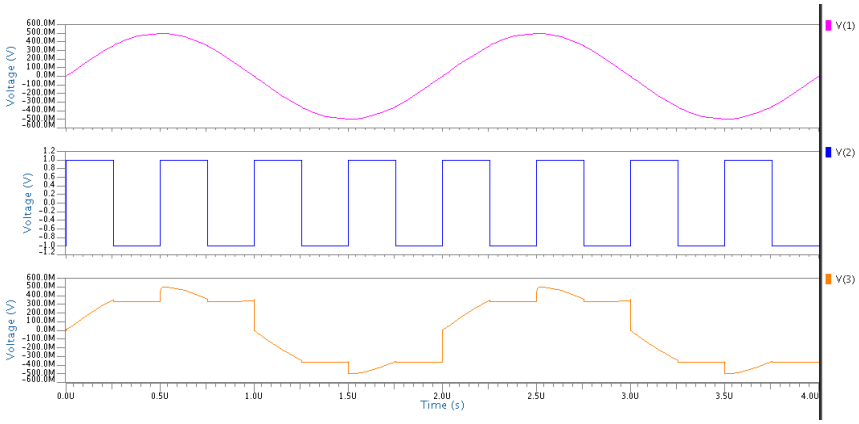
"Figure 3 on resistance of MOSFET switches [1]"

The sampling speed of MOSFET switch is depends on the on resistance of the switch and the value of the sampling capacitor. To accommodate higher voltage swing the on resistance of the switch should be low. Fig. 3 shows the on resistance of a PMOS, an NMOS and a CMOS transmission gate switch.

3.1 Simulation results



"Figure 4 Schematic of NMOSFET as a Switch"



"Figure 5 Transient Response of NMOSFET as a Switch"

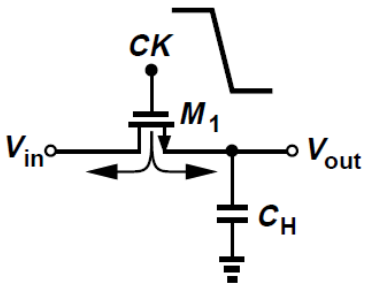
IV. NONIDEAL EFFECTS OF MOSFET SWITCHES

There are two non-ideal effects in MOSFET switches.

1. Charge sharing effect
2. Clock feed through effect

4.1 Charge sharing effect

Charge injection can be understood with the help of Fig.6. When the MOSFET switch is on and V_{DS} is small, some charge under the gate oxide resulted from the inverted channel. When the MOSFET turns off, this charge is injected onto the capacitor and into V_{in}. Since V_{in} is assumed to be a low-impedance, source-driven node, the injected charge has no effect on this node but the charge injected onto C_{load} results in a change in voltage across it.



"Figure 6 Charge Injection Effect in NMOS Switch [3]"

Consider the sampling circuit of Fig.6 and recall that for a MOSFET to be on, a channel must exist at the oxide-silicon interface. Assuming $V_{in} \cong V_{out}$, the total charge in the inversion layer as

$$Q_{ch} = W\ L\ C_{ox}\ (V_{DD} - V_{in} - V_{th}) \qquad (4.1)$$

where L denotes the effective channel length. When the switch turns off, Q_{ch} exits through the source and drain terminals, a phenomenon called "channel charge injection."

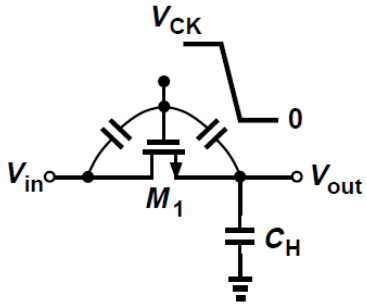
The charge injected to the left side on Fig.6 is absorbed by the input source, creating no error. On the other hand, the charge injected to the right side is deposited on C_H, introducing an error in the voltage stored on the capacitor. For example, if half of Q_{ch} is injected onto C_H, the resulting error equals

$$\Delta V = \frac{W L C_{ox}(V_{DD} - V_{in} - V_{th})}{2 C_H} \quad (4.2)$$

An important question that arises now is: why did we assume in arriving at that exactly *half* of the channel charge in injected onto C_H? In reality, the fraction of charge that exits through the source and drain terminals is a relatively complex function of various parameters such as the impedance seen at each terminal to ground and the transition time of the clock. Investigations of this effect have not yielded any rule of thumb that can predict the charge splitting in terms of such parameters. Furthermore, in many cases, these parameters, e.g., the clock transition time, are poorly controlled. Also, most circuit simulation programs model charge injection quite inaccurately. As a worst-case estimate, we can assume that the entire channel charge is injected onto the sampling capacitor.

4.2 Clock feed through effect

Clock feed through can be understood with the help of Fig.7. The capacitances between the gate/drain and gate/source of the MOSFET are modeled with the assumption that the MOSFET is operating in the triode region. When the gate clock signal goes high, the clock signal feeds through the gate/drain and gate/source capacitances. Now, as the switch turns on, the input signal, Vin is connected to the load capacitor through the NMOS switch. The result is that *C* load is charged to Vin and the capacitive feed through has no effect on the final value of V_{out}. When the clock signal makes the transition low, that is, the n-channel MOSFET turns off. A capacitive voltage divider exists between the gate-drain/gate-source capacitance and the load capacitance.



"Figure 7 Clock feed through Effect in NMOS Switch [3]"

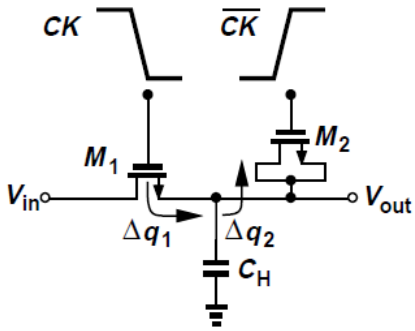
Assuming the overlap capacitance is constant, we express the error as

$$\Delta V = V_{CK} \frac{W C_{ov}}{W C_{ov} + C_H} \quad (4.3)$$

Where C_{ov} is the overlap capacitance per unit width. The error ΔV is independent of the input level, manifesting itself as a constant offset in the input/output characteristic. As with charge injection, clock feed through leads to a trade-off between speed and precision as well.

4.3 Charge Injection & Clock feed through Cancellation

The dependence of charge injection upon the input level and the trade-off expressed by $F = u_n/L^2$ make it necessary to seek methods of cancelling the effect of charge injection so as to achieve a higher F. To arrive at the first technique, we postulate that the charge injected by the main transistor can be *removed* by means of a second transistor.



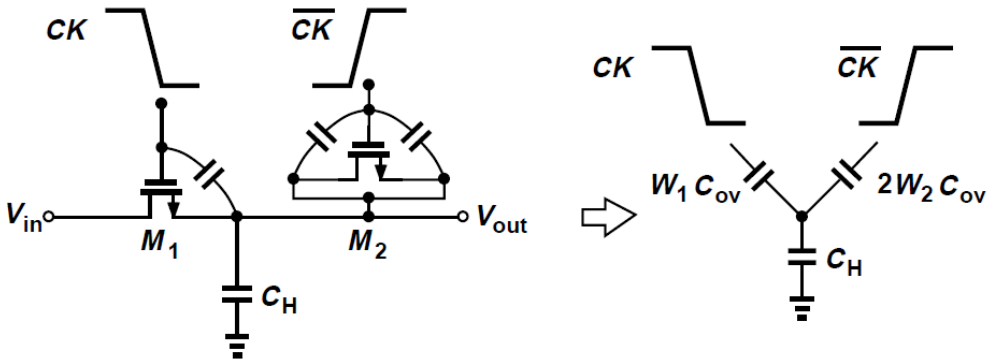
"Figure 8 Addition of dummy device to reduce charge injection and clock feed through [3]"

As shown in Fig.8, a "dummy" switch, M_2, driven by $\overline{CK}$ is added to the circuit such that after M_1 turns off and M_2 turns on, the channel charge deposited by the former on C_H is absorbed by the latter to create a channel. Note that both the source and drain of M_2 are connected to the output node.

How do we ensure that the charge injected by M_1, Δq_1, is equal to that absorbed by M_2, Δq_2? Suppose half of the channel charge of M_1 is injected onto C_H,

$$\Delta q_1 = \frac{W_1 L_1 C_{ox}}{2} (V_{CK} - V_{in} - V_{th1}) \quad (4.4)$$

Since $\Delta q_2 = W_2 L_2 C_{ox} (V_{CK} - V_{in} - V_{yh2})$, if we choose $W_2 = 0.5W_1$ and $L_2 = L_1$, then $\Delta q_2 = \Delta q_1$. Unfortunately, the assumption of equal splitting of charge between source and drain is generally invalid, making this approach less attractive.



"Figure 9 Clock feed through suppression by dummy switch [3]"

Interestingly, with the choice $W_2 = 0.5W_1$ and $L_2 = L_1$, the effect of clock feed through is suppressed. As depicted in Fig.9, the total charge in V_{out} is zero because

$$-V_{CK} \frac{W_1 C_{ov}}{W_1 C_{ov} + C_H + 2 W_2 C_{ov}} + V_{CK} \frac{2 W_2 C_{ov}}{W_1 C_{ov} + C_H + 2 W_2 C_{ov}} = 0 \quad (4.5)$$

V. PROS AND CONS OF SC CIRCUITS

The cons of switched capacitor circuits are as follows.

- MOSFET switches contribute non-ideal effects to the SC circuits.
- The MOSFET switch has non-zero voltage dependent on resistance which is not desirable.
- SC circuits have more stray capacitances as compare to conventional circuits.

Despite of these issues SC circuits are favorable because they have many advantages as well. Some pros of SC circuits are as summarized below.

- SC circuit can be used as a replacement of resistor in integrated circuits and it is easier to fabricate SC reliably with a small area and wide range of values as compare to resistor.
- Characteristics of SC circuit are determined by capacitance ratio.
- SC has the benefit of adjusting its value by changing the switching frequency.

REFERENCES

[1] R. Jacob Baker, Harry W. Li, David E. Boyce, "CMOS Circuit Design, Layout and Simulation," IEEE Press Series on Microelectronic Systems, 1997, pp.719-752.

[2] Phillip E. Allen , Douglas R. Holberg , "CMOS Analog Circuit Design ,"Oxford University Press, Second Edition, 2002, pp.492-600.

[3] Behzad Razavi, "Design of Analog CMOS Integrated circuit, "McGraw Hill Publication, 2001, pp.201-245,405-447.

[4] Mingliang Liu, "Demystifying Switched-Capacitor Circuits," Newnes, Elvister, 2006.

[5] Andrew Masami Abo, Design for Reliability of Low-voltage, Switched capacitor Circuits, Ph.D Dissertation, Dept. of Electrical Engineering and Computer Science, University of California, Berkeley (1999)5-8.

[6] Dr. William R. Grisé, Applications of Switched-Capacitor Circuits in Active Filters and Instrumentation Amplifiers, the Technology Interface, the Electronic Journal of Engineering and Technology, 3(1999).

