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Design of Pipelined ADC for High Speed Application

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Abstract — *This paper describes the implementation of a 8-bit 500 MS/s pipelined ADC using a conventional 0.18µm CMOS technology in Tanner EDA Tool. Two-stage OPAMP topology is used after Sample and hold block for improving the settling performance and in residue amplification. The supply voltage for this Pipelined ADC is 1.8 V. The simulation result shows speed of 0.5 GHz achieved with input frequency of 1 MHz and power dissipation of 169mW.*

Keywords- *Pipeline, High Speed, ADC*

I. INTRODUCTION

ADC is the key building block in today's high speed communication system and video system. With the development of these electronics systems, high resolution and high-speed ADC is becoming more important. High-speed low-power Analog-to-Digital converter (ADC) is the critical building blocks in modern communication and signal processing systems. It is the interface between the analog and digital signal processing. For signal processing, digital domain is preferred over analog because it has many advantages like noise immunity, storage capability, security etc. Due to these, today nearly all modern electronics are primarily digitally operated. As electronics and telecommunication moving fast towards digitalization and increasing demand on speed and accuracy to processed data, there is an increasing need for high speed and high resolution ADCs over recent years. Many good ADC architectures are available to satisfy different requirements in different applications. To name some: flash ADC, folding and interpolating ADC, two-step ADC, pipeline ADC, successive-approximation-register ADC, delta-sigma ADC, integrating ADC etc. Comparison of various ADC architectures are shown in Table 1 and its application based on resolution is also shown in Figure 1.

Among various available ADC architectures, the pipelined ADC has the feature of maintaining high accuracy at high conversion rate with low complexity and comparatively low power consumption. Therefore it is used extensively in high-quality video systems, high speed data acquisition systems and high performance digital communication systems where both precision and speed are critical.

Table 1. Comparison of various ADC[6]

Architecture	Latency	Speed	Accuracy	Area
Flash	No	High	Low	High
Folding/interpolating	No	Medium-High	Low-Medium	Medium-High
Delta-Sigma	Yes	Low	High	Medium
SAR	Yes	Low	Medium-High	Low
Pipeline	Yes	Medium	Medium-High	Medium

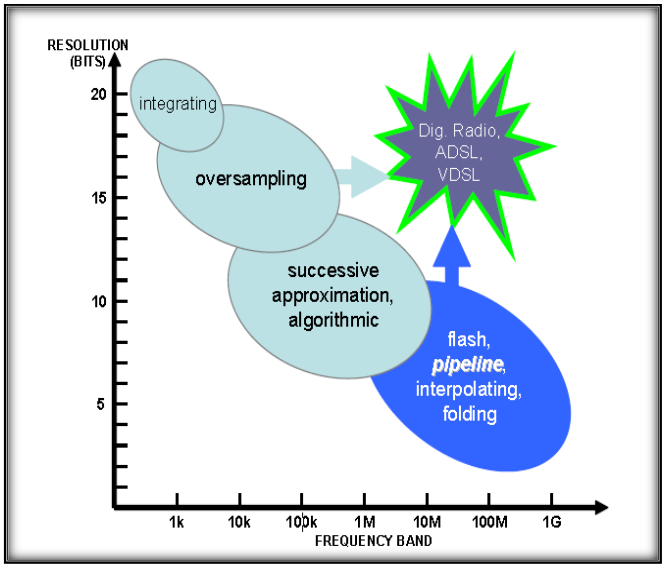

Figure 1. Various ADC architecture based on Application [7]

This paper is being divided into six sections. In section two, Generalized structure of pipelined ADC is introduced. In section three, different component of Pipelined ADC: Sample & hold , Comparator, 1-Bit DAC and OPAMP is implemented and simulation results are presented. In section four, summary of measurement result is done. In section five, conclusion has been discussed.

II. PIPLINED ADC ARCHITECTURE

Generalized structure of Pipelined ADC is shown in figure. It consisting of various cascade stage, In which each stage has a sample and hold (S/H) block, a sub-ADC (low resolution flash ADCs), a sub digital-to-analog converter (sub-DAC), a subtractor and an inter-stage gain amplifier. The operation of each stage has following step:

1. The sampled input signal is quantized by the sub-ADC to produce the output digital code for this stage.
2. Then the output digital code is converted back to an analog signal by the sub-DAC.
3. This quantized analog signal is subtracted from the input signal, resulting in a residue that is amplified and then passed onto the next stage.

This steps are repeated in each stage.

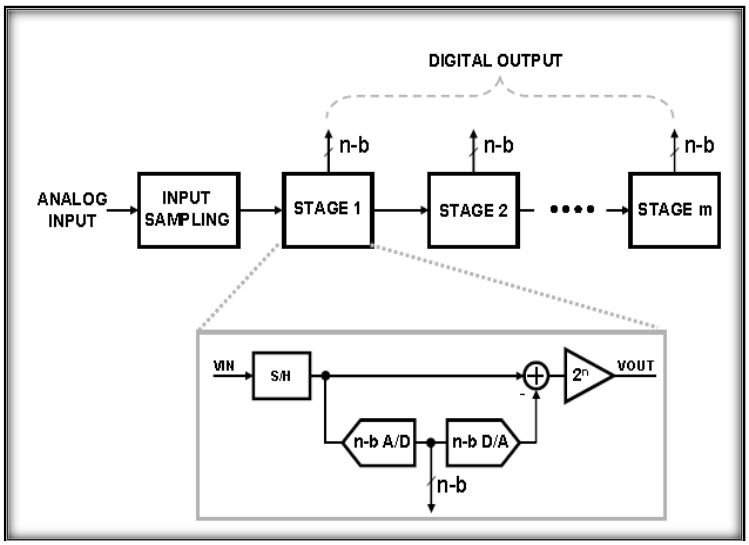

Figure 2. Generalized Structure of Pipeline ADC [3]

III. CIRCUIT IMPLEMENTATION

3.1. Sample and Hold Circuit

Sample & Hold circuit has been realized using a transmission gate and a capacitor as shown in figure 3.The operation of this circuit is as below.
Whenever Clk is high, the Transmission Gate turn On, which in turn allows V_{OUT} to track V_{IN}. When Clk goes to logic low, the Transmission Gate turn Off. During this time, C_s will keep V_{OUT} equal to V_{IN} at the instance when Clk goes low. Transient simulation of sample and hold is shown in figure 4.

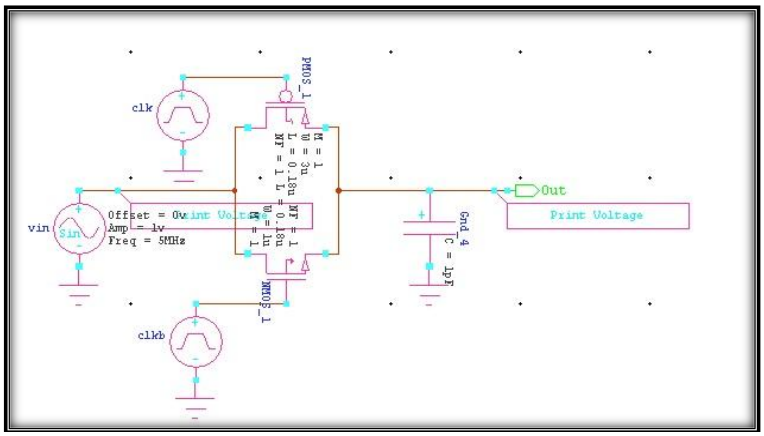

Figure 3. **S/H circuit using TG[4]**

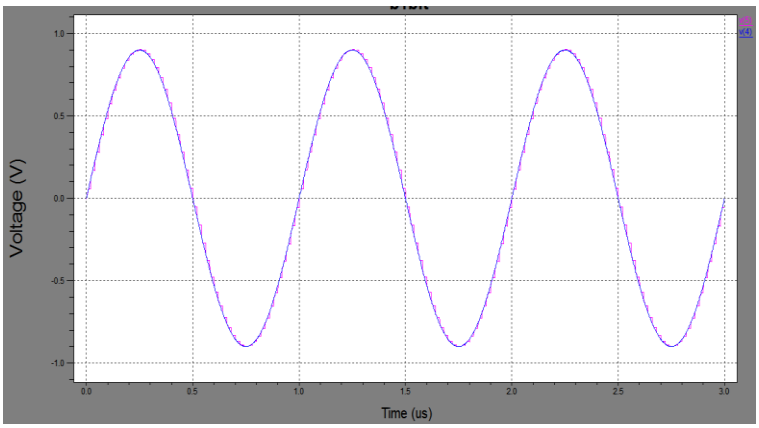

Figure 4. **Transient simulation of Sample and Hold**

3.2. Comparator:

The Pipelined ADC consists of a 1-bit ADC which can be implemented using comparator. Here two stage open loop OPAMP is used as a comparator. The design of comparator is similar to the design of an Op-amp .The only difference between both is to the use of the compensation network. Comparator does not need any type of compensation network because its function is to switching from Positive rail to Negative rail. When a sine wave is input to the circuit, the comparator switches from rail to rail. Implementation of comparator and simulation result of comparator is shown in Figure 5 & 6 respectively.

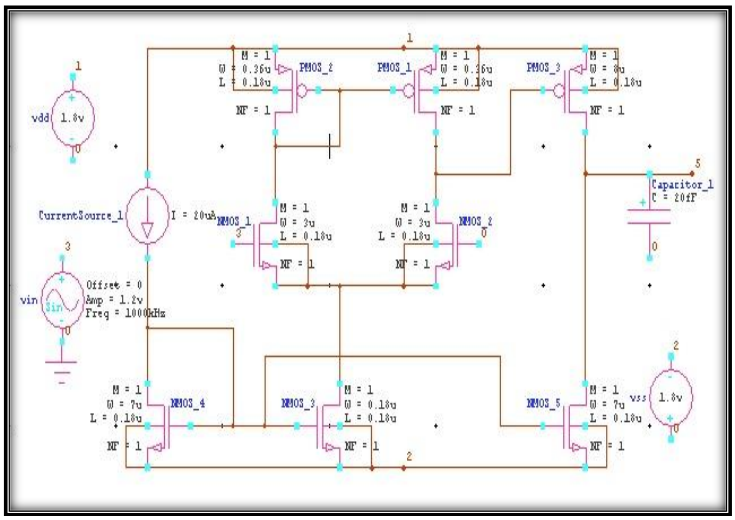

Figure 5. Design of Comparator[2]

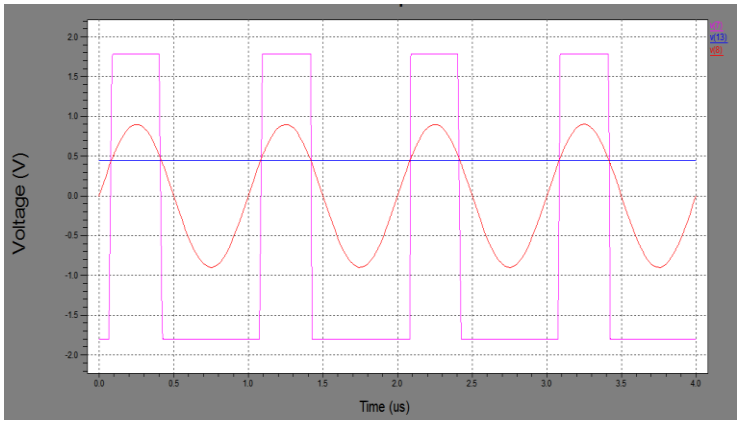

Figure 6. Transient simulation of comparator

3.3. 1-Bit DAC:

This 1- Bit DAC converts the 1-bit digital to an analog signal and fed back to the subtractor as shown in the block diagram of pipeline ADC of Figure 2. Figure 7 shows the circuit level diagram of 1-bit DAC. It has been implemented with the help of two TG. As the number of bits is only 1-bit, the respective analog output will also have two levels and similar to that of digital output. Therefore 1-bit DAC has two reference voltages as shown in Figure 7, a positive reference voltage of $+V_{REF}$ and a negative reference voltage of $-V_{REF}$.
Here in implementation of 1-bit DAC, the multiplexer has to select V_{REF} or 0 depending on the output of the comparator which acts like a selection line.

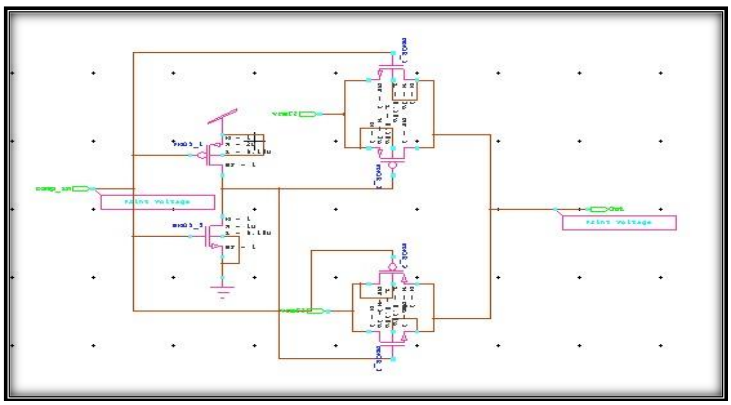

Figure 7. DAC using TG[5]

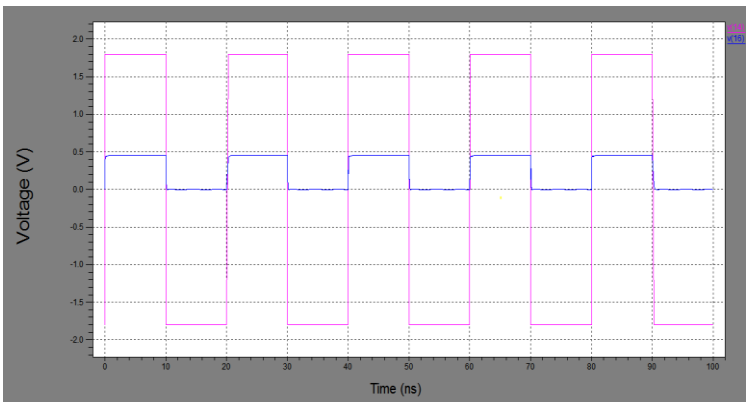

Figure 8. Transient Simulation of DAC

3.4. OPAMP:

Operational amplifier is an integral part of many analog and mixed and mixed-signal systems. Operational Amplifier is defined as high gain differential amplifier. Since OPAMP is usually employed to implement a feedback system, there open loop gain is chosen according to the precision required of the closed-loop circuit. An ideal OPAMP has infinite differential voltage gain, infinite input resistance, and zero output resistance. Different topologies are used based on the requirement. Here in this paper used two stage OPAMP as shown in figure 9.Use of opamp in Pipeline ADC design is for generation of residue voltage and for residue amplification as per the operation of Pipeline ADC. The frequency response of used OPAMP is shown in figure 10.With the use of this OPAMP gain and phase margin achieved is 52.90dB and 53.58 degree respectively.

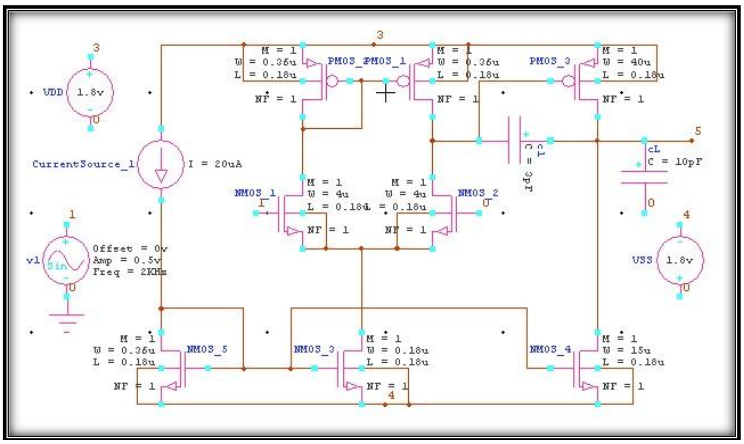

Figure 9. Two Stage OPAMP circuit [2]

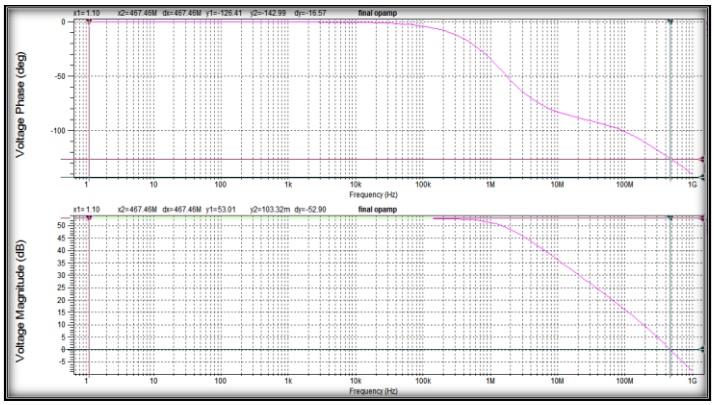

Figure 10. Frequency Response of Two Stage OPAMP

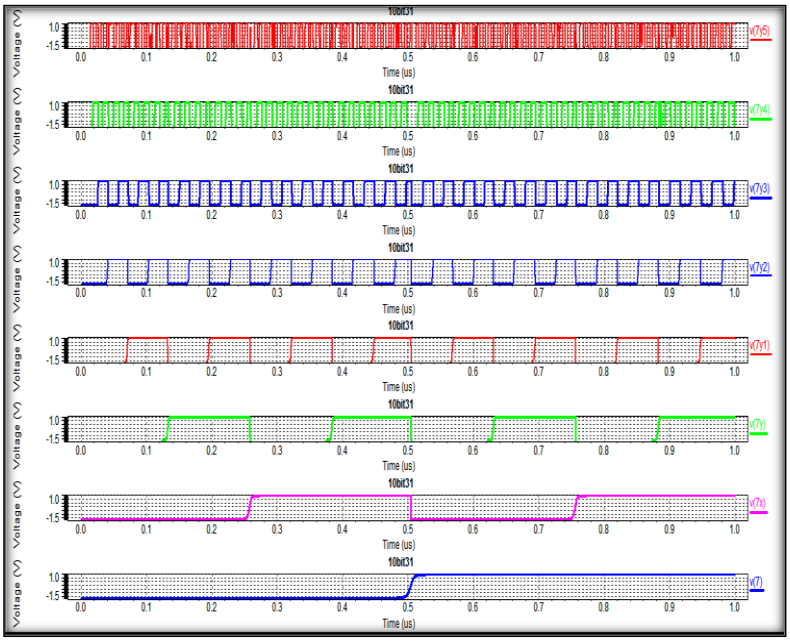

Figure 10: 8 bit Digital output of Pipelined ADC for Ramp input

IV. SUMMARY OF SIMMULATION RESULTS

Table 2. Summary of ADC Simulation Result

Parameter	Value
Technology	0.18µm
Supply voltage	1.8V
Samples	500MS/s
Input Frequency	1MHz
Resolution	8 bit
Conversion Speed	0.5GHz
Power dissipation	169mW

V. CONCLUSION

In this paper, pipelined ADC with front-end of the S/H and the MDAC is proposed. With the use of Two Stage OPAMP in Sample and hold and in Residue Amplification settling performance is improved. From the Table II, Speed achieved is 0.5GHz with input frequency of 1MHz.The ADC consumes 169mw power under power supply voltage of 1.8V.

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