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A REVIEW ON TWO-STAGE CMOS OPERATIONAL AMPLIFIER USING FREQUENCY COMPENSATION TECHNIQUES

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Abstract — *An Operational Amplifier is a direct-coupled high-gain amplifier usually consisting of one or more differential amplifiers followed by a level transistor and output stage. The op-amp has become one of the most versatile and important building blocks in analog circuit design. In this paper, we are presenting a review on CMOS two stage op-amp using frequency compensation techniques. Two –stage CMOS op-amp design procedure involve that first stage is differential amplifier, second stage is common source amplifier and final stage is output buffer. There are introduce various frequency compensation techniques like miller compensation, resistor nulling, parallel compensation, voltage buffer, current buffer. In this paper, we are presenting the relation between frequency dependent parameter like slew rate, phase margin, compensation capacitor, bandwidth, gain bandwidth product and stability.*

Keywords- *Two-Stage CMOS Op-Amp, Frequency Compensation Techniques, Stability, Gain-Bandwidth Product, Slew Rate, Phase Margin.*

I. INTRODUCTION

Design of high performance of analog integrated circuit is becoming most versatile and essential with the continuous trades toward the reduce power supply voltage and transistor channel length.MOS transistor is most success than bipolar transistor because it can be scaled down to smaller dimension and higher performance. Due to scaling down to transistor size, it most advantage is we can integrate more number of transistors on the same size and we can get faster amplifier than previous one. This leads to continuous growth of the processing capacity per chip and operating frequency. In most electronics circuit, operational amplifier is the most common building block for any analog mixed signal system. Due to reducing transistor channel length and power supply, design of op-amp face continuous challenge. There is tradeoff among speed, power and gain and other parameter because of different W/L ratio. In analog CMOS circuit, single stage CMOS op-amp like differential amplifier has lower gain and improve gain we can use another cascading stage is common source amplifier. Two-stage CMOS op-amp names that it's contain 'TWO GAIN STAGE' so that overall output voltage gain is increase. The implementation of CMOS two-stage op-amp is face the problem of stability due to contain two pole and one zero and DC gain with higher unity gain frequency has been more difficult problem. There have been several techniques to propose to evaluate this problem. The purpose of the design methodology in this paper is propose accurate equation for the design of two-stage CMOS op-amp.

We formulate CMOS op-amp design problem and their aspects ratios. In this paper, we present frequency compensation techniques can be apply wide verity of amplifier structure, but in this review paper we apply the method to specific two-stage CMOS op-amp. The variation in the performance of CMOS op-amp with variation of width, length and value of compensation capacitor is discussed.

II. BLOCK DIAGRAM OF TWO-STAGE CMOS OP-AMP

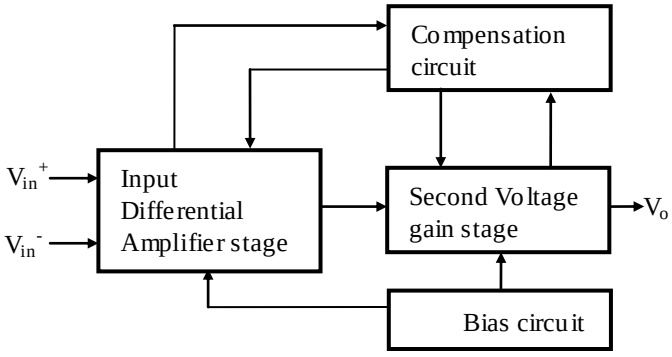

Fig.1 Block diagram of two-stage CMOS Op-Amp [1]

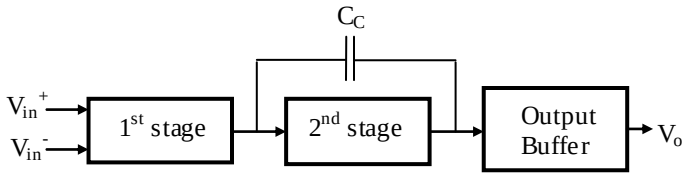

Fig.2 Simplified block diagram of two-stage CMOS Op-Amp [1]

General block diagram of two-stage CMOS op-amp is shown in Fig. [1] and simplified block diagram with output buffer in Fig. [2]. The topology of this circuit is that of a standard two- stage CMOS op-amp. It has three subparts, namely input differential amplifier stage, second gain stage and biasing circuit. The gain of these topologies is limited by the product of the input pair transconductance and the output impedance. In cascode circuit, its provide high gain while limiting the output swing [10].

The first block is a differential amplifier. It has two inputs that are the inverting and non-inverting voltage. It gives a differential voltage at the output or a differential current which depends only on differential input voltage. The second block is a differential ended to single-ended converter. It is used to transform the differential signal generated by the first block into a single ended output signal. In single stage amplifier, the gain provided by the input stages is not sufficient, so there is an additional amplification is required which is provided by the second stage, i.e. the common source amplifier, driven by the first stage output. As this stage uses differential input unbalanced output differential amplifier, so it provides the required extra gain. The biasing circuit is here to provide the proper operating point to each transistor in its saturation region. Third stage, the output buffer stage provides the low impedance at output and larger output current needed to drive the load of op-amp or improves the slew rate. Compensation capacitor is included to ensure stability when op-amp is used with feedback. Because C_C is place between input and output of the second common source stage, so it is called Miller capacitance.

III. CIRCUIT DIAGRAM OF TWO-STAGE CMOS OP-AMP

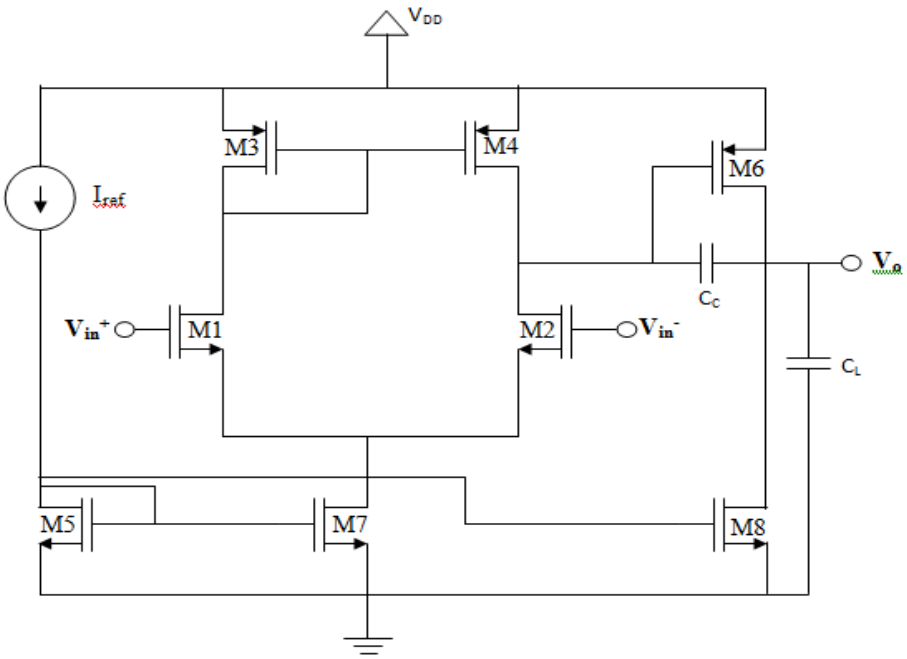

Fig.3: Two-Stage CMOS Operation Amplifier [1]

A. First stage:

It contains two part of two-stage op-amp. Transistor M1, M2, M3, and M4 constitute the first stage of differential amplifier. M1 and M2 transistors are nMOS. M3 and M4 transistors are pMOS transistor. Input voltage Vin+ and Vin- are given to gate terminal of transistor M1 and M2. Gate of M1 is noninverting input and gate of M2 is inverting input. M3 and M4 constitute current mirror. A differential input signal is applied across the two input terminals will be amplified according to the gain of the differential stage. So that gain of this stage is the transconductance of M1 times to the total output resistance seen at the drain of M4. The main resistances that constitute to the output resistance are that of the input transistors and output resistance of the load transistors M3 and M4.

In this circuit, current mirror active load used has three main advantages. First, active load devices crate large output resistance that provides small amount of chip area. Second current mirror topology provides the differential to single ended conversion of input signal.

$$A_{V1} = -g_{m1} \times (r_{o4} \| r_{o2}) \quad \ldots\ldots(1)$$

The differential to single ended conversion is achieved by using current mirror M3 and M4. The current from M1 is mirror by M3 and M4 and subtracted from the current from M2. Finally the differential current from M1 and M2 multiplied by the output resistance of the input stage that gives the single ended output voltage. This is the part of the second stage.

B. Second stage:

Second stage is a common source stage. The aim of this second stage is to provide the additional gain consisting of transistors M6 and M8. Input of the second stage is the output of the differential amplifier stage. This stage receives the output from the drain of M4 and amplifies it through M6 by the common source configuration. Similar to differential amplifier, this stage employs an active device, M8 to work as the load resistance for M6. The gain of this stage is the transconductance of M6 times the effective load resistance comprised of the output resistance of M6 and M8. Transconductance and output resistance of the second stage is given by G_{m2} and R_{out}

$$A_{V2} = -g_{m6} \times (r_{o6} \| r_{o8}) \quad \ldots\ldots(2)$$

Therefore, overall voltage gain is given by $A = g_{m1} \times g_{m6} (r_{o4} \| r_{o2}) \times (r_{o6} \| r_{o8})$ ……..(3)

C. Output buffer:

Third stage is output buffer stage which is simply common drain stage. This stage is often called a source follower, because the source voltage follows the gate voltage, except for a level shift. When possible, it is desirable to tie the substrate of the source-follower device to its source in order to eliminate gain degradations due to the body effect. This connection also results in a smaller dc voltage drop from the gate to the source of the source-follower device, which is a major limitation on the maximum positive output voltage. So that in fig 5.3, we don't show output buffer stage due above drawback.

D. Biasing circuit:

The purpose of the biasing circuit is to provide the gate to source voltage of the entire transistor. The biasing of the operational amplifier is achieved with only three transistors. Transistor M5 supplies a voltage between gate and source of M7 and M8. Transistors M7 and M8 sink a certain amount of current based on their gate to source voltage which is controlled by the bias string. M5 is diode connected to ensure they operate in the saturation region. Proper biasing of the other transistor in the circuit (M1-M4, M6) is controlled by the node voltages present in the circuit itself. M6 is biased by the gate to source voltage set up by the V_{GS} of the current mirror load as are the M3 and M4 transistors

IV. FREQUENCY COMPENSATION TECHNIQUES

Frequency compensation is a techniques used in amplifier circuit. It has two primary goals: to avoid unintentional creation of positive feedback which will cause to oscillate amplifier and to control overshoot and ringing in amplifier step response [11]. Gain of the single stage does not suffice, so that one must add extra stage to the circuit, the issues of frequency compensation arises.

4.1. Parallel compensation

Two-stage CMOS op-amp has two dominating pole; $P_1=1/r_{p2}*c_{p1}$ and $P_2=-1/r_1c_1$ ……..(4)
So circuit need of compensation. Inserting series combination of R_c and C_c between two transistors so that reduced midband gain of amplifier and transform frequency response into 1st order characteristics as shown in figure. Inserting of resistor and capacitor introduces two addition poles P_{c1}, P_{c2} and two addition zero Z_{c1}, z_{c2}.

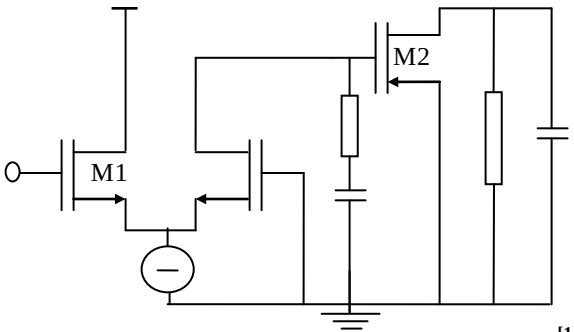

Fig.4: Two-stage op-amp using parallel compensation [11]

Two-stage CMOS op-amp has two dominating pole;

$P_1=1/r_{p2}*c_{p1}$ .....(5)

$P_2=-1/r_1c_1$ .....(6)

So circuit need of compensation. Inserting series combination of R_c and C_c between two transistors so that reduced midband gain of amplifier and transform frequency response into 1st order characteristics as shown in figure. Inserting of resistor and capacitor introduces two addition poles P_{c1}, P_{c2} and two addition zero Z_{c1}, z_{c2}.

Location of pole approximately is $P_{c1}=-1/r_{p2}C_c$ and $P_{c2}=-1/R_cC_c$..... (7)

While zero follow from $Zc1=-1/r_{p2}C_{p2}$ and $Zc2=-1/R_cC_c$..... (8)

4.2 Pole splitting compensation*;*

I. Single capacitor miller compensation

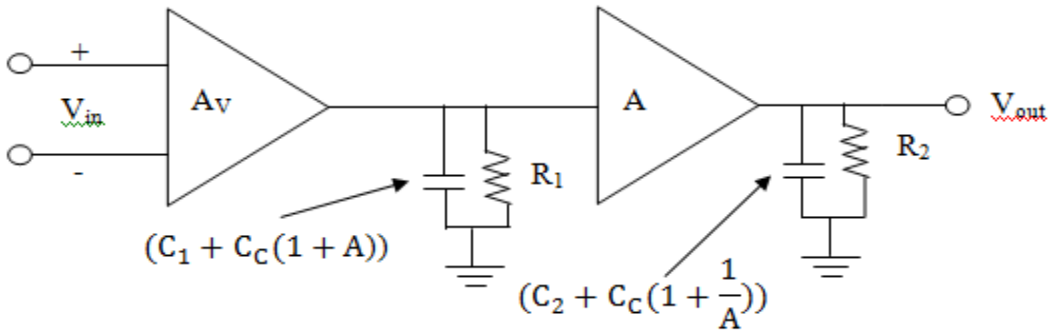

Fig.4: Two-stage op-amp using parallel compensation [11]

For a two-stage CMOS Operational amplifier, single capacitor miller compensation which reduce frequency of dominant pole and move output pole away from the origin this effect is called pole splitting. In this method compensation capacitor is connected in second stage. Miller theorem states that impedance seen in parallel with the gain stage that can be modeled as impedance connected from the input of that gain stage to the ground and impedance connecting from the output of that gain stage to the ground. Impedance is purely capacitive and second stage has inverting gain Before the implementation of pole-splitting, the first and second stage has pole frequencies, Where R1, C1 are the output resistance and capacitance of first stage and R2, C2 are the output resistance and capacitance of second stage. Due to reduce frequency of the first stage, op-amp's phase margin improves that makes op-amp more stable than before compensation. In term of stability, one of the trades of is bandwidth. If the first stage bandwidth is reduced, the overall bandwidth will be reduced. While designing the op-amp with cascade topology, the zeroes quite far from the origin, in two-stage op-amps with miller compensation, As poles in left half plane, zero in the right half plan contribute more phase shift moving the phase crossover toward the origin. It is two effects which are to eliminating the effect of the right half-plan zero. One approach has been to insert a source follower in the path from the output back through the compensation capacitor. And second is to insert a nulling resistor in series with the compensation capacitor

. Before the implementation of pole-splitting, the first and second stage has pole frequencies,

$$\omega_1 = \frac{1}{R_1C_1} \quad \text{and} \quad \omega_2 = \frac{1}{R_2C_2} \qquad \text{.....(9)}$$

After compensation, these frequency become

$$\omega_1 = \frac{1}{R_1(C_1 + C_C(1 + A))} \quad \text{and} \quad \omega_1 = \frac{1}{R_2(C_2 + C_C(1 + \frac{1}{A}))} \qquad \text{.....(10)}$$

II. Single capacitor miller compensation with resistor nulling

We can move the zero so as to cancel the first nondominant pole. This occur if the value of nulling resistor in chosen such that the frequency of zero is same as that of the first nondominant pole. The possibility of canceling the nondominant pole makes this technique quite attractive. To remove the RHP zero, Miller capacitor with a nulling resistor in series is used as shown in Fig . The equation of the zero becomes

$$Z_1 = \frac{1}{C_C(\frac{1}{g_{m6}} - R_M)} \quad \text{.....(11)}$$

If the value of the resistor R_M is equal to $1/g_{m6}$, miller resistor, where g_{m6} is transconductance of second stage, then the zero moves to infinity. If RM increases, beyond a value of $1/g_{m6}$, then the RHP zero moves to the LHP, which can be used to improve the phase margin and increase stability.

III. Voltage buffer

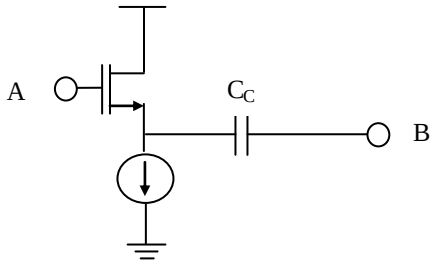

Fig.5: Voltage buffer compensation [10]

Ideal voltage buffer with zero resistance to compensate the right half plane zero. Simple common drain techniques is employed and connected node A and node B. Finite output resistance of the voltage buffer which is equal to $1/g_m$, compensation branch introduces a left half plane zero at

$$f_z = g_{m6}/2\pi C_C \quad \text{.....(12)}$$

This compensation shows high accuracy since it only depends on matching tolerances between transconductance and capacitor. Compensation techniques based on nulling resistor and voltage buffer gives same compensation capacitor and same gain-bandwidth product

IV. Current buffer(common gate transistor)

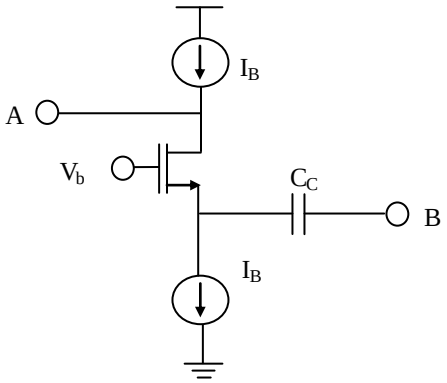

Fig.6: Current buffer Compensation [10]

Compensation based on current buffer (common gate transistor) shown in figure. This approach is very efficient for gain-bandwidth product and PSRR performance. In these techniques minimum allowable values of C_C is smaller. Smaller C_C is provides higher degree of freedom in trading noise performance with power consumption.

TABLE 1. SURVEY OF VARIOUS PARAMETERS OF TWO-STAGE CMOS OPERATIONAL AMPLIFIER

Op-amp parameter	Reference paper							
	[1]	[2]	[3]	[4]	[5]	[6]	[7]	[8]
Supply voltage(V)	2.5	1.2	1.5	1.2	0.9	2.5	1.8	1.8
CMOS technology	2µm	0.13µm	0.18µm	0.13µm	0.18µm	0.18µm	0.18µm	0.15µm
DC Gain (dB)	96	54.89	92.5	85.93	94	36.747	66	59.53
Slew Rate (V/µs)	10	5.82	16.75	44.29	200	12.5	-	185
UBG(MHz)	4.416	32.59	236	55	549	16.54	100	504.9
Phase margin (Degree)	70	-	81.3	-	68	48.1	57	60.65
Output swing (V)	1-2.4	-	1.26	1.1	-	-	-	-
CMRR(dB)	-	-	-	61	-	133.69	75	-

V. CONCLUSION

This paper described basic two-stage CMOS operational amplifier employing first stage as differential input amplifier and second stage as common source amplifier. Compare to single stage amplifier, two-stage CMOS amplifier is higher gain and high output swing. For low power application and analysis of frequency dependant parameter like slew rate, gain bandwidth product, unity gain bandwidth, phase margin and stability analysis, frequency compensation techniques introduced. Compensation based current buffer has high GBW, improved slew rate, increase output swing and area efficient for low C_C value.

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