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Low Power Folding and Interpolating Analog to Digital Converter using 180nm Technology

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Abstract— Folding and interpolating A/D converters have been shown to be an effective means of digitization of high bandwidth signals at intermediate resolution. The paper focuses on design of 5-bit folding & interpolating ADC. The converter architecture is designed with reduced number of comparators and minimum hardware. The folding amplifier with folding factor=4 can be used to produce more than one zero-crossing point to reduce required number of comparators. To achieve the design goal, folding amplifier is used in the design of coarse and fine converter both. To reduce the power consumption, encoder based on XOR-OR logic is used. The design is implemented using 0.18µm technology at 1.8Vsupply voltage.

Keywords- Folding amplifier, Interpolation, Comparator, Digital Encoder, Fine ADC, Coarse ADC

I. INTRODUCTION

Analog-to-digital converters have been incorporated into most of the complex mixed signal systems. However, low-voltage and low- power constraints often have to be met in these systems, particularly for battery-powered portable devices. Full flash and multi-step flash ADCs are the well-known architectures for a high-speed analog to digital conversion [1]. However, these architectures require large power dissipation. When the need for a relatively high conversion rate and medium resolution dominates, folding and interpolating architecture exhibits a good performance. For instance, this architecture has been employed to design a 5-bit folding and interpolating ADC using a 0.18um CMOS technology. The high-speed and low-power constraints can also be met with folding and interpolation techniques. However, with this architecture, it is difficult to achieve a high resolution (e.g., 6-bit) due to the limitation in folding factor. In this paper a low-power, 1.8V four-level folder is designed. This is used to design a low- power, 1.8V folding and interpolation ADC with 5-bit resolution. Thirty two-level folding signal is achieved by such four folding amplifier having folding factor=4. Addition intermediate signals are generated using resistive interpolation technique with interpolation rate=2. After analog preprocessing, one comparator deals with more quantization levels. Hence, the number of the comparators is reduced. The number of comparators required for a folding ADC decreases as the folding order increases. The architecture still keeps high speed conversion feature.

Section-II discusses the proposed architecture of folding and interpolating ADC. The details of novel low voltage, low power folding amplifier is shown in section-III. Section-IV discuses resistive interpolation technique. The high speed low power comparator and encoder design are described in section-V. Finally, the conclusion is presented in Section V.

II. ARCHITECTURE OF FOLDING & INTERPOLATING ADC

The concept of Folding A/D converter was first introduced by Arbel and Kurz [9] in 1975. The main motivation was the dramatic reduction of the number of comparators required in the design. Fig. 1 shows the block diagram of a folding A/D converter. The folding and interpolating A/D converter contains two separate converters, namely, the coarse and the fine converter. The input signal is fed into both converters in parallel. The input voltage is applied to a pre-processing circuit depicted as the "folding circuit," and the output of this folding circuit is connected to a N-n-bits fine A/D converter. The input signal is also directly connected to a n-bits coarse A/D converter.

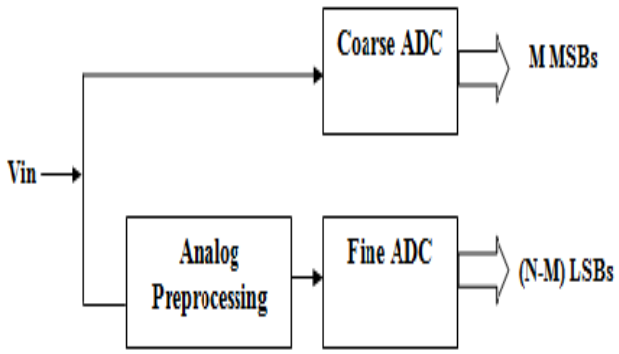

Figure 1 Block Diagram of folding ADC

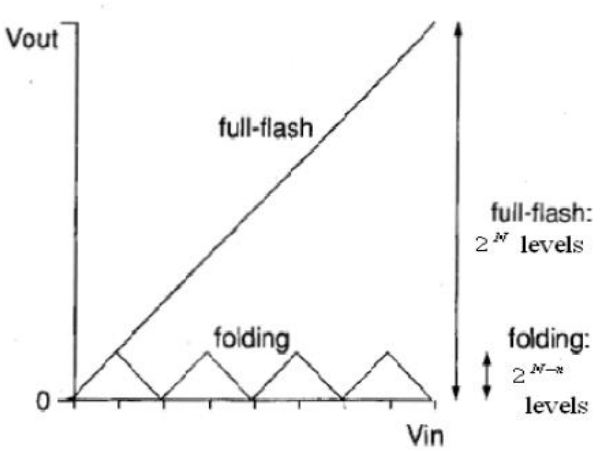

Figure 2 Transfer curve of folding circuit in comparison with transfer curve of full flash ADC

The operation of the folding circuit is illustrated in figure 2, where the transfer function of the folding circuit is given. The input-output characteristics of folding circuit can be parameterized by number of folds. This parameter determines resolution of both coarse and fine ADC. Lower folding factors require more fine comparators, while higher folding factors result in, amongst other things, more pre-processing hardware. The "zig-zag" shaped transfer curve covers the whole *Vin* range, and the output voltage of the folding circuit needs to be converted to only $2^N - n$ levels corresponding to the least significant bits (LSB's) of the A/D converter output code.

In order to distinguish the n possible input voltages, the n-bit coarse A/D converter is required, which generates the n most significant bits (MSB's) of the A/D converter. The total comparator count for this folding converter is 2^{N-n} (fine) + 2^n (coarse), which is much less than the 2^N required for a full flash. Also the n most significant bits and the N-n least significant bits are generated synchronously, and thus, a sample and hold function is basically not required. The throughput of a folding A/D converter is equal to that of a full-flash, while a two or multi-step converter requires several clock cycles to convert the data. Interpolation further reduces the number of preamplifiers.

Due to the folding characteristic, if the input goes from zero to full scale once, the output goes from *Vin* to *Vmax*, *F* times. The input signal frequency is multiplied in the analog pre-processing of the A/D converter as a result of the folding operation. The maximum frequency multiplication in a folding system is determined by the folding factor of the A/D converter. A high folding factor results in fewer comparators, but it lowers the maximum input signal frequency of the A/D converter. The non-linearity errors in the folding characteristic also depend on the frequency of operation. At high speeds, the rate of the change of the signal becomes comparable with the intrinsic time-constants of the circuit. The input-output characteristic tends to be rounded at the folding point and hence the non-linearity increases. The non-linearity falls to zero at zero crossing points. Thus, if only these points are considered, the polarity of the difference between input voltage and reference voltage can be determined correctly.

An ADC employing folding technique can produce more zero crossing points than flash ones, thus reducing the number of comparators, power consumption and chip area. Also the interpolation

technique can produce more than one signal thus reducing the number of folding amplifier and circuit complexity. The LSBs number of zero crossing points is determined by following equation.

$$Z = N_F * FF * I \quad \text{..... (1)}$$

Where N_F is the number of primarily folding waveform, F_F is the folding factor and I is the interpolation rate.

The choice of folding factor F_F and the number of folding block N_F play very important role in design of folding and interpolating ADC. The speed and bandwidth of the ADC are affected by the bandwidth of the folding circuits. Moreover, the accuracy of the ADC is dominate by the folding circuits in which the correct zero crossing points must be generated to meet the required resolution. Here, zero crossing points are generated to achieve high speed, accuracy and low power operation. The folding amplifier is designed using0.18um technology, 1.8V supply voltage with folding factor F_F=4. Further, parallel folding saves the number of comparators. The number of folding block N_F is selected four. The interpolation factor I=2 is chosen for the design.

Figure 3 shows block diagram of implemented 5-bits folding & interpolating converter. The reference voltages and input signal are applied to the fine and coarse converter through folding block. The differential signals are applied to comparators. The output of comparators is cyclic thermometer code. Finally encoder converts cyclic thermometer code into binary code.

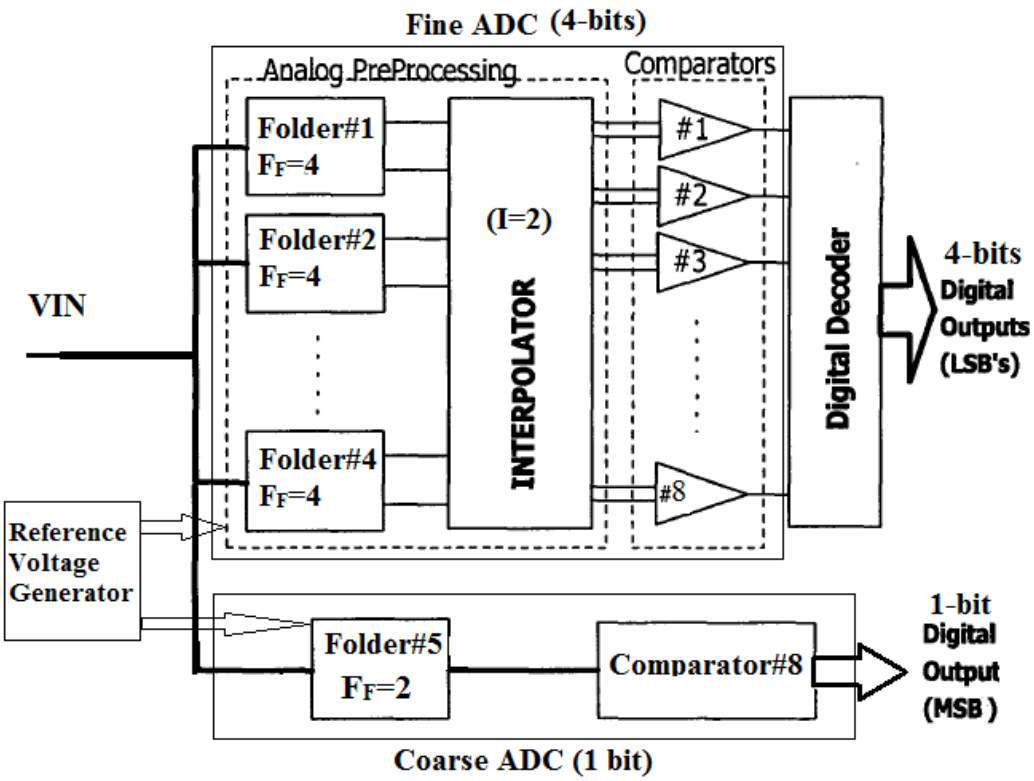

Figure 3 Architecture of 5-bit folding & interpolating ADC

III. Folding Amplifier

Voltage mode folding amplifier is based on differential pairs. To implement folding amplifier with folding factor of N, N differential pairs and N tail current sources are required. A typical voltage mode folding amplifier is shown in figure 3. The zero-crossing points are determined by reference voltage Vref. Figure 3 shows folding amplifier with folding factor=4. It requires four cross-coupled differential amplifiers with tail current sources I1…. I4. Vr1…Vr4 indicates various reference voltages. The inputs of the differential pairs are connected to the converter input voltage Vin and reference voltages Vr1…Vr4 Because of cross coupling in the differential amplifier, two of tail currents are switched to the load resistor R1 and other two are switched to R2. Depending on the input

signal level with respect to the reference level the currents switched to the load resistor change. The outputs of adjacent stages are added with opposite polarity. The resistive ladder is used to generate a set of reference voltages for folding amplifier. The amplifier whose reference voltage is close to the input voltage is "active", while the two amplifiers not close to a crossing point are saturated. The basic function performed by the folding amplifiers is the conversion of the increasing (or decreasing) input signal into a number of sinusoidal output signals. In some of the cases, dummy differential pair is used for proper dc current balance. [6]

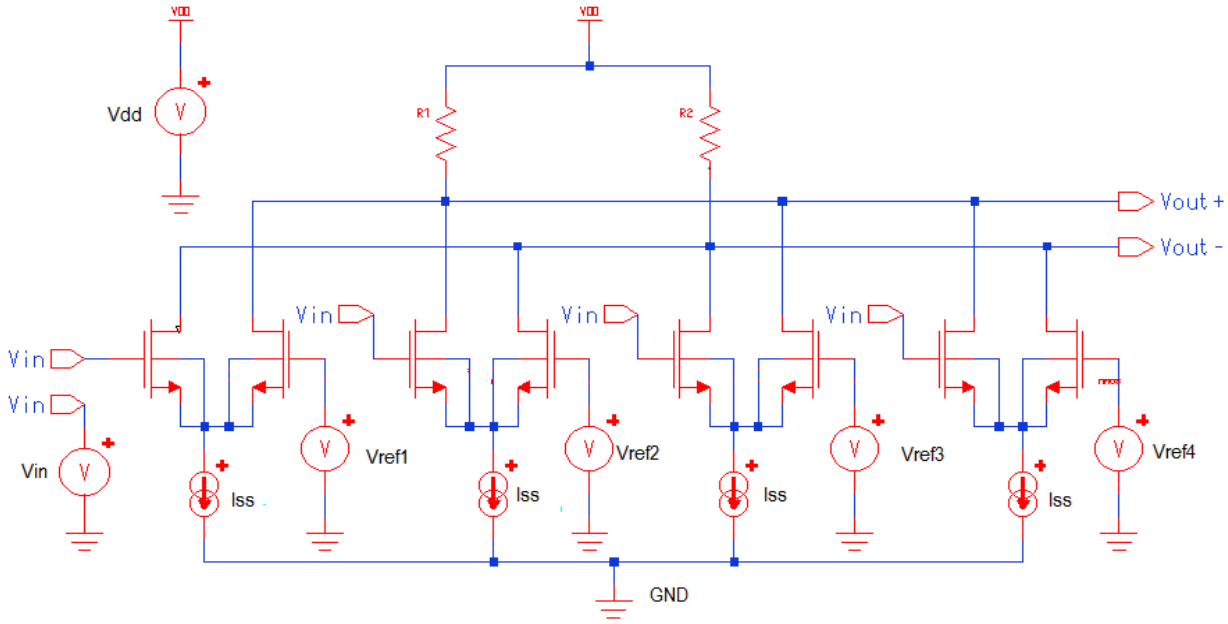

Figure 4 Folding amplifier with folding factor=4 **[6]**

The simulation results are obtained using 0.18um CMOS technology at 1.8V. Figure 4 shows dc response of folding amplifier with folding factor = 4. The reference voltages are Vref1=0.35V, Vref2=0.7V, Vref3=1.05V, Vref1=1.4V.

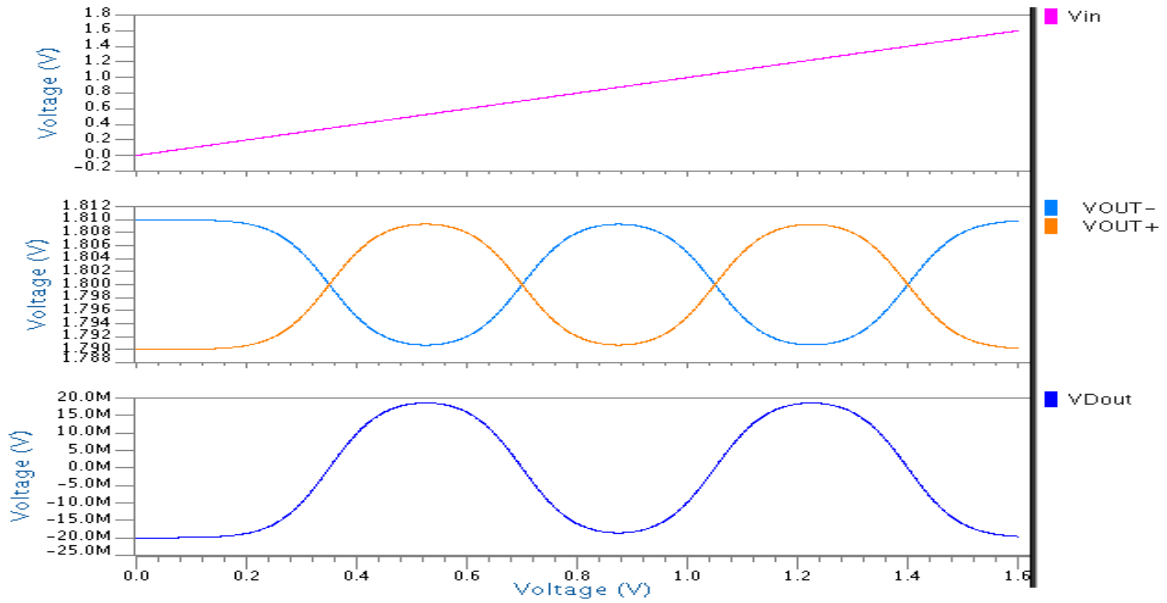

Figure 5 DC Simulation Results of Folding Amplifier using 0.18um technology (Vin 1.6V)

Figure 6 shows DC simulation results with sixteen zero crossing points, which are determined by reference voltage levels. The design can be combined to increase number of zero crossing points

without increasing number of folding amplifiers using interpolation technique. The sixteen reference voltages are generated through active divider to reduce static power dissipation.

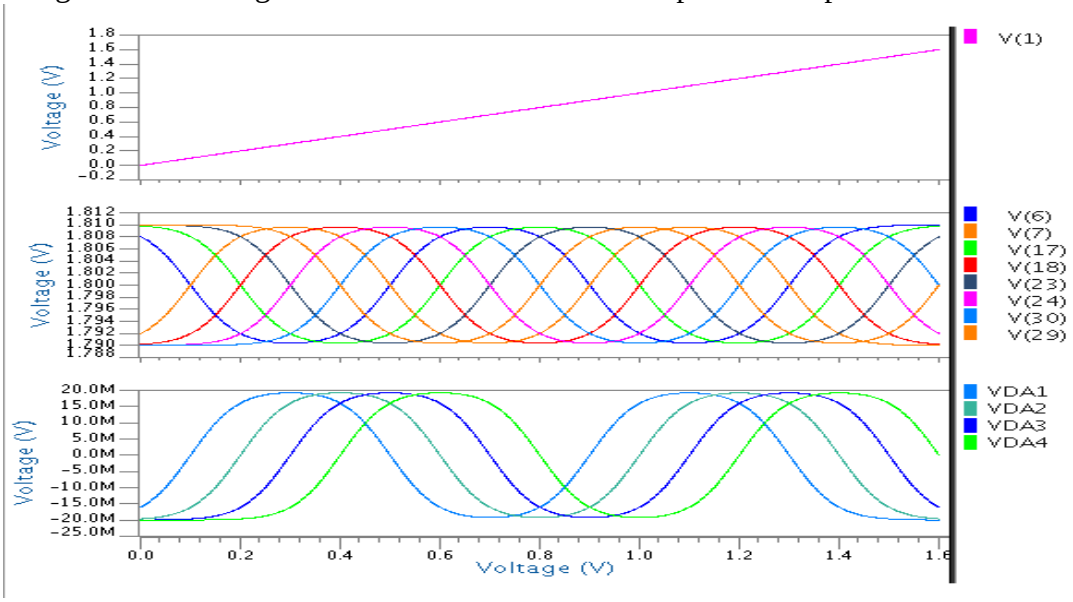

Figure 6 Generated Sixteen Zero Crossing points using four parallel folding amplifiers

IV. RESISTIVE INTERPOLATION

Interpolation is often employed to generate extra folding waveforms without increasing number of folding amplifiers. There are basically two methods to interpolate the folded signals, namely voltage-mode (resistive) interpolation and current-mode interpolation. The current-mode interpolation is based on summation of currents reflected through current mirrors with different ratios. However this method is complex proves to be power hungry and not very precise due to the non-idealities of the current mirrors. For these reasons resistive interpolation is preferred. The voltage-mode (resistive) interpolation can be implemented using a resistance ladder.

The advantage of a voltage-mode interpolation is its design simplicity and low power operation. However, larger interpolating factor means larger nonlinearity error, which is caused by performing interpolation between nonlinear signals. The design uses interpolation factor=2 to avoid non linearity and zero crossing point error. Figure 7(a) shows how the resistive interpolation technique can be implemented to generate intermediate signals from the output of folding amplifier. Figure 7(b) shows that there is no zero crossing point error due to folding & interpolating techniques.

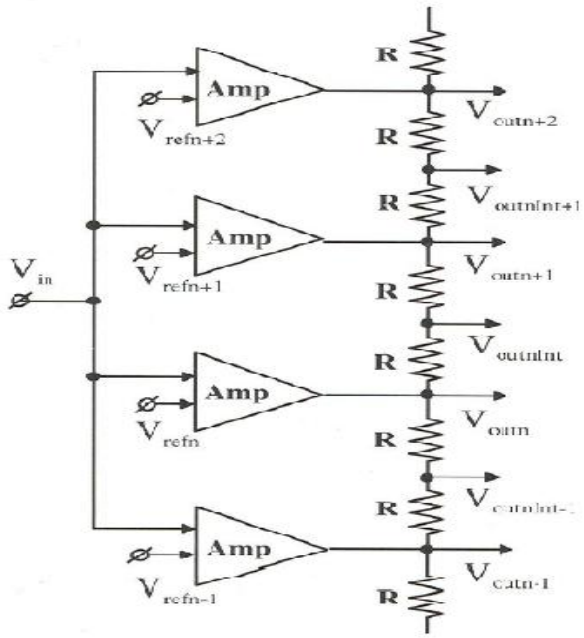

Figure 7(a) Implemented resistive interpolation technique

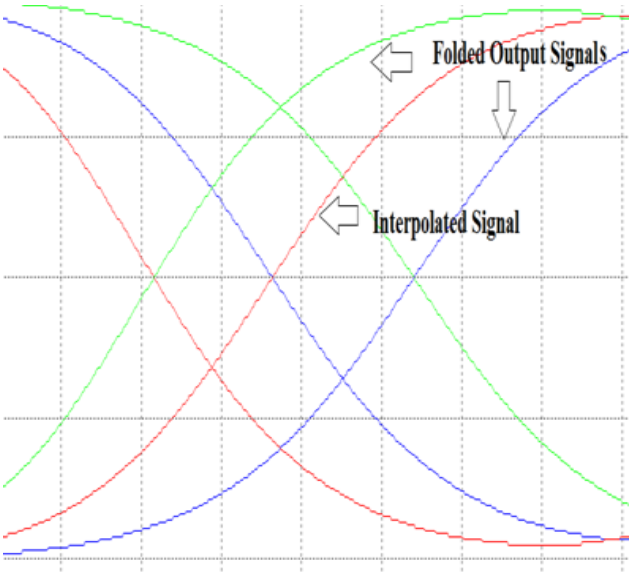

Figure 7(b) No zero crossing point error

Figure 8 shows zero crossing points generated with folding and interpolating stage.

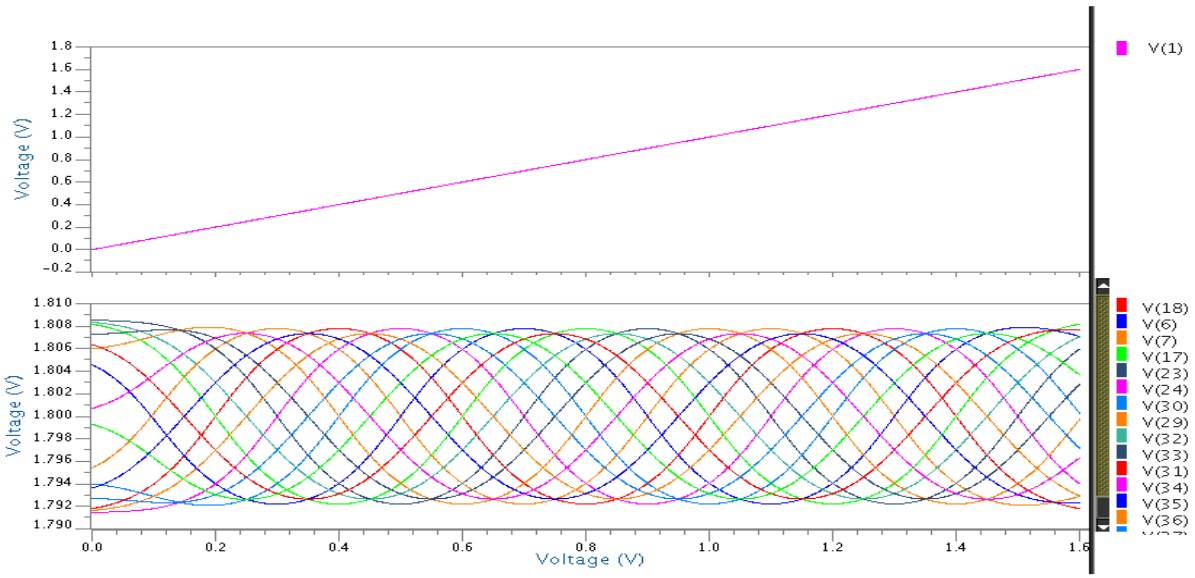

Figure 8 Zero crossing points using folding & interpolation techniques

V. Low Power Voltage Comparator

In order to achieve low power, high-speed operation of the design, comparator is another important block. When a comparator must drive a significant amount of output capacitance in very short times, it is advisable to follow the latch by circuits that can quickly generate large amount of current. A high-speed comparator following these principles is designed in [3][17]. It consists of three stages which are preamplifier, a latch (decision circuit) and output driver. The first stage is a differential amplifier with active loads. It is low gain, high bandwidth amplifier that drives a latch (decision circuit). The decision circuit is the heart of high speed comparator and it should be capable of discriminating mV level signals. [3] The latch outputs are used to drive output buffer stage as shown in Figure 9.The main function of the output buffer is to convert the output of decision circuit into a logic signal. The width of the MOS devices is adjusted in the way that the minimal propagation time delay can be obtained.

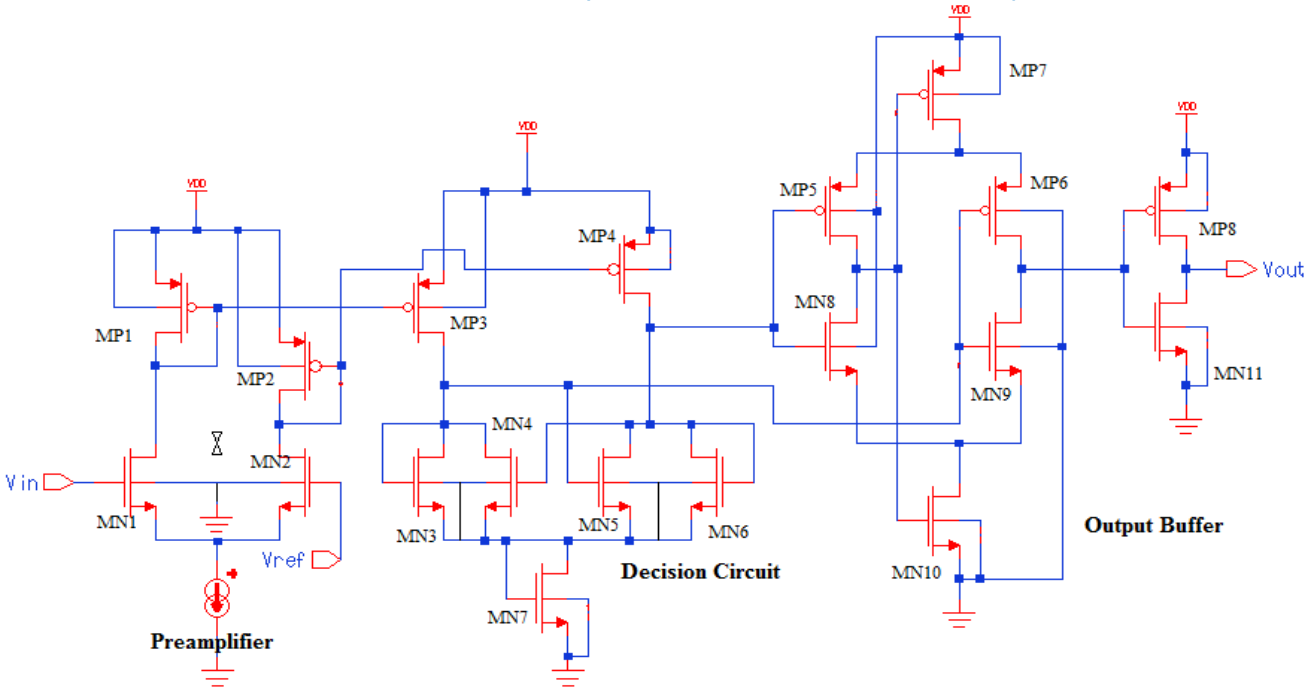

***Figure 9 High Performance Voltage Comparator* [3][17]**

VI. SIMULATION RESULTS

The 5-bit folding and interpolating ADC is simulated at 0.18um CMOS technology, 1.8V supply voltage. To reduce power consumption, active divider is used. Instead of using traditional flash architecture for implementing coarse converter, folding circuit is used as preprocessing. Folding amplifier and comparators are design using low power approach. The simulation result of the high performance comparator is shown in figure 10. The reference voltage Vref=0.3V and the input voltage is varying around this reference voltage which is set the sinusoidal voltage VIN=1.8V and frequency=25MHz. If the input signal is higher than 0.3V, the comparator output will become high.

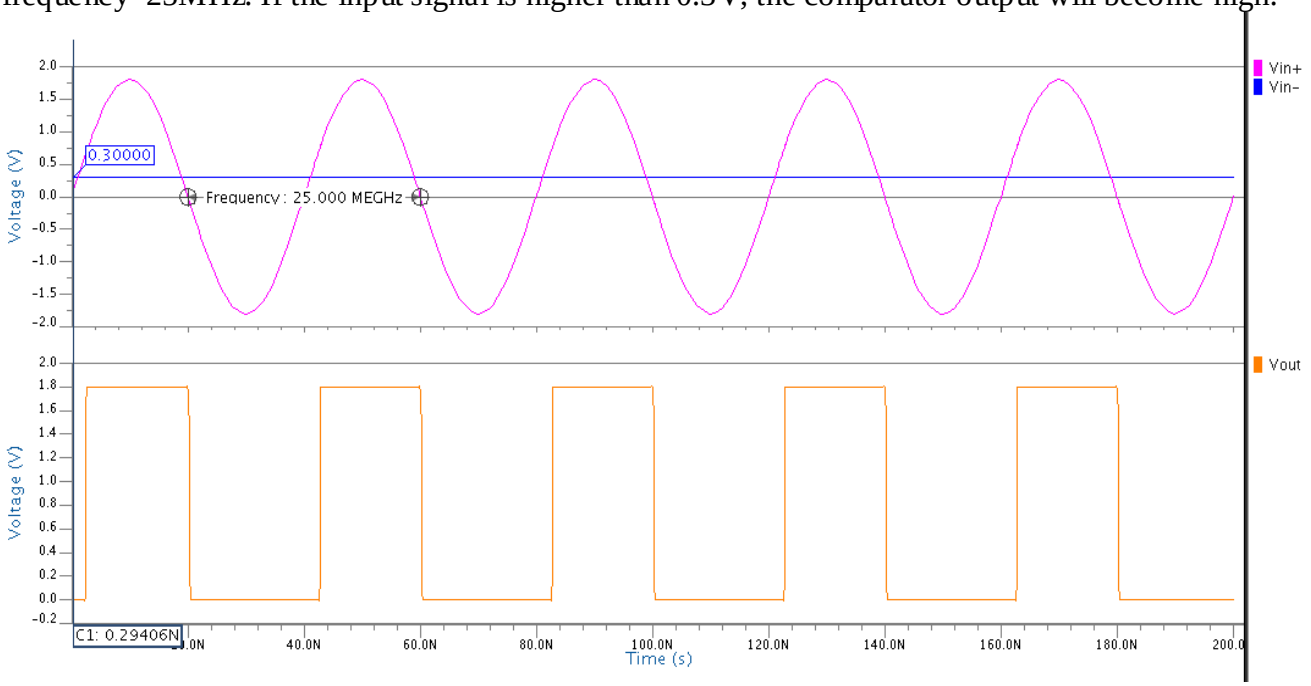

Figure 10 Transient analysis of comparator

Table I summarizes the simulation results of the comparator operating at 25MHz. Furthermore a lower propagation delay is achieved for the circuit with CMOS 0.18um technology as shown in table. Gain

of this comparator is high which is around 60.23dB. DC power dissipation is simulated and is approximately 248.5uW. The bandwidth of this comparator is 26.41MHz

Table I Simulation Results of Comparator

Parameter	Result
Input signal frequency (MHz)	25
Power (uW)	248.5
Delay (nS)	1.627
Gain (dB)	60.23
Bandwidth (MHz)	26.41

The simulation result of the fine converter is shown in figure 11. The output of the comparator array is cyclic thermometer code due to the analog preprocessing. The cyclic output can be easily converted into binary code. The advantage of the architecture is it requires only 9 comparators at the cost of folding amplifier. The folding amplifiers used in coarse converter help in reducing latency difference of fine and coarse converter.

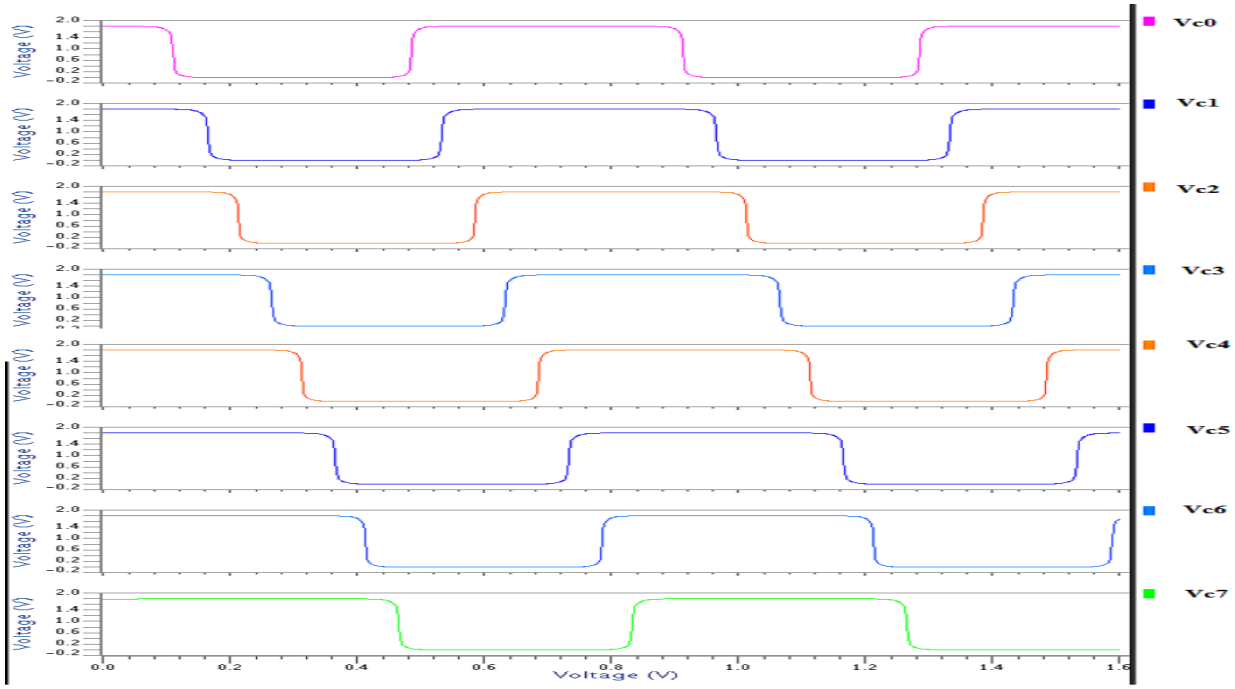

Figure 11 Cyclic thermometer code of Fine converter

Table II shows the truth table for conversion of cyclic thermometer code to binary code. The encoder based on XOR-OR logic can be used to convert the cyclic code into binary. This type of encoder is proposed in [3]. To convert cyclic code into binary, logic shown in equations (2) can be used, comparing binary and cyclic code.[3]

Table II Truth table for cyclic thermometer code to binary conversion

Cyclic Thermometer Code								Binary code			
C7	C6	C5	C4	C3	C2	C1	C0	B3	B2	B1	B0
0	0	0	0	0	0	0	0	0	0	0	0
0	0	0	0	0	0	0	1	0	0	0	1
0	0	0	0	0	0	1	1	0	0	1	0
0	0	0	0	0	1	1	1	0	0	1	1
0	0	0	0	1	1	1	1	0	1	0	0

0	0	0	1	1	1	1	1	0	1	0	1
0	0	1	1	1	1	1	1	0	1	1	0
1	1	1	1	1	1	1	1	1	1	1	1
1	1	1	1	1	1	1	1	1	0	0	0
1	1	1	1	1	1	1	0	1	0	0	1
1	1	1	1	1	1	0	0	1	0	1	0
1	1	1	1	1	0	0	0	1	0	1	1
1	1	1	1	0	0	0	0	1	1	0	0
1	1	1	0	0	0	0	0	1	1	0	1
1	1	0	0	0	0	0	0	1	1	1	0
1	0	0	0	0	0	0	0	1	1	1	1

Encoder logic design:

B3=C7 ..... (5.1)

B2 =C7 XOR C3 ..... (5.1)

B1= (C7 XOR C5) OR (C3 XOR C1) ..... (5.3)

B0= (C7 XOR C6) OR (C5 XOR C4) OR (C3 XOR C2) XOR (C1 XOR C0) ..... (5.3)

Where B0-B3 are 4 bit fine converter output and C0-C7 are 8 bit fine comparator output.

The output of the encoder and coarse ADC is shown in figure 12. VB4 –VB0 are 5 bit output data bits of whole ADC design.

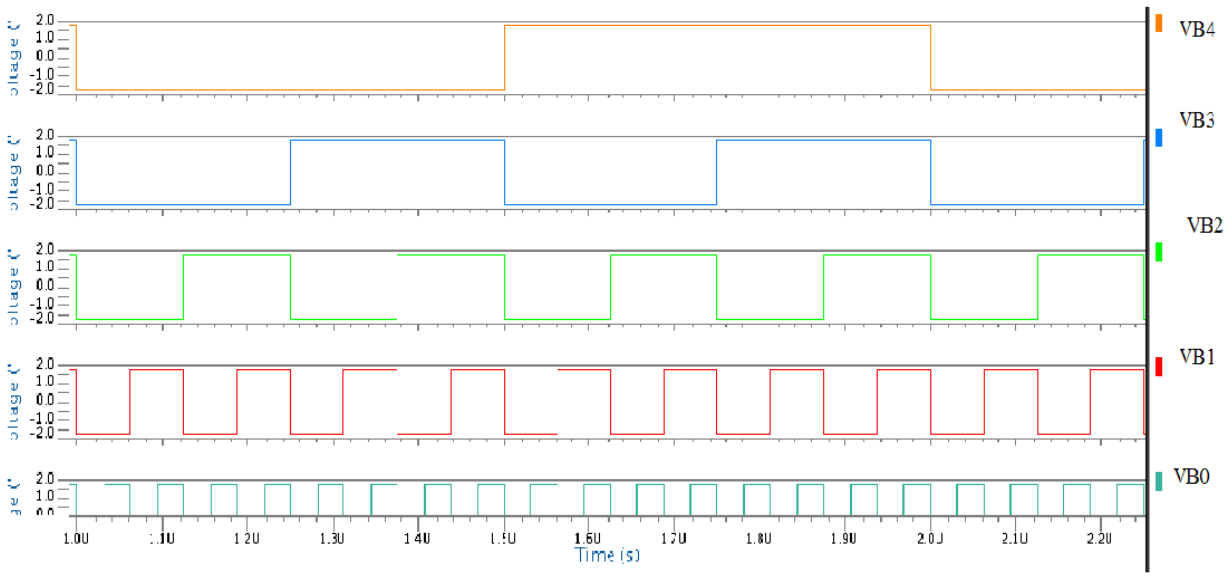

Figure 12 Output of the encoder combined with MSB bit

VII. CONCLUSION

In this paper, low power folding and interpolating ADC is designed with low power folding amplifier and high performance comparator. The architecture uses folding amplifier for both fine and coarse ADC. To achieve low power and high speed operation folding amplifier, comparator and encoder are optimized. The ADC design is simulated using TSMC 0.18um CMOS model file with 1.8V supply voltage. The design proposed in this paper shows that folding and interpolating ADCs have the ability to reach very high conversion speed while maintaining medium resolution with relatively low power dissipation. The simulation results indicate that the designed ADC achieves low power operation.

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