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Characterization and Simulation of Self Cascode CMOS Current Mirror Circuit using 0.18μm Technology

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Abstract —*Current mirror is the core structure for almost all analog and mixed signal VLSI design circuits determine the performance of analog structures, which largely depends on their characteristics. In this paper the current mirror circuits presented, which having low voltage and high output resistance structure has been proposed. The performance of self-cascade CMOS current mirror is optimized with high output impedance and can operate at 1 V or below. The proposed circuit has an input current range of operation is 10μA.To support the analysis, circuit is simulated using Eldo-spice, IC Station and Design Architect(Mentor Graphics).To carry out the simulation, TSMC 0.18μm technology is used.*

Keywords-*Current mirror, cascode current mirror, low voltage analog circuit, analog and mix VLSI design.*

I. INTRODUCTION

Today's modern CMOS technologies with shorter channel lengths, smaller voltage gain and lower supply voltage impose many constraints on the performance and circuit structures of the current mirrors. So that, led to the analog designers to look for innovative design techniques like self cascode CMOS current mirror [1].This paper describe the investigation of the merits and demerits of various current mirror circuits and simulated simple current mirror first then improved our circuit's result by various circuits like cascode current mirror, Wilson current mirror and at last self cascode CMOS current mirror. Finally author has analyzed its results through the SPICE simulations for 0.18μm CMOS technology. [2]

II. SIMPLE CMOS CURRENT MIRROR

The simple current mirror can also be implemented using MOSFET transistors (Figure.1).M1 and M2 transistors are operating in the saturation or active mode. Here, the output current I_{out} is directly related to I_{REF} and Simulation results for I_{out} v/s V_{out} curve for simple Current Mirror is shown in figure.2. In this design channel length modulation is neglected.

$$I_{ref} = ½\ \mu_n C_{ox}(W/L)_1 (V_{gs} - V_{th})^2 \quad \ldots (1)$$

$$I_{out} = ½\ \mu_n C_{ox}(W/L)_2 (V_{gs} - V_{th})^2 \quad \ldots (2)$$

Equation (2) is divided by eq. (1), we have

$$I_{out} = I_{ref} (W/L)_2 / (W/L)_1 \quad \ldots (3)$$

Limitation of circuit

A. The output current is having the channel length modulation effects and current gain is poor is verified by eq.(4)

$$\frac{I_{out}}{I_{RFE}} = \left(\frac{W_2 L_1}{W_1 L_2}\right)\left(\frac{1+\lambda V_{ds\,2}}{1+\lambda V_{ds\,1}}\right) \quad \ldots (4)$$

Where, $V_{ds\,1} \neq V_{ds\,2}$

B. Output resistance is finite and small value.

Simulation Results

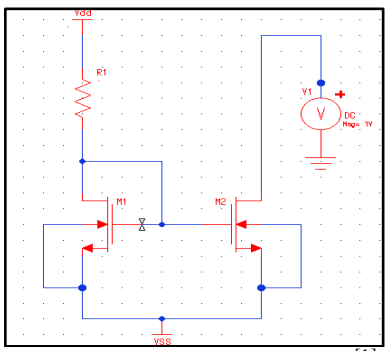

Figure.1 Simple Current Mirror [1]

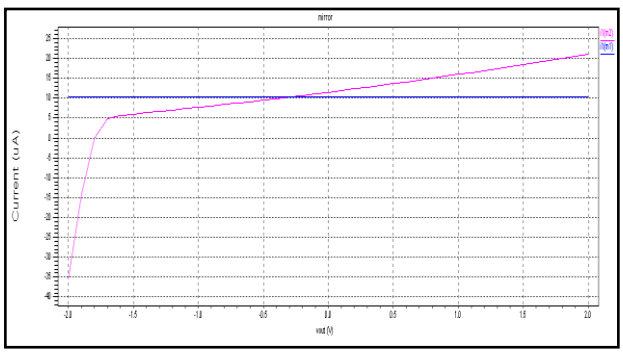

Figure.2 I_{out} v/s V_{out} curve simple current mirror

III. CASCODE CMOS CURRENT MIRROR

The cascode structure is employed to increase the output impedance as shown in figure.3 and the implementation requires NMOS technology which is used to remove the drawback of channel length modulation as shown in simple current mirror. In simple current mirror the channel length modulation effect was not considered. [6] This effect results in significant error in copying current. By the input transistor operating in saturation, the output current will copy the input current; without increases in ambient temperature. Simulation results for I_{out} v/s V_{out} curve for simple Current Mirror is shown in figure.4. [1]

Merits

A. Cascode current mirror eliminates the channel length modulation effect where, $V_{ds1} = V_{ds2}$ is constant.

$$\frac{I_{out}}{I_{RFE}} = \left(\frac{W_2 L_1}{W_1 L_2}\right)\left(\frac{1+\lambda V_{ds2}}{1+\lambda V_{ds1}}\right)$$

B. Output resistance is high.

Demerits

A. Current becomes constant for quite large value of V_{ds} e.g. in this case minimum V_{ds} is 0.5 V.

B. Body effect is also present which create the error in output current.

Simulation Result

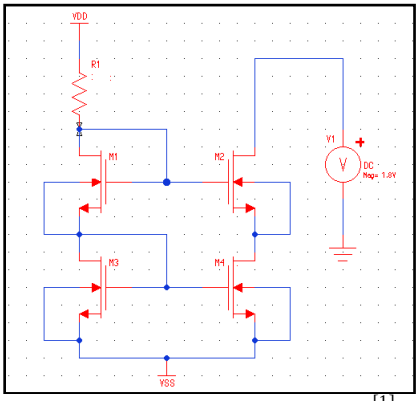

Figure.3 Cascode Current Mirror [1]

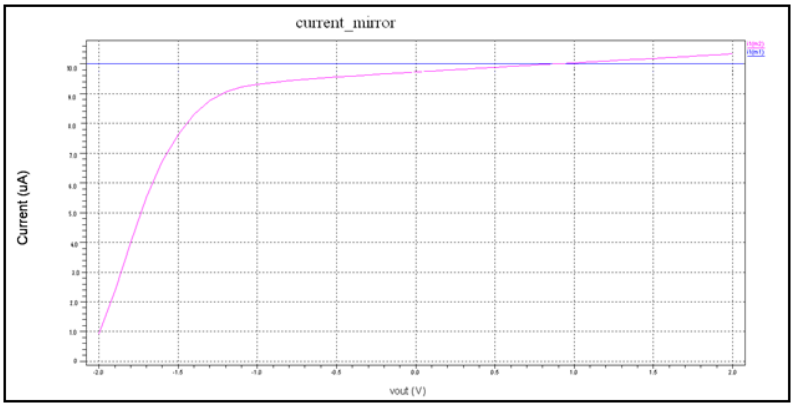

Figure.4 I_{out} v/s V_{out} curve cascode current mirror

IV. WILSON CMOS CURRENT MIRROR

A Wilson current mirror is a circuit which designed to provide a constant current as shown in figure.5. In this, circuit has the advantage of virtually eliminating the current mismatch of the conventional current mirror thereby ensuring that the output current I_{out} is almost equal to the reference or input current I_{Ref} thus eliminating the drawbacks of cascode current mirror structure. Simulation results for I_{out} v/s V_{out} curve for Wilson Current Mirror is shown in figure.6. [1]

Merits

A. Curve is much flatter than the simple and cascade current mirror

B. By the positive feedback effect output resistance become higher than the cascode mirror.

Demerits

B. Current becomes constant for quite large value of V_{ds} e.g. in this case minimum V_{ds} is 0.53 V.

Simulation Results

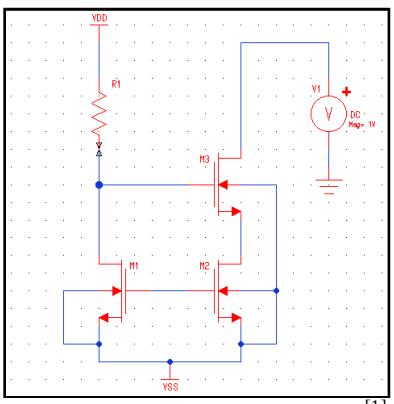

Figure.5 Wilson Current Mirror [1]

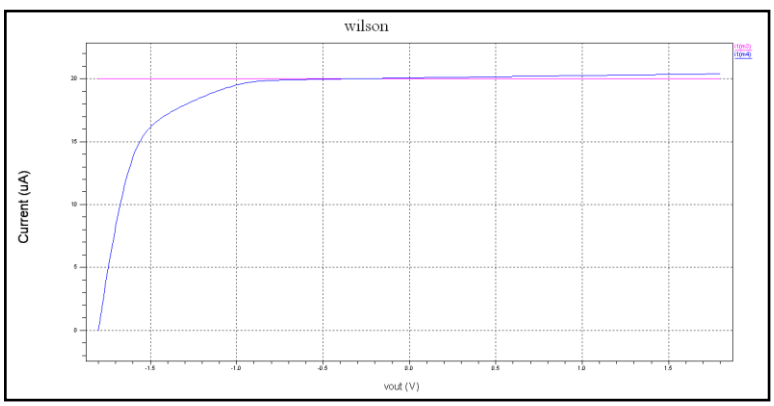

Figure.6 I_{out} v/s V_{out} curve Wilson Current Mirror

V. LOW VOLTAGE SELF CASCODE CMOS CURRENT MIRROR

Figure.7 shows the circuit topology of the self cascode current mirror configuration which is proposed and in this circuit transistor M3 is used for biasing purpose to drive transistors in saturation region. Simulation results for I_{out} v/s V_{out} curve for low voltage self cascade Current Mirror is shown in figure 8. [4-10]

Here, to turn on the Output transistors the required minimum voltage is

$$Vmin_{(out)} = 2V_{ON} \quad \ldots (5)$$

To drive the input transistor the minimum voltage requirement is

$$Vmin_{(in)} = V_T + V_{ON} \quad \ldots (6)$$

Output and input resistance of the proposed current mirror is given by

$$R_{out} = r_{ds1}\, g_{m3}\, r_{ds3} \quad \ldots (7)$$

$$R_{in} = 1 / g_m \quad \ldots (8)$$

Here, the current transfer ratio is excellent because of $V_{DS1} = V_{DS2}$

Merits

A. High performance since output current is constant for low value of V_{out}.
B. Output impedance is higher.

Demerits

B. High Power dissipation.

Simulation Results

The proposed design topology is done using Eldo-spice, IC Station and Design architect (Mentor Graphics).TSMC 0.18µm CMOS technology is used for the simulation. The proposed scheme has an input current range of operation is 10µA and 1V voltage supply is used. Table1 shows technology parameter and Table 2 shows the transistor aspect ratios for self cascode current mirror.

Table. 1 Technology Parameters

Power Supply	V_{dd}=0.9v & V_{ss}= -0.9v
Technology	TSMC 0.18 µm
Model File	LEVEL 53
Spice simulator	Eldo spice, IC Station and Design architect (Mentor Graphics)

Table. 2 Transistor Aspect Ratios of fig.7

Transistors	W (µm)	L(µm)
M1,M2,M4	22	1
M3	8	1

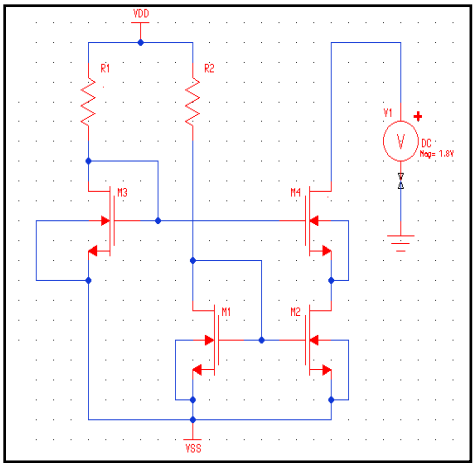

Figure.7 Low voltage self cascode Current Mirror [4]

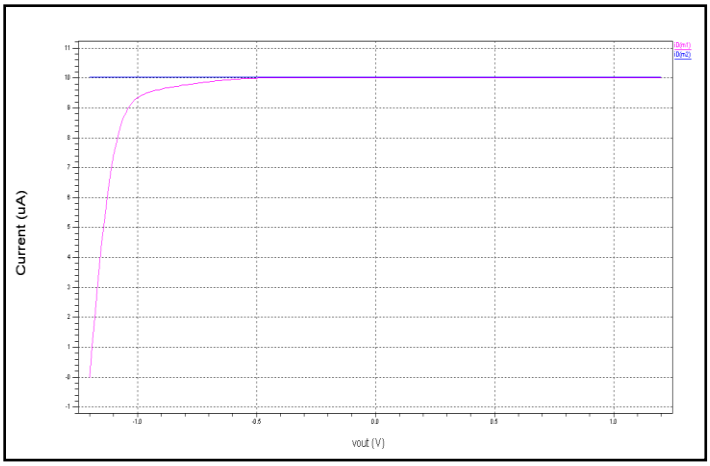

Figure.8 I_{out} v/s V_{out} Low voltage self cascade Current Mirror

Comparison of different current mirrors circuits:

A comparison of different current mirrors circuit base on above simulation is given in Table 3. This Table Compares the values of output impedance for each mirror and the minimum output voltage required for running the circuit.

Table.3 Comparison of different current mirrors circuits

Analysis	Simple	Cascode	Wilson	Low voltage Self cascode
No. of Transistor	2	4	3	4
Power Dissipation	13.55µW	28.76µW	51.73µW	55.02µW
O/P Resistance	11.34K Ω	17.88K Ω	26.97 K Ω	47.74K Ω
Stability	Poor	Good	Better	Excellent

REFERENCES

[1] R. Jecob Baker, Harry W. Li, David E. Boyce, "CMOS Circuit Design, Layout and Simulation", IEEE Press Series on Microelectronic Systems, 1997, pp.613-651.

[2] Phillip E. Allen, Douglas R. Holberg, "CMOS Analog Circuit Design", Oxford University Press, Second Edition, 2002, pp.134-142.

[3] D. Johns and K. Martin, "Analog Integrated Circuit Design" John Wiley & Sons, Inc., New York.

[4] Khalil Monfaredi, Hassan FarajiBaghtash, MajidAbbasi"A Novel Low Power Very Low Voltage High Performance Current Mirror "International Science Index Vol:4, No:10@2010

[5] Yonghua Cong and Randall L. Geiger "Cascode Current Mirrors with Low Input, Output and Supply Voltage Requirements"Roc. 43rd IEEE Midwest Symp. onCis and Systems. Lansing Ms Aug 8-1 1@2000 IEEE.

[6] Erik Bruun and Peter Shah "Dynamic Range of Low-Voltage Cascode Current Mirrors" 0-7803-25'70-2195 $4.00 @1995 IEEE

[7] N. Charalampidis, M. Spasos, K. Tsiakmakis and K. Hayatleh"Analysis, simulation and circuit implementation of a precise high-output impedance analog current mirror" 978-1-4244-5795-3/10/$26.00 ©2010 IEEE

[8] Raguvaran.E, Deepak Prasath.N, Alexander.J, Prithiviraj.N and Santhanalakshmi.M"A Very–High Impedance Current Mirror for Bio-medical Applications" 978-1-4244-9477-4/11/$26.00 ©2011 IEEE

[9] N. Charalampidis, M. Spasos, K. Tsiakmakis and K. Hayatleh"Analysis, simulation and circuit implementation of a precise high-output impedance analog current mirror" 978-1-4244-5795-3/10/$26.00 ©2010 IEEE

[10] Maneesha Gupta, AbhinavMalhotra, AnuMalik"Low-voltage Current Mirror with extended Bandwidth" 978-1-4673-0934-9/12/$31.00 c 2012 IEEE.

