Scientific Journal of Impact Factor(SJIF): 3.134

e-ISSN(O): 2348-4470
p-ISSN(P): 2348-6406

International Journal of Advance Engineering and Research Development

Volume 2,Issue 4, April -2015

# Design and Implementation of Sub Modules of Successive Approximation Register A/D Converter

Purvi J. Patel[1], Priyesh P. Gandhi[2]

[1]PG Student Electronics & Communication, LCIT-Bhandu,Gujarat Technological University, Gujarat, India
[2]Assistant Professor, L.C. Institute of Technology,Bhandu, Mahesana, Gujarat, India

**Abstract** — *This paper describes the implementation of a 8-bit 50 MS/s SAR ADC using 180nm TSMC CMOS VLSI Process in Mentor Graphics. Here main building blocks of SAR ADC like comparator, sample and hold, SAR Register and DAC are implemented. The supply voltage for this SAR ADC is ±1.8 V. The simulation result shows speed of 50 MHz achieved with input frequency of 1 MHz and power dissipation of 0.2v.*

**Keywords**- *SAR, TSMC, ADC, CMOS, VLSI*

## I. INTRODUCTION

ADC is the key building block in today's high speed communication system and video system. With the development of these electronics systems, energy efficient ADC is becoming more important. For processing on signals, digital domain is better than analog because it has many advantages like noise immunity, storage capability, security etc. There are many ADC architectures are available like flash ADC, sigma delta ADC, folding and interpolating ADC, two-step ADC, pipelined ADC, SARADC etc. Comparison of various ADC architectures is shown in Table 1 and its application based on resolution is also shown in Figure 1.

***Table 1. Comparison of various ADC*** [6]

| Architecture | Latency | Speed | Accuracy | Area |
|---|---|---|---|---|
| Flash | No | High | Low | High |
| Folding/interpolating | No | Medium-High | Low-Medium | Medium-High |
| Delta-Sigma | Yes | Low | High | Medium |
| Pipeline | Yes | Medium | Medium-High | Medium |
| SAR | Yes | Low | Medium-High | Low |

Among various ADC architectures, the SAR ADC has the attractive feature of maintaining high accuracy at medium conversion rate. For this reason it is used extensively in acquisition systems and high performance digital communication systems where both precision and smaller area is critical.

In this paper different components of SAR ADC are implemented in 180nm CMOS VLSI Process in mentor graphics.

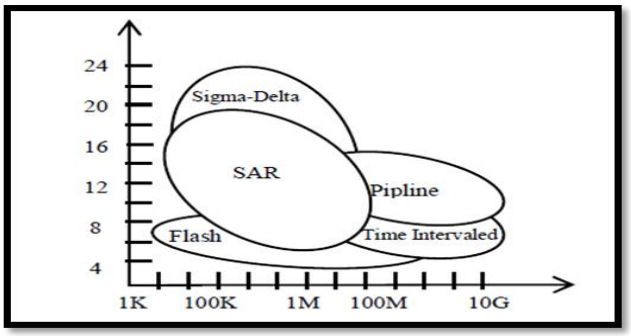


***Figure 1. Various ADC Architectures Based on Resolution*** [5]

 

## II. SAR ADC ARCHITECTURE

A SAR ADC converts a continuous analog signal into a digital representation through a binary search algorithm.

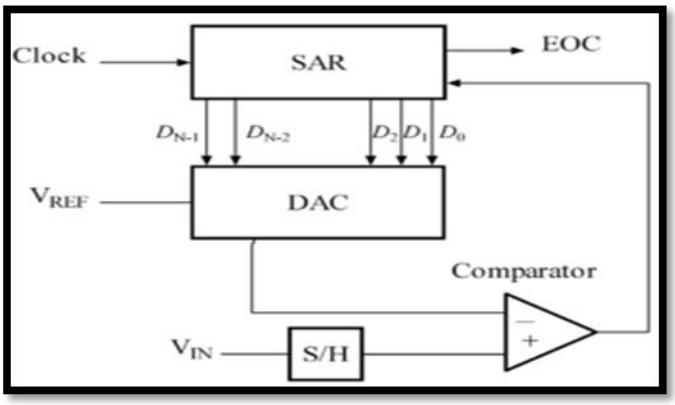


***Figure 2. Block Diagram of SAR ADC*** [7]

This ADC has four main blocks that are a sample and hold circuit, an analog voltage comparator, a successive approximation register and a DAC.

The SAR is initialized by setting MSB bit. This code is applied into the DAC, which then gives the analog equivalent of this code into the comparator circuit for comparison with the sampled input voltage. If $V_{DAC} > V_{in}$ the comparator causes the SAR to reset this bit or the bit is left a 1. Then the next bit is set to 1 and the same process is done, continuing this binary search until every bit in the SAR has been tested. The resulting code is the digital approximation of the sampled input voltage and is finally output by the SAR at the end of the conversion.

## III. CIRCUIT IMPLEMENTATION

### 3.1 Sample and Hold Circuit

SH circuit can be realized using only a transmission gate and a capacitor as shown in figure 3.The operation of this circuit is quite simple. When the clock signal is at logic high level, the TG switch is ON and it allows $V_{OUT}$ to track $V_{IN}$. When the clock signal is at logic low level, the TG is OFF. During this time, capacitance at the output will keep output voltage is equal to the value of $V_{IN}$ at the instance when the clock signal goes low. Transient simulation of sample and hold is shown in figure 4.

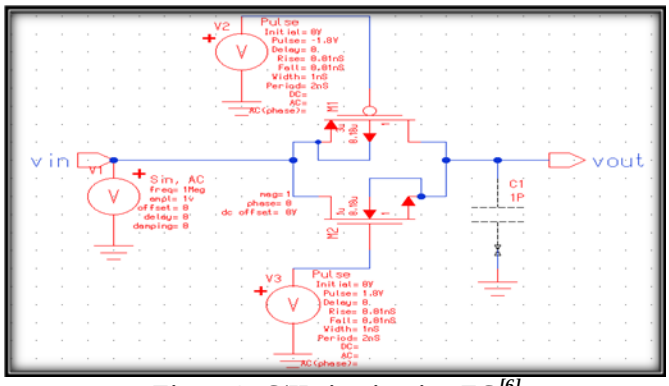


***Figure 3. S/H circuit using TG*** [6]

 

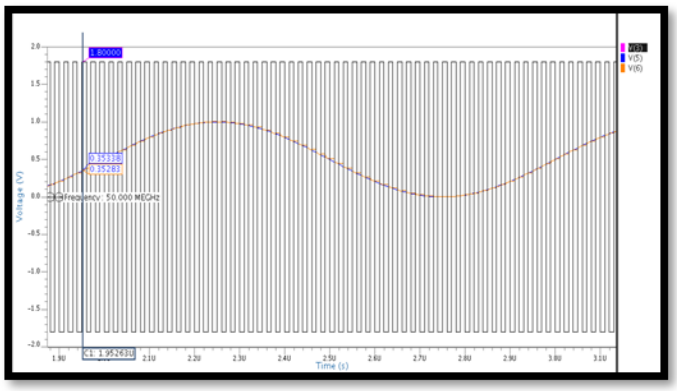

*Figure 4. Transient simulation of Sample and Hold*

### 3.2 Comparator

The SAR ADC consists of a comparator which is used to compare two signals one is from the output of sample and hold and second is from the output of DAC. Here two stage open loop OPAMP is used as a comparator. When a sine wave is input to the circuit, the comparator switches from logic high to logic low. Implementation of comparator and simulation result of comparator is shown in Figure 5 & 6 respectively.

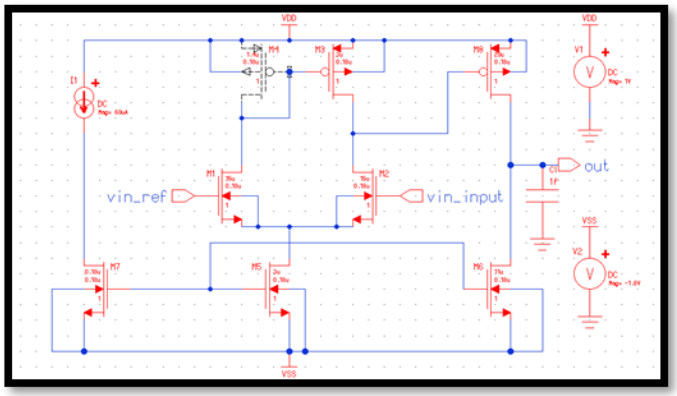


*Figure 5. Design of Comparator [2]*

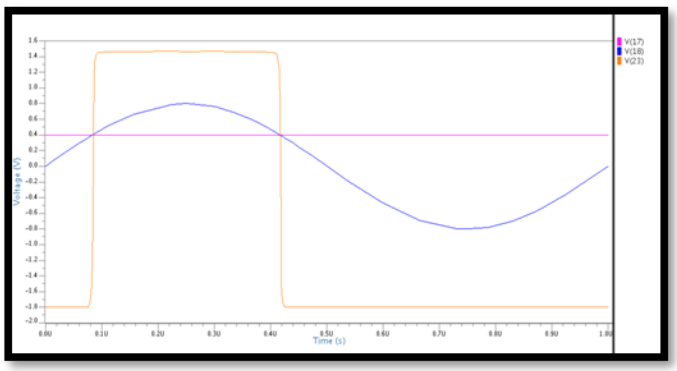

*Figure 6. Transient simulation of comparator*

### 3.3 Successive Approximation Register(SAR) Logic

SAR logic consists of a ring counter and a shift register. At least 2N-1 flip flops are employed in this kind of SAR. SAR control logic determines the value of bits sequentially based on the result of the comparator. Each conversion takes 9 clock cycles. In the first clock cycle, SAR is in the reset mode and all the outputs are zero. In the next 8 clock cycles, data is converted and each bit is determined sequentially. The last cycle is for storing the results of the complete conversion.

 

In each cycle of clock, one of the outputs in the ring counter sets a Flip Flop in the code register. The output of Flip Flop is used as the clock signal for the previous Flip Flop. At rising edge of the clock, this Flip Flop loads the result from the comparator.

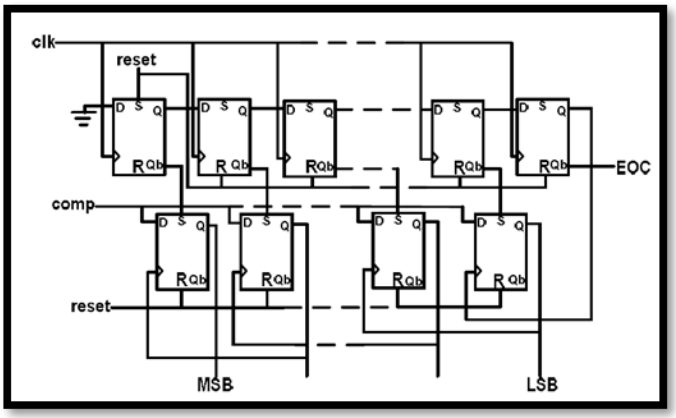


***Figure 7. Block Diagram of SAR Logic*** [3]

### 3.3.1 D Flip-Flop

The schematic of the DFF is illustrated in Figure 8. This register is sensitive to the positive edge of the clock. Here output Q follows the input D when the clock is at logic 1.And when the clock signal goes to logic low, the output will preserve its state.

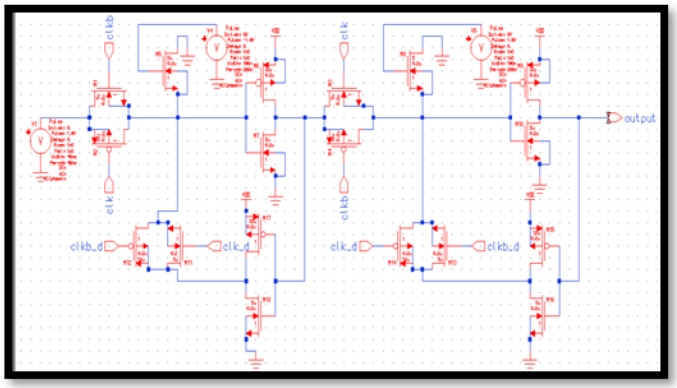

***Figure 8. D Flip-Flop*** [4]

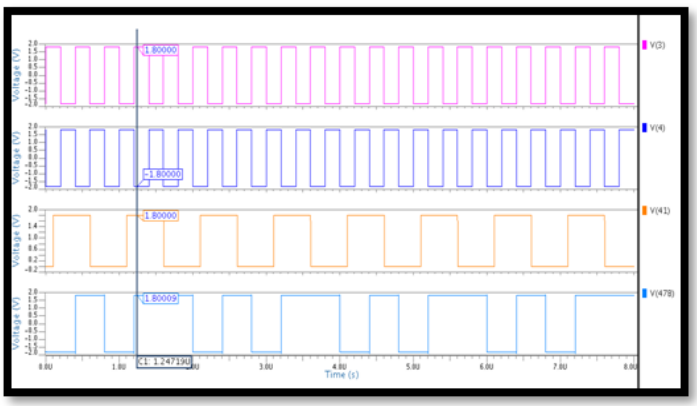

***Figure 9. Transient response of D Flip Flop***

 

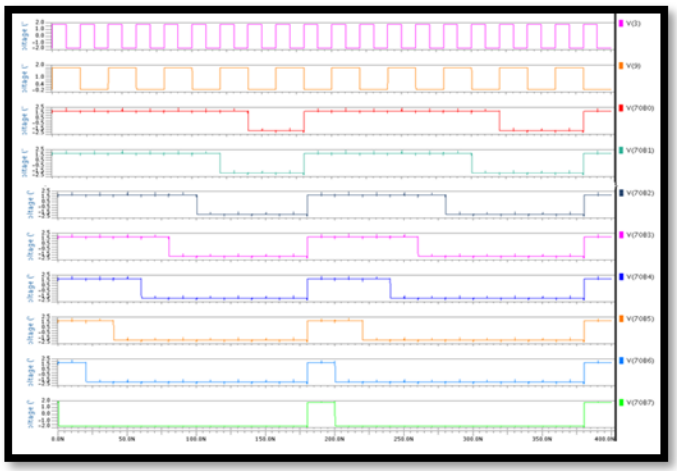

*Figure 10. Transient response of 8-Bit SAR Logic*

### 3.4 DAC

There are many DAC architectures available. Among them, charge scaling DAC is used in this ADC. It consists of a parallel array of binary-weighted capacitors that are connected to an op-amp. Initially capacitances are discharged and then the digital signal switches each capacitor to either $V_{REF}$ or ground, causing the output voltage to be a function of the voltage division among the binary-weighted capacitors.

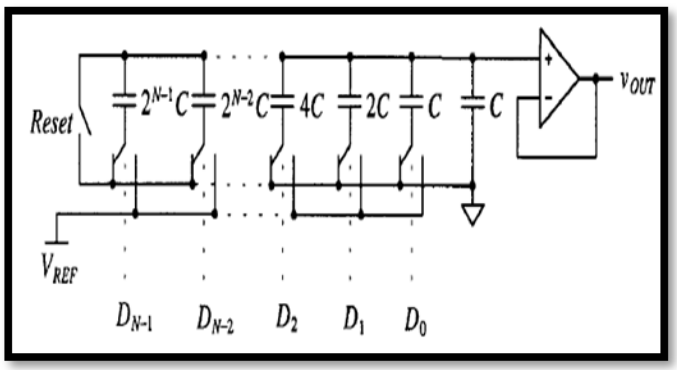


*Figure 11. Block Diagram of Charge Scaling DAC [1]*

#### 3.4.1 OPAMP

Operational amplifiers are used here in DAC part. Here OpAmp is used as a buffer. Two stage operational amplifier is used in this paper.

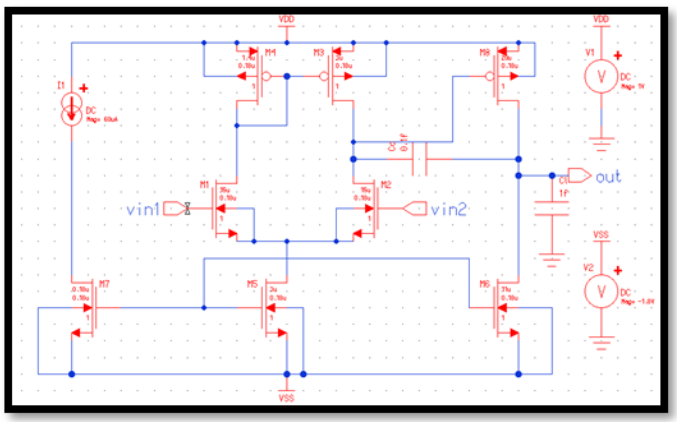


*Figure 12. Two Stage OPAMP circuit [2]*

 

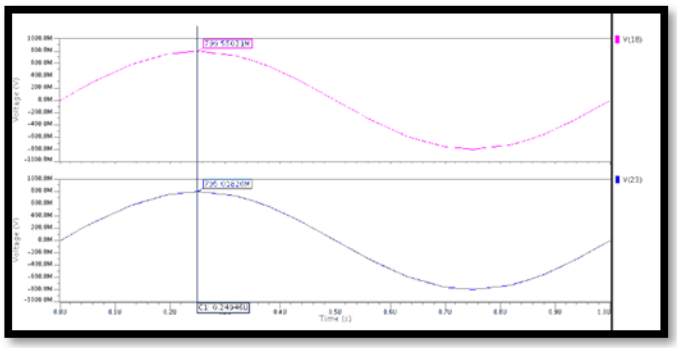

*Figure 13. Transient response of OpAmp*

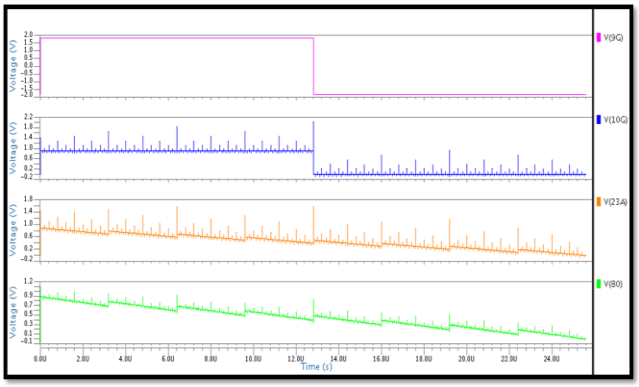

*Figure 14. Transient response of 8-Bit DAC*

## V. SUMMARY OF SIMULATION RESULT

Table 2. Summary of Simulation Result

| Parameter | Value |
|---|---|
| Technology | 180nm |
| Supply voltage | 1.8V |
| Samples | 50MS/s |
| Input Frequency | 1MHz |
| Speed | 50MHz |
| Power dissipation | 170mW |

## IV. CONCLUSION

In this paper to design high performance SAR ADC, different key building blocks of SAR ADC such as Sample and Hold, Comparator, two Stage Operational Amplifier ,DAC and SAR Logic are implemented and Simulated in 180nm TSMC digital CMOS process with sampling rate of 50MS/S.

## REFERENCES

[1]. R. Jecob Baker, Harry W. Li, David E. Boyce, "CMOS Circuit Design, Layout and Simulation", IEEE Press Series on Microelectronic Systems, 1997, pp.685-699.
[2]. Phillip E. Allen, Douglas R. Holberg, "CMOS Analog Circuit Design", Oxford University Press, Second Edition, 2002, pp.439-488.
[3]. Meghana Kulkarni, Muttappa Shingadi, G.H. Kulkarni, "6-Bit Charge Scaling DAC and SAR ADC", IJAREEIE Vol. 3, Issue 12, December 2014
[4]. Rabeeh Majidi, "Low Power Design of Successive Approximation Registers" Worcester MA USA

 

[5]. Hur A. Hassan, Izhal Abdul Halin, Ishak Bin Aris , Mohd Khair Bin Hassan Presented, "Design of A Low Power 8-bit SAR-ADC CMOS" Proceedings of 2009 Student Conference on Research and Development (SCOReD 2009),16-18 Nov. 2009, UPM Serdang, Malaysia
[6]. Bharti Chaudhri, "Development of High Performance Pipelined ADC", Thesis Gujarat Technological University, Department of Electronics and communication Engineering, May-2014.
[7]. Http://en.m.wikipedia.org/wiki/Successive_approximation_ADC

 