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NON OVERLAPPING CLOCKS FOR SWITCHED CAPACITOR CIRCUITS

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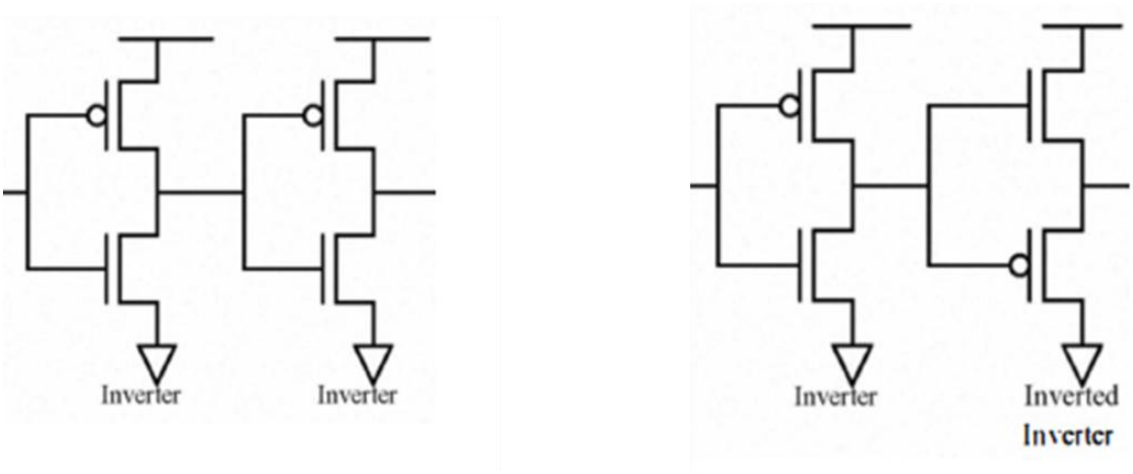
Abstract: Switched capacitor techniques are very popular forimplementation of Mixed Signal blocks in CMOS VLSI. Non-OverlappingClock (NOC) generator is one of the key blocksin the implementation of switched capacitor circuits. StandardNOC generator circuits available in the literature uses delaycircuits realized using simple inverters connected in a chain. By using inverter chain delay generated is very small so to generate larger delay it requires larger numbers of inverters. This affects the area and powerbudget of the design. In this work it is proposed to use invertersin inverted form to realize significant delay with less number oftransistors. Simulation results suggest that the proposed circuitwill be area and power efficient as compared to the conventionalNOC circuits.

Keywords: NOC(Non-overlapping clocks), SC (Switched capacitor circuits), Inverted inverter

I. INTRODUCTION

In Analog and Mixed Signal design Switchedcapacitor(SC) circuits are the most default standard for circuitimplementation in CMOS VLSI. SC circuits are veryimportant as analog signal processing blocks such as switchedcapacitor integrators, filters and voltage comparators. Mixedsignal applications like Analog to Digital Converter (ADC),Sigma Delta Modulators and Sampled Analog Architecturesemploy Switched Capacitor circuits extensively. SC circuits offerseveral advantages such as high accuracy, low power consumptionand better temperature invariance. To implement any SCblock, it is required to charge and discharge the capacitorthrough switches by means of a non-overlapping clock. Forimplementation of NOC generator, there are several standard designsbased on the delay element realized through chain of invertersand few NAND/NOR gates. To achieve larger delay, some technique demands more number ofinverters which in turn consumes more power and area.To reduce the number of stages for a given delay,use of transmission gates (TG) between two inverters are alsoproposed. In this kind of design, the delay of combinedblock (Inverter + TG) is more than that of twoinverters of same size mainly due to the larger input capacitanceseen by the inverter. However, two parallel charging(discharging) paths through NMOS and PMOS combinationeffectively reduces the delay than expected.

In this paper use of inverter in combinationwith an Inverted inverter (altering the position of nMOS withpMOS and vice versa) as a unit delay element. As mentioned, the delay of this combination is more for two reasons. First,the signal swing of the inverted inverter is not rail to railbut less by VT on both sides. Therefore, the effective voltage swingof the inverted inverter output is between $VDD - VTn$ to$|VTp|$. However, the voltage swing will beless if the input voltage to the inverted inverter has less thanfull swing, which will be the case when number of such blocksis connected as a chain. Thus, switching delay is increased bynot allowing the inverter transistors to tum off during the entireexcursion of the signal. Therefore, when NMOS transistor ofthe inverter is applied high voltage ($VDD - VTn$), both pulldownpath and pull-up path is active. Moreover, the nMOStransistor will be getting less gate source voltage, which resultsless drain current to pull the output to low state. Eventually,the discharging will be slower than that of a normal inverterwith input VDD. Using similar logic, it is evident that pull-uptime will also be slower than that of a normal inverter withlogic 0 input.



(a) (b)

Figure 1: Delay chain (a) Cascaded inverter, (b) Inverter with inverted inverter

II. DELAY OF INVERTED INVERTER

The inverted inverter can be viewed as similar topass gate, where the drain terminal of nMOS is input, whichis now connected to VDD and the switch is activated by aweak logic high signal. Also, the drain terminal of PMOSis connected to ground and the switch is activated by weaklogic low signal. If we assume that the weak 1 (generatedat the output of the inverter) is represented by $(VDD - x)$,the output of the pass gate will be $(VDD - x - VTn)$, whereVTn represents the threshold voltage of the inverter with bodyvoltage $\sim VDD - VTn$. Similarly, the output voltage of the passgate when pMOS pass transistor is on will be weak 0 andis $\sim VTp$. Here also, $|VTP|$ represents the threshold voltage ofthe pMOS transistor with substrate bias of VTP which willbe quite higher than $VTpo$.

III. NON-OVERLAPPING CLOCK GENERATOR

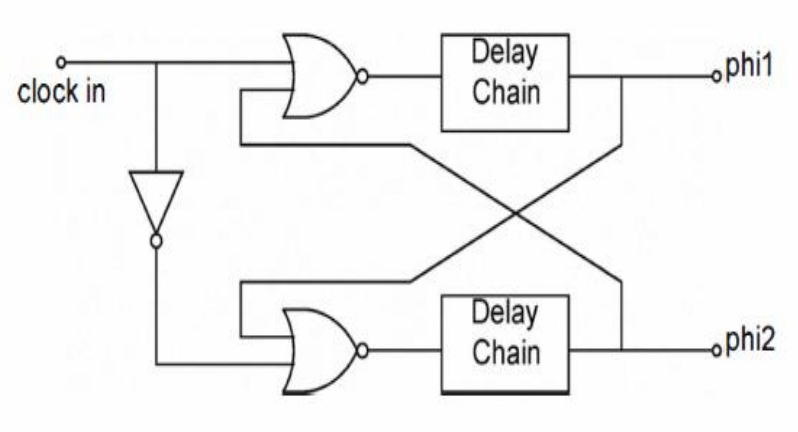


Figure 2: Block diagram of non-overlapping clock generator

To generate non-overlapping clocks with better delay, the block diagram is shown in figure. Here the NOR based circuit and for delay chain cascaded inverted inverter is used. As mentioned earlier inverted inverter has larger delay than cascaded inverter with same transistor count. Also by increasing stages we can achieve larger delay.

IV. SIMULATION RESULTS

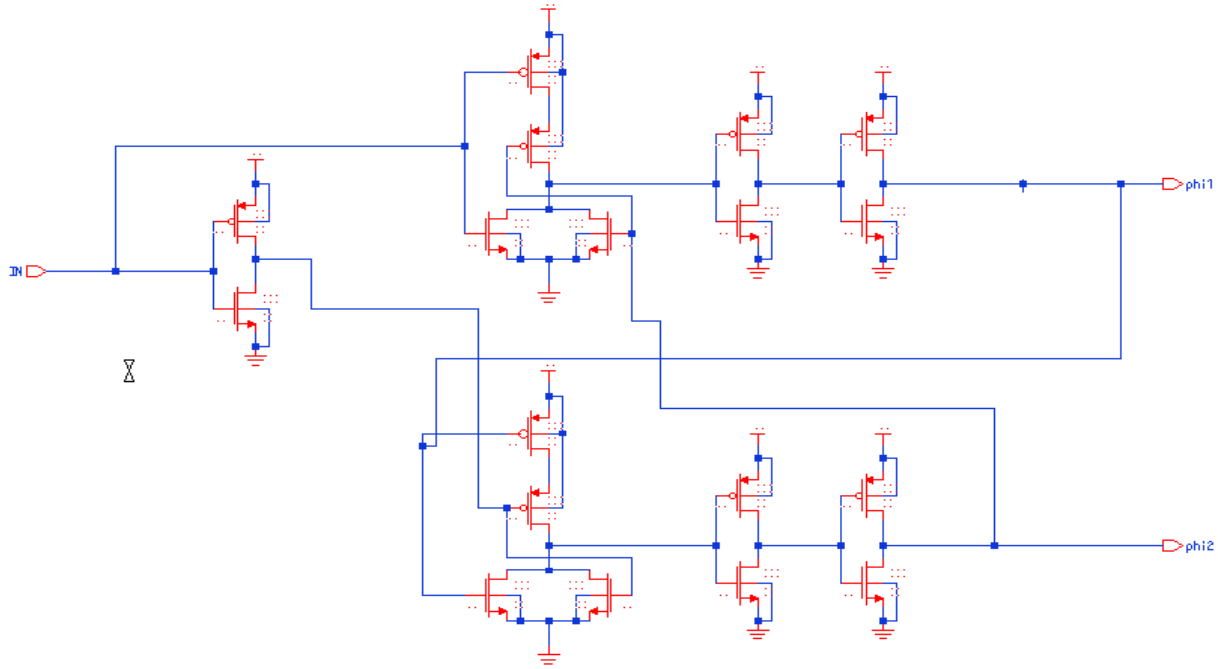


Figure 3: Non overlapping clock generator using inverter chain

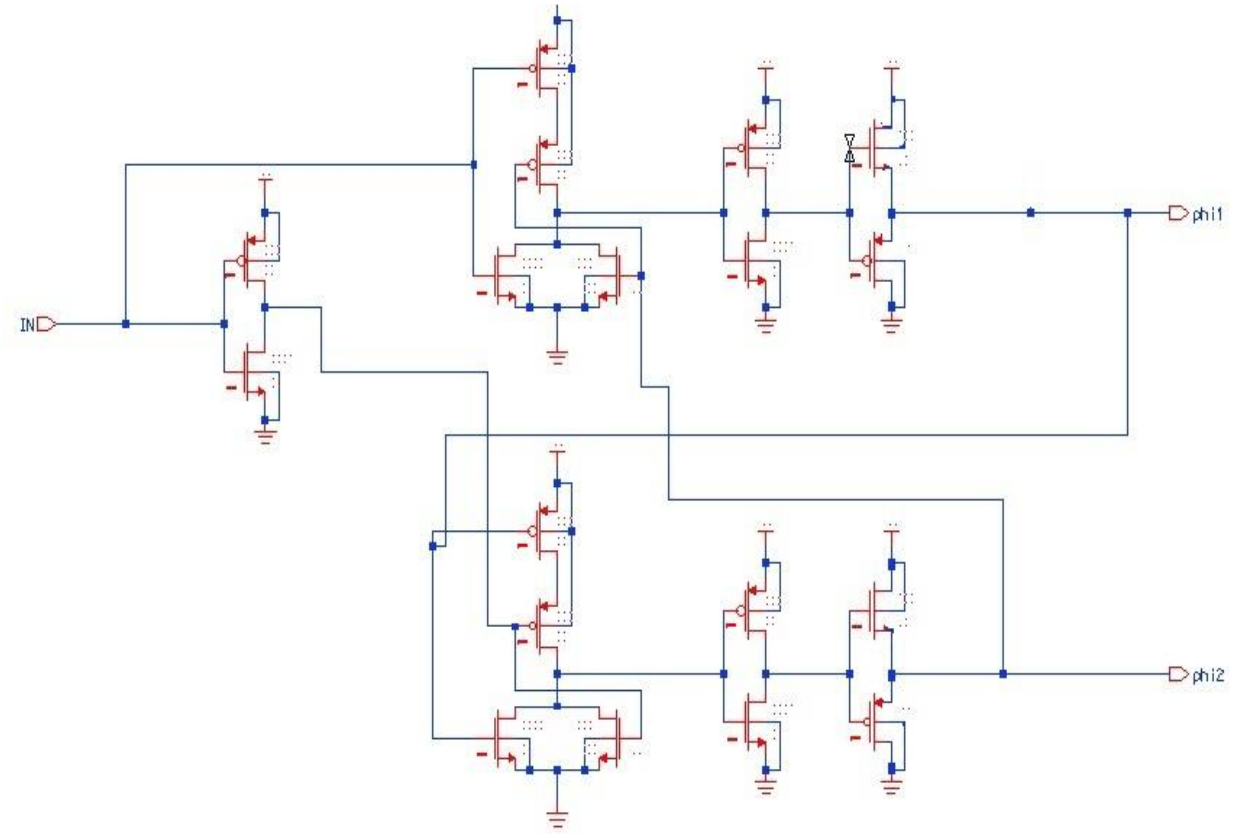


Figure 4: Non overlapping clock generator using inverted inverter

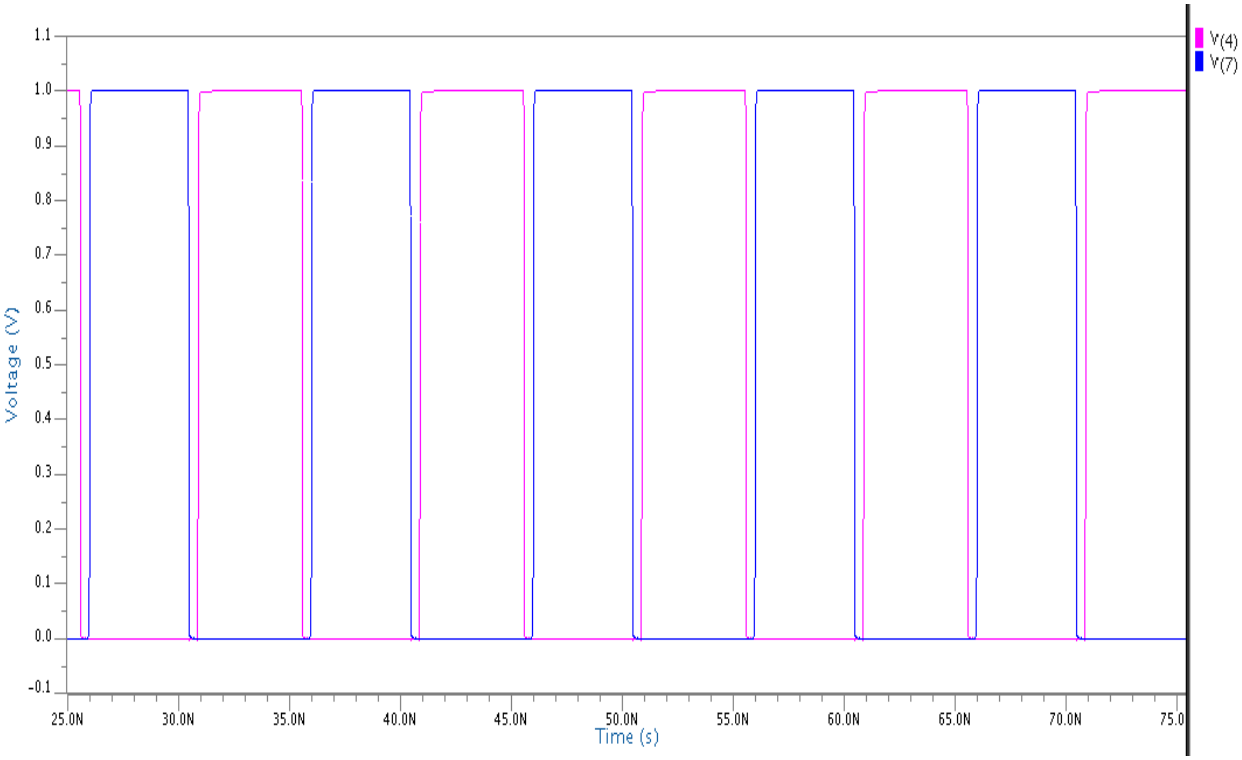


Figure 5: Non overlapping clock signals using inverted inverter

TABLE I: Delay comparison of non-overlapping clock generator using different architectures

	Cascaded Inverter	Inverter with Inverted inverter
Transistor Count	4	4
Delay	153ps	5.111ns

TABLE II. Comparison Table

	This work	[2]
Technology	90nm	180nm
Transistor Count	4	4
Delay	5.111ns	7.2ns

V. CONCLUSION

In this paper we have used inverter in combination with inverted inverter to generate non-overlapping clock signals. Use of this block is generates larger delay compared to inverter chain. By using this, delay between two non-overlapping clock is 5.111ns in 90nm technology.

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