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Offset Analysis and Performance Optimization of Charge Sharing Dynamic Latch Comparator

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Abstract: In Charge Sharing Dynamic Latch Comparator the minimum amount of differential voltage at the input can be detected correctly at the output of the comparator if it does not get affected by the noises and errors generated inside the comparator. To improve the performance of the Charge Sharing Dynamic Latch comparator, all the noises and errors should be minimized. In this paper, an attempt has been made to reduce the offset error generated within the latched comparator by introducing extra circuit elements.

Keywords : Charge Sharing Dynamic Latch Comparator, Offset error Optimization

I. INTRODUCTION

A Comparator is a circuit which compares the two analog signal and depending on the comparison gives the output either logic '1' or logic '0'[1]. Because of the high speed operation and low power consumption latched comparators are very much suitable for high speed Analog-to-Digital Converters (ADC). The high speed are obtained due to the positive feedback mechanism present in the Charge Sharing Dynamic Latch comparators. In addition to the high speed operation and low power consumption, good resolution of the latched comparator is very much essential in order to improve the performance of the latched comparator. This parameter of the comparator gets affected due to the noise and errors generated within the comparator. The noise and errors which affect the performance of the comparator so far the circuit is concerned are: kickback noise, offset error, and metastability error. Offset error occurs due to the lack of symmetry of the latched comparator circuitry. This offset error limits the minimum achievable comparator resolution. In other words, the input signal whose amplitude is smaller than the input offset voltage will not be correctly detected by the comparator[7].

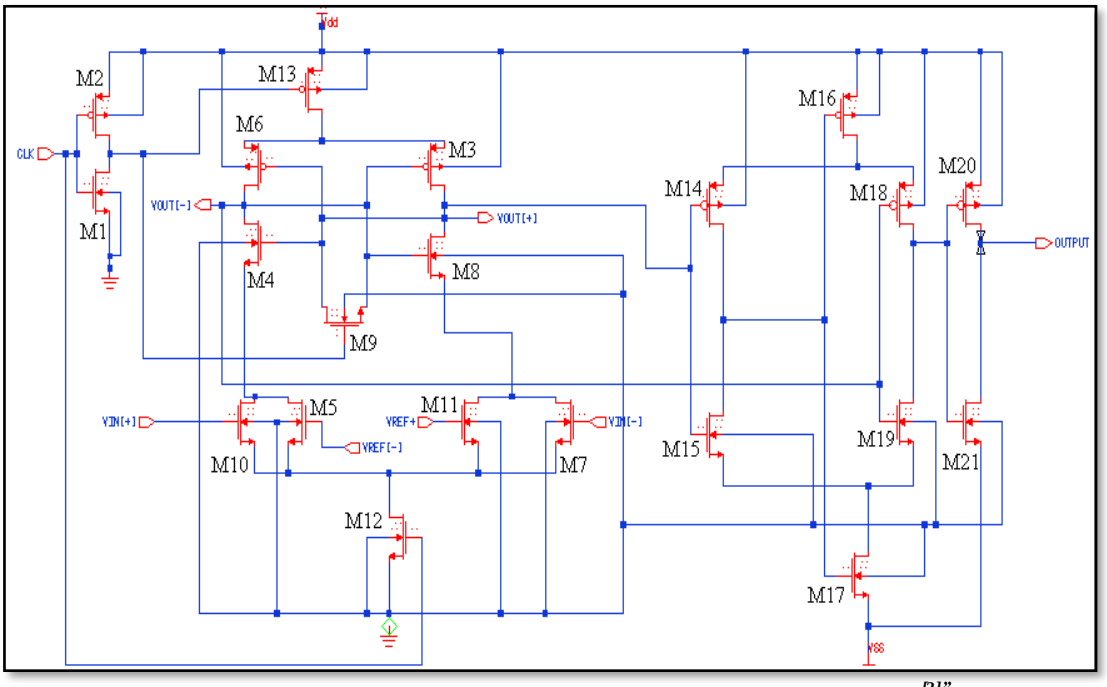
The subsequent sections have been arranged in the following manner. Section 2 describes the Charge Sharing dynamic Latch Comparator. Offset error optimizations and full circuit implementation are discussed in Section 3. Section 4 simulation results are presented. Finally, Section 5 concludes the paper.

II. CMOS VOLTAGE COMPARATOR

2.1 Theory

This topology combines the good features of the other two of dynamic latch comparator that suitable with pipeline A/D converters which is resistive dividing comparator and differential current sensing comparator . The nMOS transistor M12 is used in series with resistive comparing circuit for regenerative mode in order to achieve low power. For reset mode pMOS pre charging circuit is absent and nMOS transistor M9 for output pass transistor for the equalization of both the voltages nearly to Vdd/2. Now, when the clock goes low, Vdd and ground both will be disconnected from the latch with the help of transistors M12 & M3.

The two ended output of the dynamic charge sharing comparator are Vout+ & Vout-. Both the outputs of the comparator are inputs to the buffer. Thus the two ended output of dynamic charge sharing comparator is being converted into single ended output for different types of analysis.



"Figure.1 schematic of Charge Sharing Dynamic Latch Comparator[2]"

2.2 Designing of the comparator

Table4.4 given below shows different widths of the transistor to be used according to the chosen technology. The length for the transistor is 0.1µm respectively for 90nm technology.

Table 1. CMOS Transistor widths in 90nm Technology

Transistor	Technology
M1,M4,M5,M7,M10,M11	0.12
M2,M3	0.12
M6,M13,M14, M16,M18,M20	0.12
M8,M9,M12, M15,M17,M19,M21	0.12

"Table 2. Different Voltage Values for 90nm Technology"

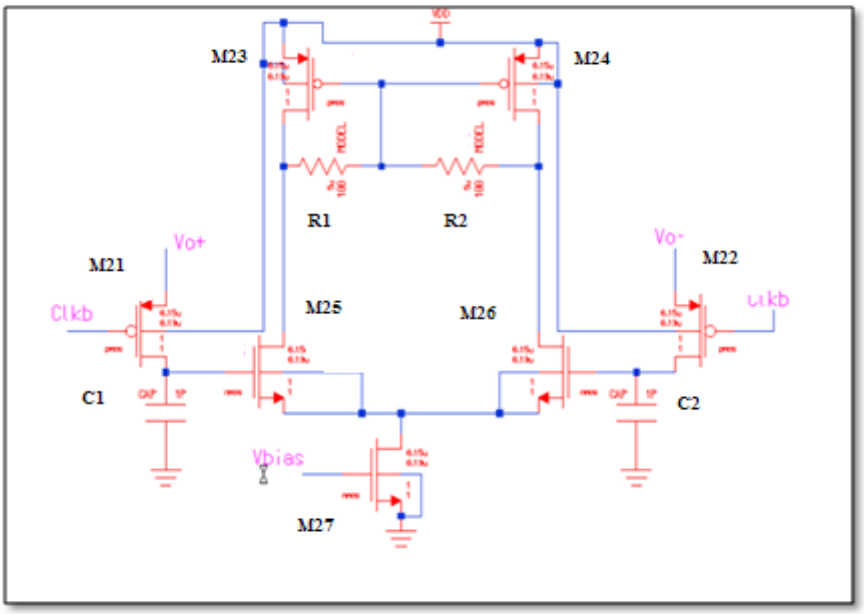
Voltage Terminals	Voltage Values(V)
Vdd	0.9
Vss	-0.9
Clkb	-0.9
Vin+	0.9
Vin-	-0.9
Vref+	0.45
Vref-	-0.45

In Table 4.5, different voltage values are given for supply voltage VDD and VSS, reference voltage Vref+ and Vref-, input voltage Vin+ and Vin-.

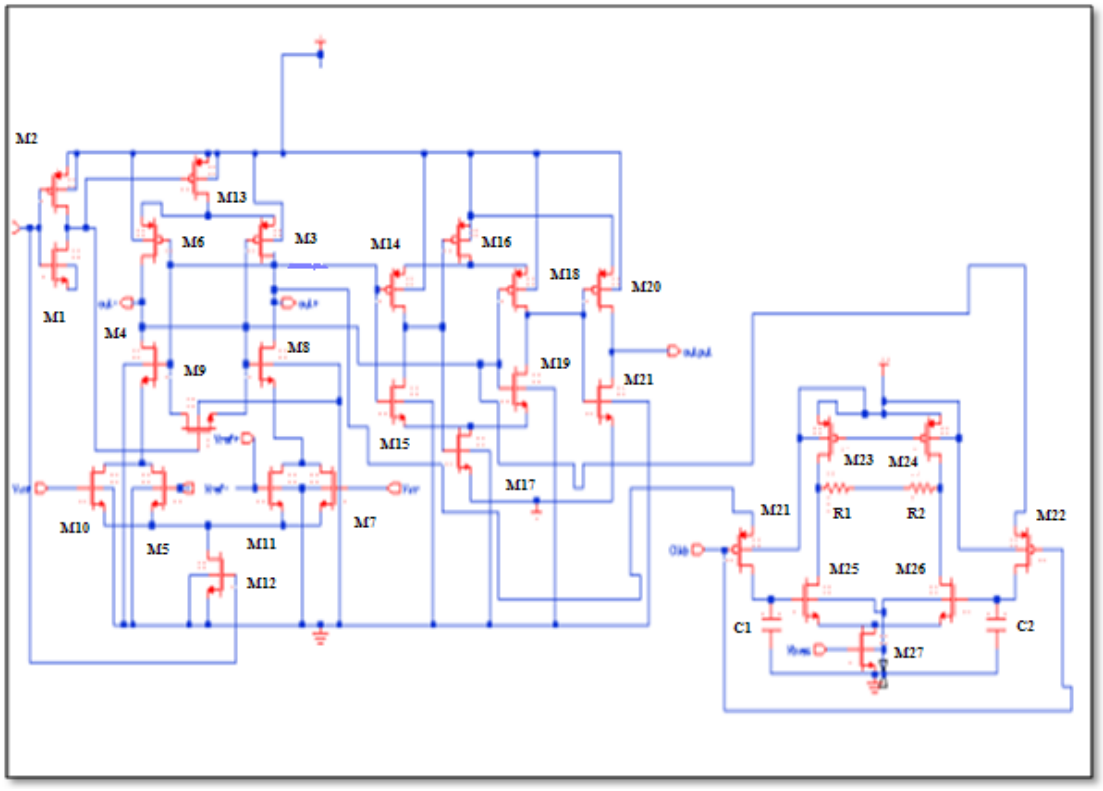
III. OFFSET ERROR OPTIMIZATION

To minimize the offset error due to mismatches in the components present in the latched comparator shown on figure 1, an offset cancellation negative feedback-loop circuit has been added. The modified latched comparator circuit is shown in figure 3.

This comparator works in three different phases: offset cancellation phase, tracking phase and latching phase. In the offset cancellation phase, clkb becomes high and clk becomes low which causes transistor 21 and 22 on bringing the offset cancellation block into action. The offset cancellation feedback-loop consists of a differential pair with active load. Its common mode voltage is set by resistive common mode feedback R1 and R2. When clkb moves to logic low with clk at logic low state, offset cancellation phase stops .



"Figure.2 Offset cancellation block[7]"

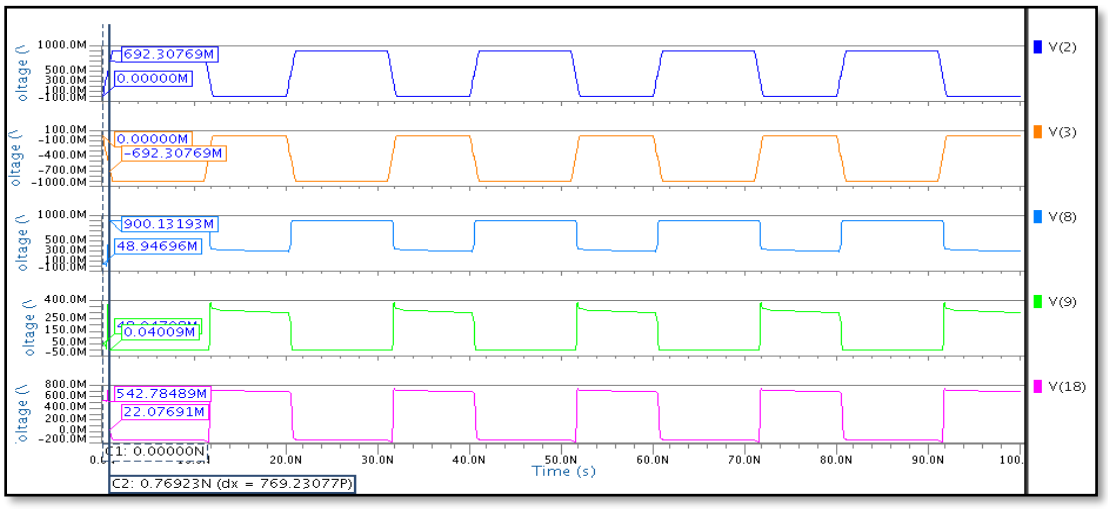


"*Figure.3 Modified Comparator Circuit*"

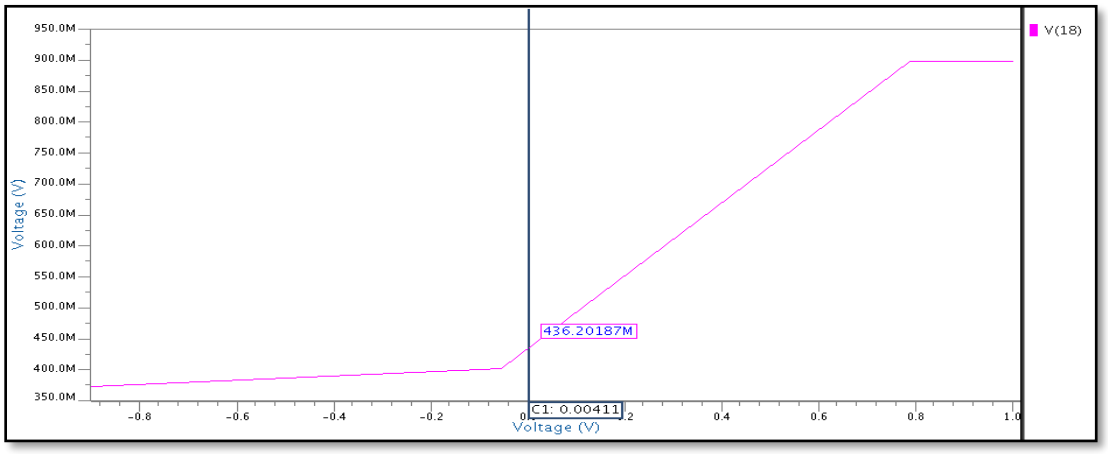
IV. SIMULATION RESULTS

The simulated results are obtained for 90nm technology. InTable-I, different voltage values are given for supply voltage VDD and VSS, reference voltage Vref+ and Vref-, input voltage Vin+ and Vin- and Clkb.

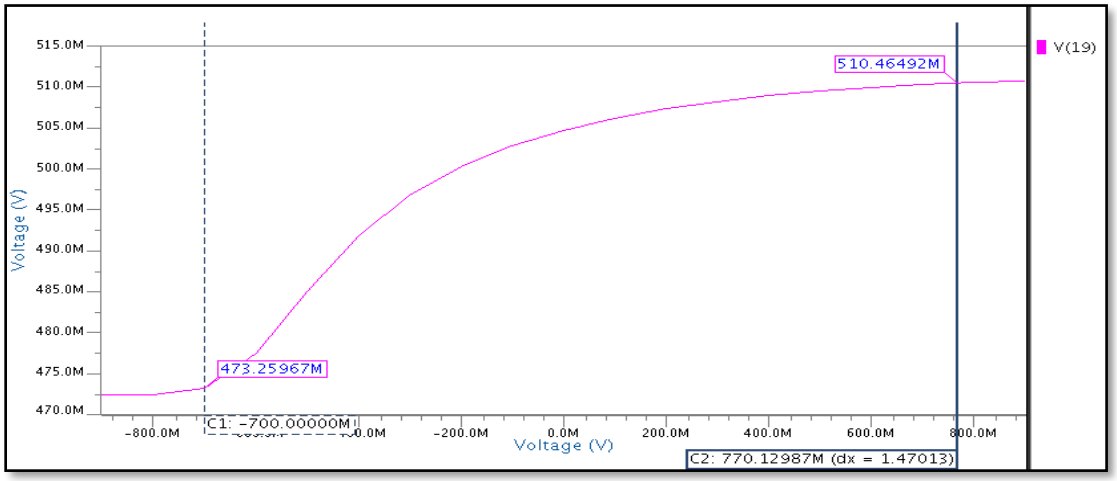
A.Simulation results of CMOS voltage comparator in 90nm Technology



"Figure.4 Transient Response"

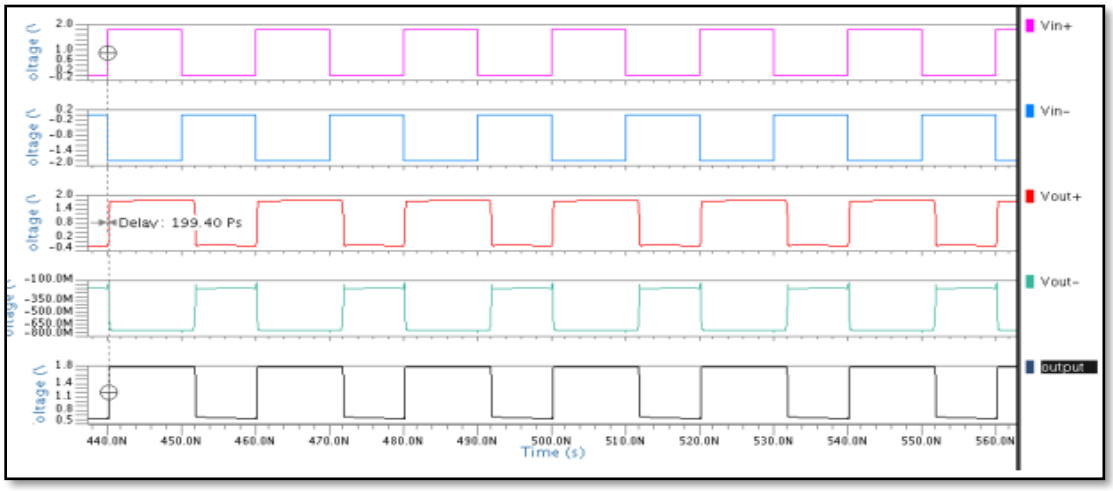


"Figure.5 Offset Voltage"

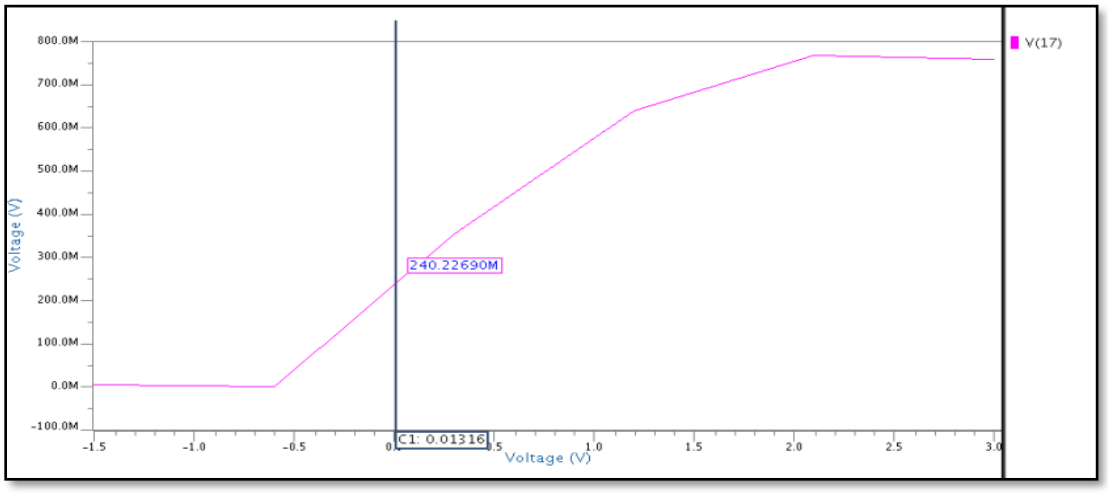


"Figure.6 Input Common Mode Range"

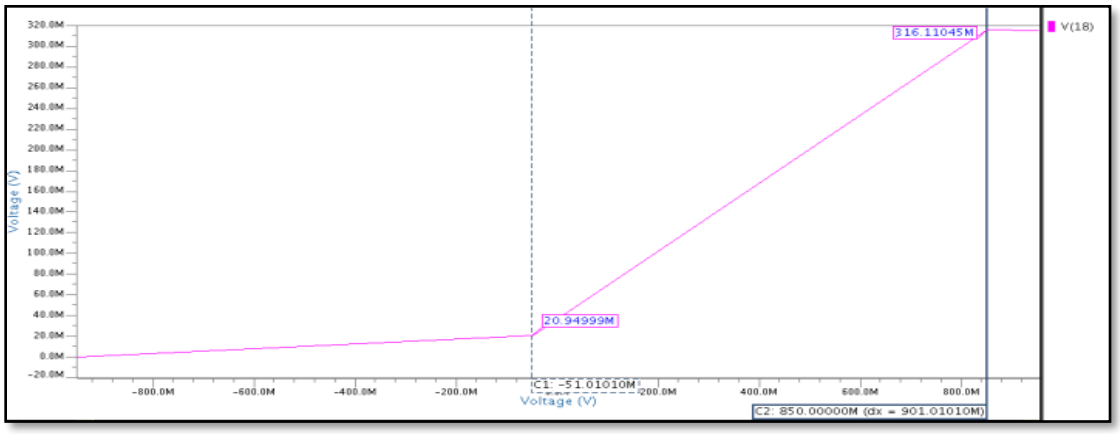
B. Simulation results of CMOS voltage comparator using offset cancellation block in 90nm Technology



"Figure.7 Transient Response"



"Fig.8 Offset Voltage"



"Fig.9 Input Common Mode Range"

V. COMPARISON

In this paper, simulated results are presented for the Charge Sharing Dynamic latch Comparator and Charge Sharing Dynamic latch Comparator using Offset Reduction Technique. The summary of the comparison is given in the Table II.

"Table 4.Simulated results of comparator with and without using offset cancellation block "

Parameters	Comparator without Offset Cancelation Block	Comparator Offset Cancelation Block
Propagation Delay(ns)	0.769	0.199
Offset(V)	0.5	0.2
ICMR(V)	1 to 2	-0.5 to 0.8
Power Dissipation(µW)	4.77	4.74

VI. CONCLUSION

In this paper, we have analyzed the effect of offset error on the performance of a Charge Sharing Dynamic Latch Comparator. The offset error of the comparator has been reduced by adding an offset reduction loop circuit reduced the offset error from 0.5V to 0.2V.

With this, it can be concluded that, the noise and error levels of a latched comparator can be reduced with proper circuit optimization which will improve the performance of the comparator.

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