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UART implementation using FPGA with configurable baudrate

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Abstract*-Universal Asynchronous Receiver Transmitter (UART) is the serial communication protocol that is used for communication in between two peripheral (device) serially. UART is a type of serial communication. now a days for specific application we need some specific keywords (features) o f UART instead of using all keywords of UART. for that, we want configure baud rate according to application. in parallel communication the complexity of system increases due to simultaneously transmission of data bits on multiple path(wires) lines. serial communication overcome these drawback of parallel communication and effective for many application for long distance communication. the implementation of UART can done through FPGA to achieve reliable ,stable and effective data transmission by using hdl language*

Keywords-*UART, HDL, FPGA, Xillinx ISE 12.1*

I. INTRODUCTION

UART transmitter send a data word in parallel form and directing the UART to send it in a serial format. As that same, which receiver receive the data in serial format, and stores the data in a parallel format. As the UART is using the asynchronous communication , the receiver cannot acknowledge the incoming of data; receiver generates a local clock for the synchronization of transmitter when start bit gets received. There is no required of generating separate clock by the transmitter. Transmitter and receiver allow the timing parameters in advance for synchronizing the Txd and Rxd units. UART is an integrated circuit which plays a important role in serial communication. UART acquires the function of conversion between the serial and parallel data. It provides Data Transfer between transmitter and receiver is at short distance and there is loss of signal distortion. Parallel communication is use for a short distance c with many number of bit address bus and data bus. Serial communication is used for a long distance transmission and is mostly used. But in some communication could not meet requirements due to Baud rate equipments. those peripheral devices have low speed we use Serial communication.

A. WHY DO WE IMPLEMENT UART?

As UART can be used when there is no compulsory for high speed and is inexpensive. The protocol can be highly configurable. The major part is matching the serial bus baud rate The main purpose of This project is sending of a data with different baud rate

B. IMPLEMENTATION OF UART

The transmitter side parallel data to serial data converter and at the receiver side serial to parallel converter. In Asynchronous serial communication, the clock are not required, but the sender and receiver must agree timing parameters. Basically Asynchronous transmission is used for long transmission distance. Hence, UART function is communication of data between computer and other devices/peripheral. UART use to full duplex communication in serial communication. This paper uses HDL language to implement the functions of Serial communication. UART communication used only two signal lines transmitting signal (Txd) & receiving signal(Rxd) for full duplex data communication. Txd is the transmitter which is output and Rxd is the receiver which is input. There are only two states available, i.e logic 1(high) and logic 0 (low) to distinguish respectively

C. BAUD RATE GENERATOR

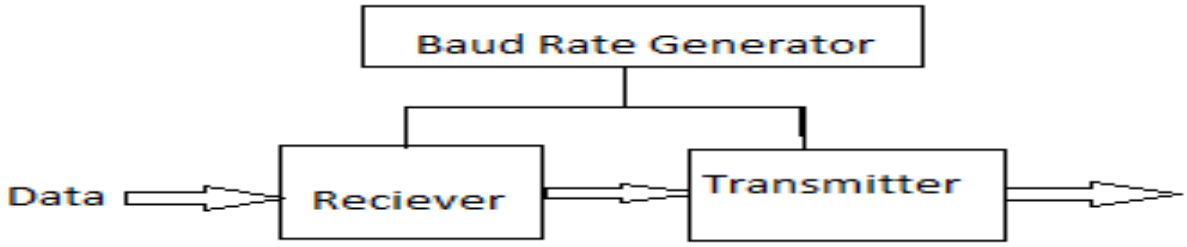


Figure 1. Baudrate Generator

Baud Rate Generator is actually a frequency divider. The frequency clock produced by the baudrate generator is not exactly the baud rate clock, but 16 times the baud rate clock. For sampling there exists the ideal time at the middle point of serial data bit. This output clock generated can be used as the receive reference clock by the receiver UART.

D. PROPOSED UART ARCHITECTURE

UART supports asynchronous serial communication in which clock is not shared between transmitter and receiver; several extra bits are sent along with data bits for synchronization purpose. This indicates that data bits are transmitted in the form of frame. This frame is received at the receiver input where de-framing is done and only the data bits are available in parallel form at the receiver side. The frame format is shown in figure 2

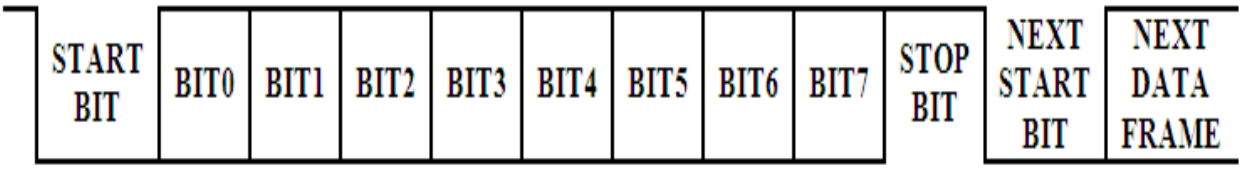
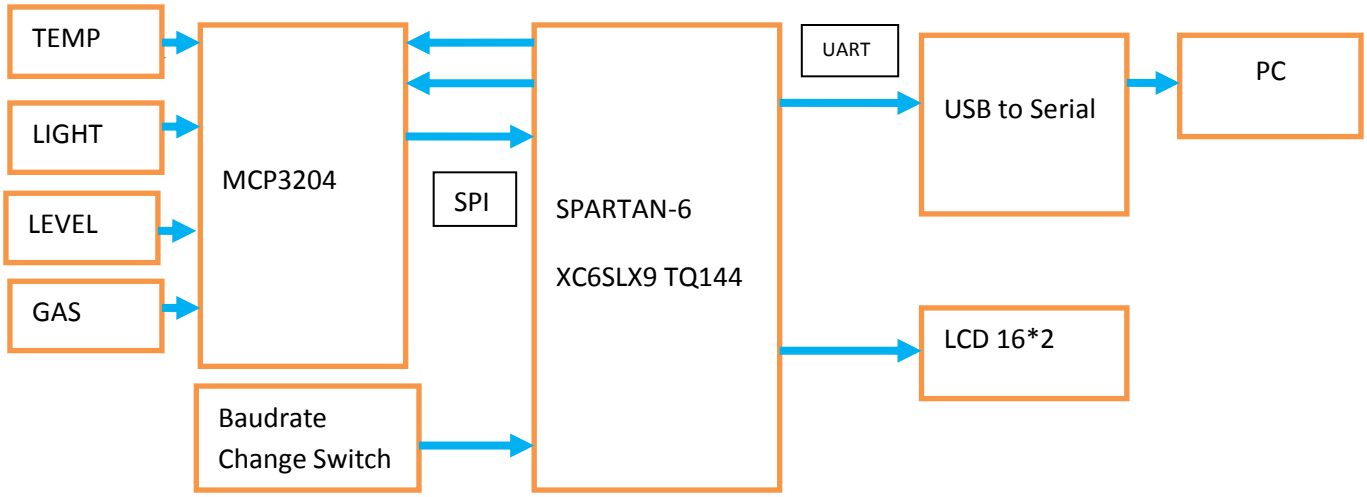


Figure 2.Frame Format For UART

II. BLOCK DIAGRAM



III. METHODOLOGY

FPGA or Field Programmable Gate Arrays can be configured by the user or designer after manufacturing and while implementation. Hence they are known as On-Site programmable. The programming of the FPGA is done using a logic diagram or a source code using a programming language to specify how the chip should work. In FPGA program can done using logic block, using HDL language. The programming of the FPGA is done using a logic circuit diagram or a source code using a programming Language likeverilog to specify how the chip should work. FPGAs have PLC (programmable logic components) known as, logic blocks, and reconfigurable interconnects which facilitate the ,wiring of the logic blocks together. The programmable logic blocks are known as configurable logic blocks and re configurable interconnects are called switch boxes. Configurable Logic blocks (CLBs) can be programmed to perform complex computational functions or simple logic gates like AND and XOR. In many FPGAs the logic blocks also include memory elements, which can be simple flip-flop or as Advantages of FPGA is as follows:

- Ability to re-program.
- High Speed.

For serial communication we need to initialization the FPGA ADC and channel of ADC.also initialize the input and output port of FPGA after that select . UART baudrate for communication our main aim is to implement the serial communication using UATR with configurable baudrate The next step is to read data from ADC channel over SPI protocol and sent to UART .in ADC we use four channel that is channel 0-3.Convert the output of sensor in to digital and store into memory. Read the data from ADC over spi communication and send to UART.UART convert these data from ADC into serial data and include extra bit that is start bit,stop bit. and send to other end peripheral device simultaneously the data is displayed on LCD. repeat the above procedure until we want take output of sensor.

IV.ADVANTAGE

1) Configurable baudrate
2) On time programming is possible
3) Reliable ,stable & compact communication.
4) It is a real time application.

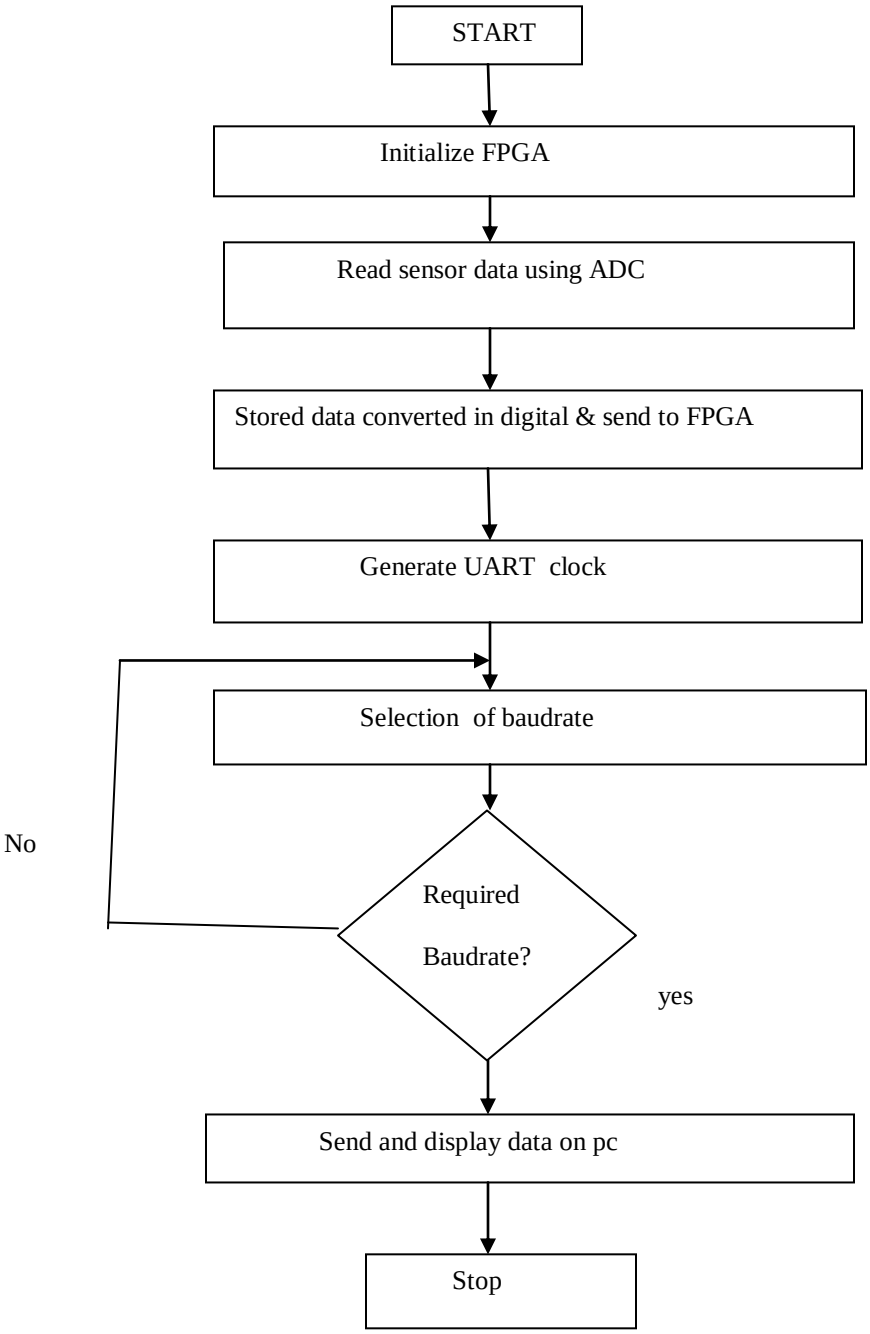
V.LIMITATIONS

1) *Cost increases*
2) For small application we can not invest large amount.

VI.APPLICATION

1) For monitoring and controlling data in industries
2) It used in real time data acquisition system.
3) It is used in GPS navigation.

VII. FLOWCHART



VIII. FUTURE SCOPE

This can be implemented through hardware if an FPGA kit is available instead of software implementation. UART Channels can be increased to speed up the data transmission.

IX. CONCLUSION

This paper describes the architecture of UART that support various data word length and different baud rates for serial transmission of data. UART which can be implemented on FPGA. Additionally we can detect the different types of errors occurred during communication and hence correct them.

X. ACKNOWLEGMENT

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